12 Output Buffer for 2 DDR and 3 SDRAM DIMMS

- **Space-saving 28-pin SSOP package**

Features

- **One input to 12 output buffer/drivers**
- **Supports up to 2 DDR DIMMs or 3 SDRAM DIMMS**
- **One additional output for feedback**
- **SMBus interface for individual output control**
- **Low skew outputs (< 100 ps)**
- **Supports 266 MHz DDR SDRAM**
- **Dedicated pin for power management support**

Functional Description

The W256 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 12 outputs. Designers can configure these outputs to support 3 unbuffered standard SDRAM DIMMs and 2 DDR DIMMs. The W256 can be used in conjunction with the W250-02 or similar clock synthesizer for the VIA Pro 266 chipset.

The W256 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up).

Block Diagram

Pin Configuration[1]

SSOP Top View

Note:

1. Internal 100K pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.
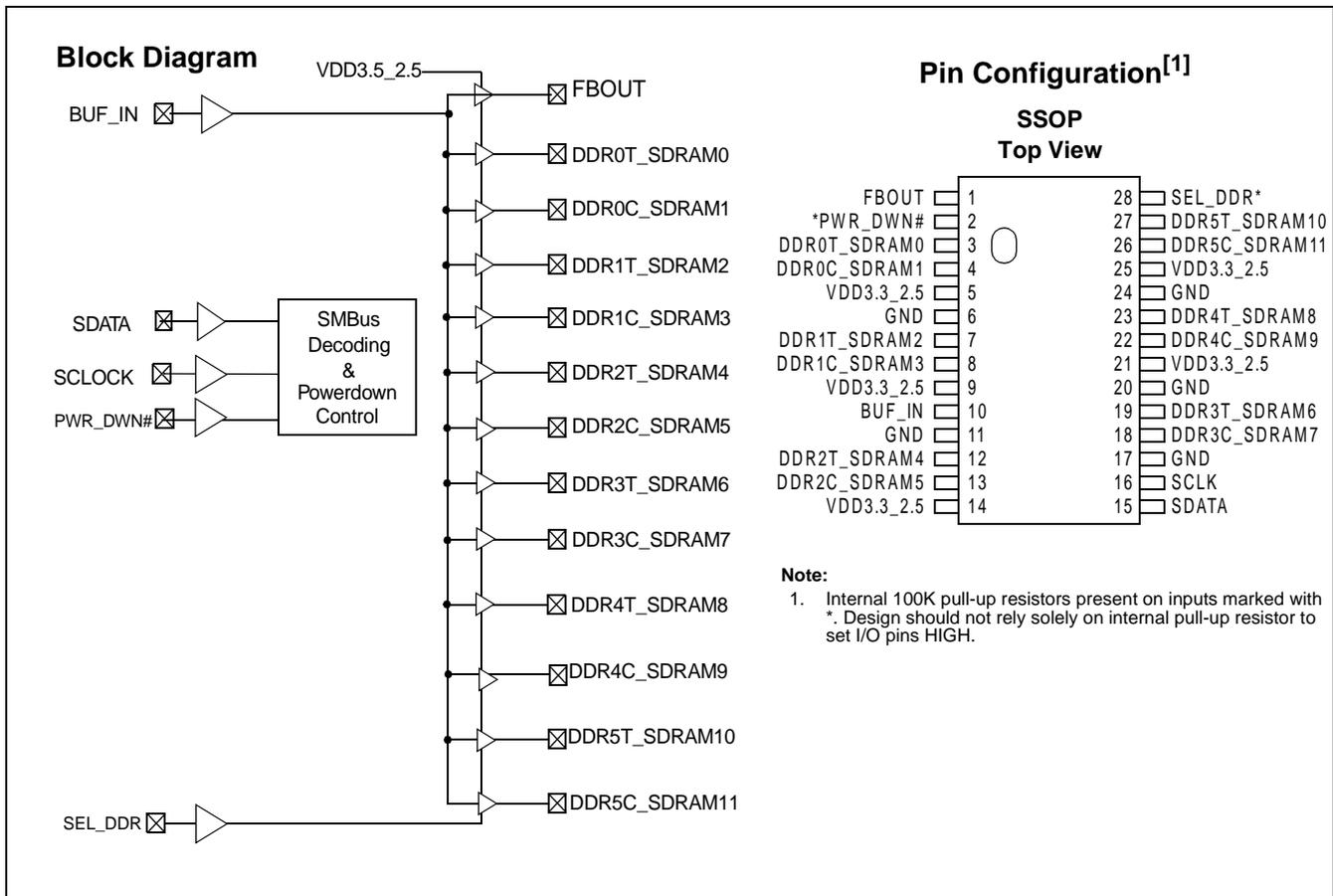
Pin Summary

Name	Pins	Description
SEL_DDR	28	Input to configure for DDR-ONLY mode or STANDARD SDRAM mode. 1 = DDR-ONLY mode. 0 = STANDARD SDRAM mode. When SEL_DDR is pulled high or configured for DDR-ONLY mode, all the buffers will be configured as DDR outputs. Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode. When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, all the buffers will be configured as STANDARD SDRAM outputs. Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode.
SCLK	16	SMBus clock input
SDATA	15	SMBus data input
BUF_IN	10	Reference input from chipset. 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.
FBOUT	1	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.
PWR_DWN#	2	Active LOW input to enable Power Down mode; all outputs will be pulled LOW.
DDR[0:5]T_SDRAM [0,2,4,6,8,10]	3, 7, 12, 19, 23, 27	Clock outputs. These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.
DDR[0:5]C_SDRAM [1,3,5,7,9, 11]	4, 8, 13, 18, 22, 26	Clock outputs. These outputs provide complementary copies of BUF_IN when SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR is inactive. Voltage swing depends on VDD3.3_2.5 power supply.
VDD3.3_2.5	5, 9, 14, 21, 25	Connect to 2.5V power supply when W256 is configured for DDR-ONLY mode. Connect to 3.3V power supply, when W256 is configured for standard SDRAM mode.
GND	6, 11, 17, 20, 24	Ground

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  .
  .
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- SMBus Address for the W256 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 6: Outputs Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	--	Reserved, drive to 0	0
Bit 6	--	Reserved, drive to 0	0
Bit 5	--	Reserved, drive to 0	0
Bit 4	1	FBOUT	1
Bit 3	27, 26	DDR5T_SDRAM10, DDR5C_SDRAM11	1
Bit 2	--	Reserved, drive to 0	1

Byte 6: Outputs Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit 1	23, 22	DDR4T_SDRAM8, DDR4C_SDRAM9	1
Bit 0	--	Reserved, drive to 0	1

Byte 7: Outputs Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	--	Reserved, drive to 0	1
Bit 6	19, 18	DDR3T_SDRAM6, DDR3C_SDRAM7	1
Bit 5	12, 13	DDR2T_SDRAM4, DDR2C_SDRAM5	1
Bit 4	--	Reserved, drive to 0	1
Bit 3	--	Reserved, drive to 0	1
Bit 2	7, 8	DDR1T_SDRAM2, DDR1C_SDRAM3	1
Bit 1	--	Reserved, drive to 0	1
Bit 0	3, 4	DDR0T_SDRAM0, DDR0C_SDRAM1	1

Maximum Ratings

Supply Voltage to Ground Potential ....–0.5 to +7.0V

DC Input Voltage (except BUF_IN) .... –0.5V to V_{DD}+0.5

Storage Temperature.................................. –65°C to +150°C

Static Discharge Voltage .... >2000V
(per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD3.3	Supply Voltage	3.135		3.465	V
VDD2.5	Supply Voltage	2.375		2.625	V
T_A	Operating Temperature (Ambient Temperature)	0		70	°C
C_{OUT}	Output Capacitance		6		pF
C_{IN}	Input Capacitance		5		pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	For all pins except SMBus			0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	$V_{IN} = 0V$			50	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$			50	μA
I_{OH}	Output HIGH Current	$VDD = 2.375V$ $V_{OUT} = 1V$	-18	-32		mA
I_{OL}	Output LOW Current	$VDD = 2.375V$ $V_{OUT} = 1.2V$	26	35		mA
V_{OL}	Output LOW Voltage[2]	$I_{OL} = 12$ mA, VDD = 2.375V			0.6	V
V_{OH}	Output HIGH Voltage[2]	$I_{OH} = -12$ mA, VDD = 2.375V	1.7			V
I_{DD}	Supply Current[2] (DDR-Only mode)	Unloaded outputs, 133 MHz			400	mA
I_{DD}	Supply Current (DDR-Only mode)	Loaded outputs, 133 MHz			500	mA
I_{DDS}	Supply Current	PWR_DWN# = 0			100	μA
V_{OUT}	Output Voltage Swing	See Test Circuity (Refer to Figure 1)	0.7		VDD +0.6	V
V_{OC}	Output Crossing Voltage		(VDD/2) -0.1	VDD/2	(VDD/2) +0.1	V
IN_{DC}	Input Clock Duty Cycle		48		52	%

Notes:
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics[Figure 3]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
--	Operating Frequency		66		133	MHz
--	Duty Cycle[2,4] = $t_2 \div t_1$	Measured at 1.4V for 3.3V outputs Measured at VDD/2 for 2.5V outputs.	IN_{DC} −5%		IN_{DC} +5%	%
t_3	SDRAM Rising Edge Rate[2]	Measured between 0.4V and 2.4V	1.0		2.50	V/ns
t_4	SDRAM Falling Edge Rate[2]	Measured between 2.4V and 0.4V	1.0		2.50	V/ns
t_{3d}	DDR Rising Edge Rate[2]	Measured between 20% to 80% of output (Refer to *Figure 1*)	0.5		1.50	V/ns
t_{4d}	DDR Falling Edge Rate[2]	Measured between 20% to 80% of output (Refer to *Figure 1*)	0.5		1.50	V/ns
t_5	Output to Output Skew[2]	All outputs equally loaded			100	ps
t_6	SDRAM Buffer HH Prop. Delay[2]	Input edge greater than 1 V/ns	5		10	ns
t_7	SDRAM Buffer LLProp. Delay[2]	Input edge greater than 1 V/ns	5		10	ns
t_8	SDRAM Buffer LLProp. Delay[2]	Input edge greater than 1 V/ns	5		10	ns

Switching Waveforms

Duty Cycle Timing
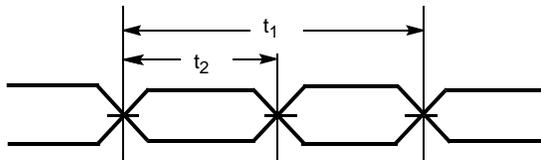
All Outputs Rise/Fall Time
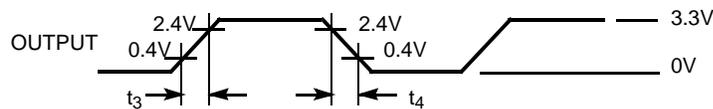
Output-Output Skew
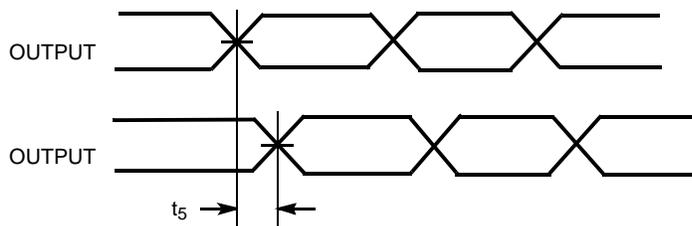
Notes:
3. All parameters specified with loaded outputs.
4. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/ns.

Switching Waveforms (continued)

SDRAM Buffer HH and LL Propagation Delay
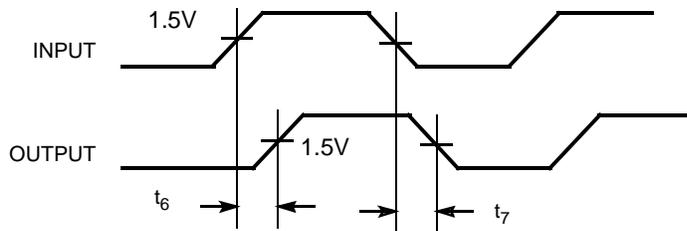
Figure 1 shows the differential clock directly terminated by a 120 Ω resistor
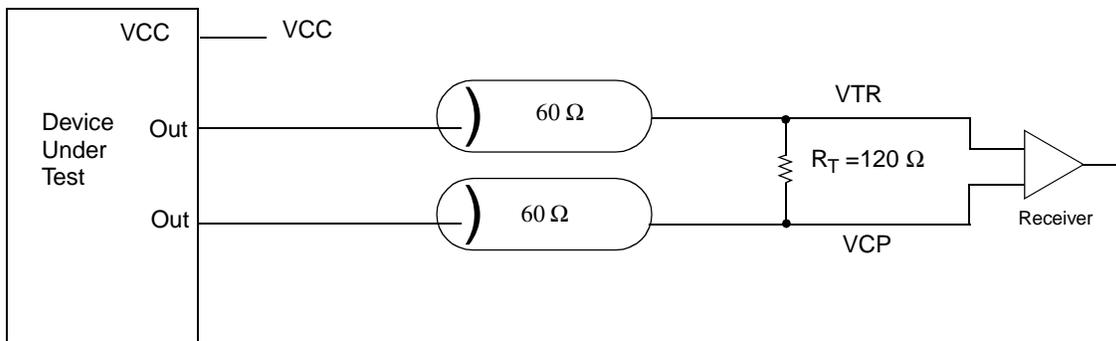
**Figure 1. Differential Signal Using Direct Termination Resistor.**

Ordering Information

Ordering Code	Package Type	Operating Range
W256	28-pin SSOP	Commercial

Document #: 38-01083-*A

Layout Example Single Voltage
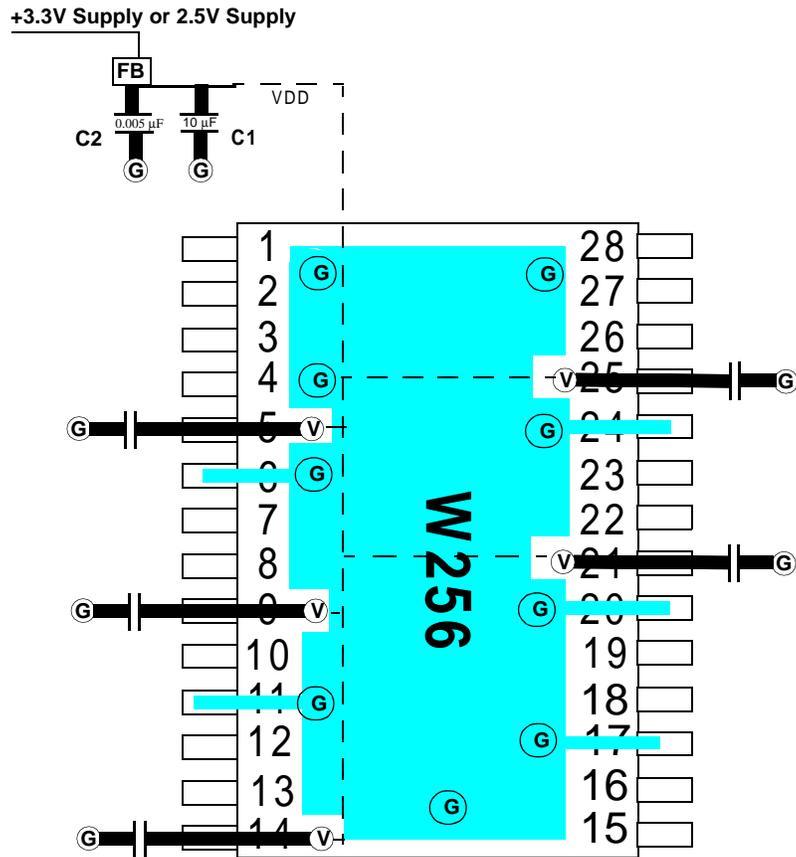
**FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)**

Cermaic Caps C1 = 10 – 22 µF   C2 = .005 µF

Ⓖ **= VIA to GND plane layer   Ⓥ =VIA to respective supply plane layer**

Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = 0.1 µF ceramic

Mechanical Package Outline

28-Pin Small Shrink Outline Package (SSOP, 209 mils)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

END VIEW

DETAIL 'A'

SECTION G-G
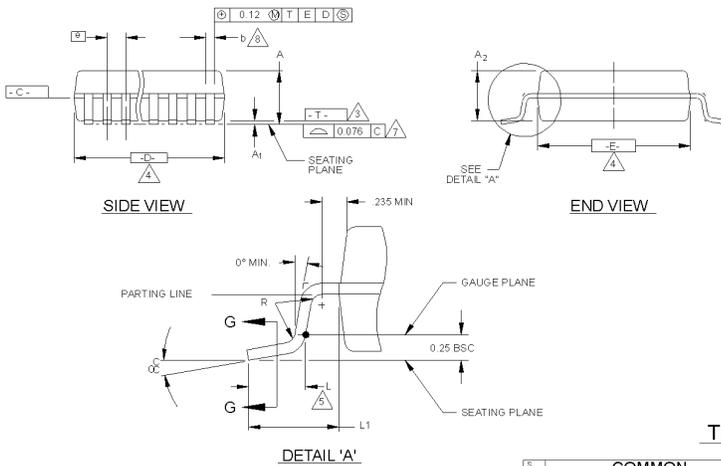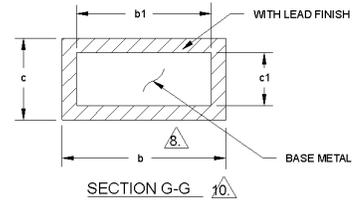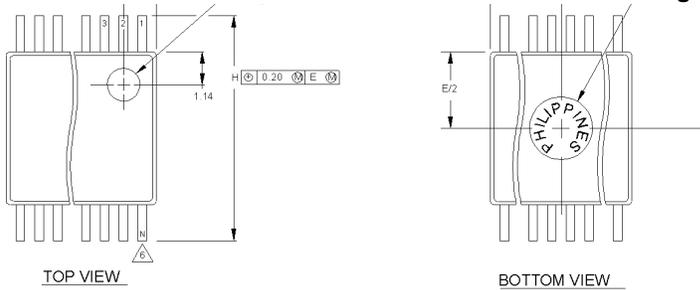
NOTES:
1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	VARI-ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
∝	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	VARI-ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A1	.002	.005	.008		AB	.239	.244	.249	16
A2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
∝	0°	4°	8°						
R	.004	.006							