Winbond Electronics Corp.

160 OUTPUT SEGMENT/COMMON STN LCD DRIVER

1. GENERAL DESCRIPTION

The WFP7151 is a 160 output segment/common driver LSI suitable driving STN dot matrix LCD panels.

Through the use of SST (Super Slim TCP) technology.

It is ideal for substantially decreasing the size of the frame section of the LCD module.

The WFP7151 is good both segment driver and common driver and a low power consuming, high-precision LCD panel display can be assembled.

2. FEATURES AND BENEFITS

(Segment mode)

- Shift clock frequency up to 8 MHz
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with MD pin.
- Automatic transfer function of an enable signal.
- Automatic counting function which in the chip select mode causes the internal clock to be stopped by automatically counting 160 of input data.

(Common model)

- Shift clock frequency up to 4 MHz
- Built-in 160-bits bi-directional shift register (divisible into 80-bits x 2)

  (80-bits shift register x 2)

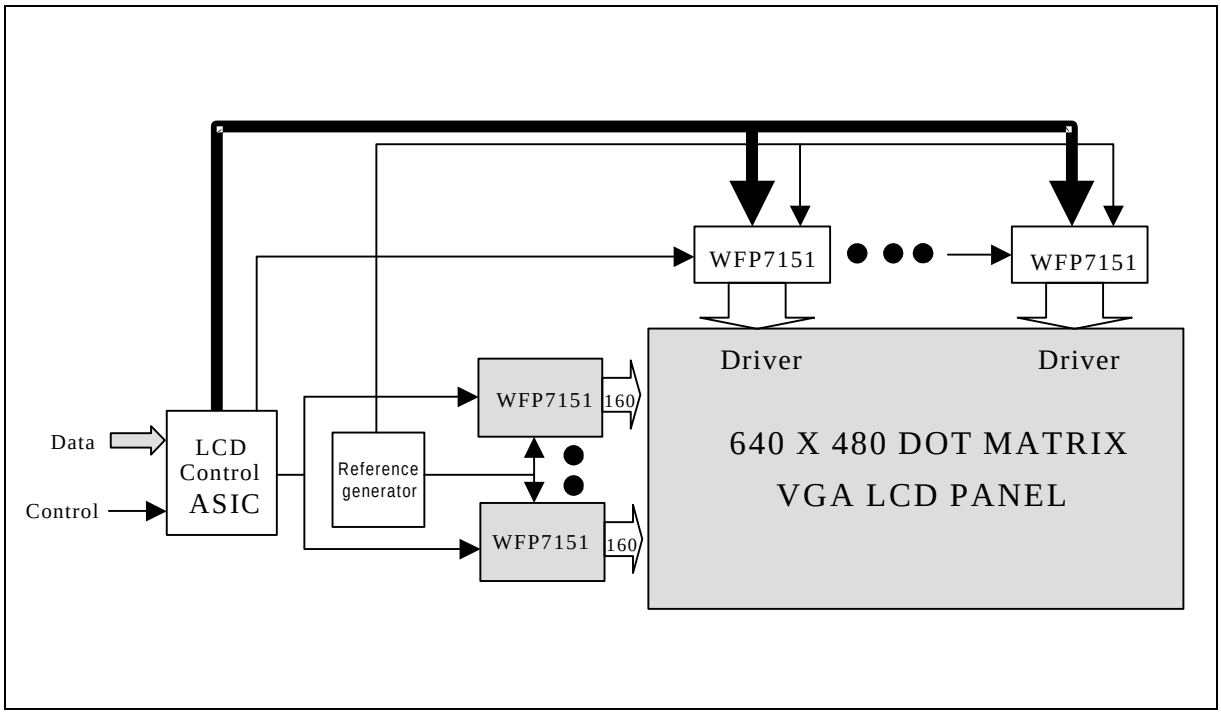
  (1) Y1 - Y160 single mode
  (2) Y160 - Y1
  (3) Y1 - Y80, Y81 - Y160 Dual mode
  (4) Y160 - Y81, Y80 - Y1

The above 4 shift directions are pin-selectable

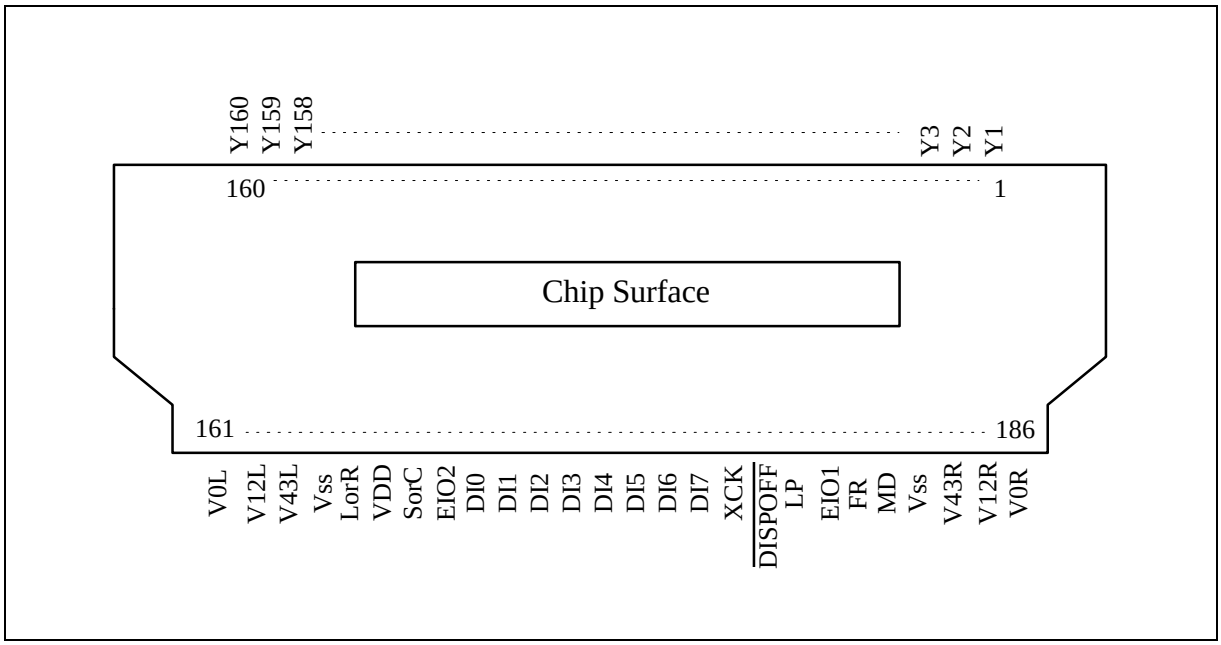
(Others)

- Supply voltage for LCD drive : +10 to +30V
- Number of LCD drive outputs : 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system : +2.5 to +5.5V
- CMOS silicon gate process (P-type silicon substrate)
- Packaged in TCP

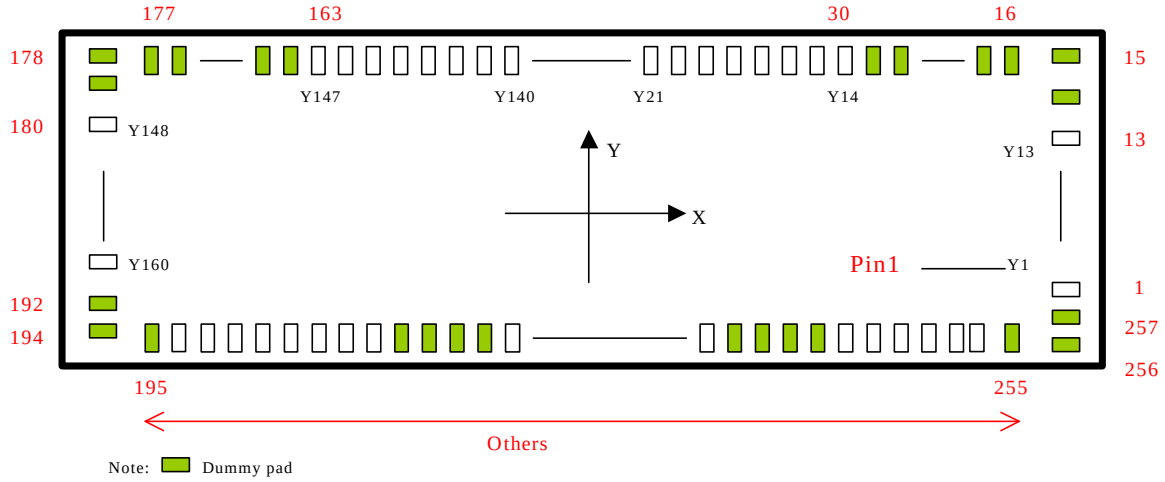
3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PAD CONFIGURATION



PARAMETER	PAD NO.	SIZE (X.)	SIZE (Y.)	UNIT
Chip Size		12317	1481	µm x µm
Pad Pitch	1 to 194 & 256, 257	70 (min.)		µm
Pad Pitch	195 to 255	140 (min.)		µm
Bumped Pad Size	1 to 15, & 178 to 194 & 256, 257	113	45	µm
Bumped Pad Size	16 to 177	45	113	µm
Bumped Pad Size	195 to 255	89	113	µm
Bumped Pad High	all pads	COG 15 TCP 20		µm
Wafer Thickness		25		mil

5.1 PAD Coordinates

PAD NO.	PAD NAME	PIN NAME	X.	Y.
1	Y<1>	1	5940.000	-429.000
2	Y<2>	2	5940.000	-359.000
3	Y<3>	3	5940.000	-289.000
4	Y<4>	4	5940.000	-219.000
5	Y<5>	5	5940.000	-149.000
6	Y<6>	6	5940.000	-79.000
7	Y<7>	7	5940.000	-9.000
8	Y<8>	8	5940.000	61.000
9	Y<9>	9	5940.000	131.000
10	Y<10>	10	5940.000	201.000
11	Y<11>	11	5940.000	271.000
12	Y<12>	12	5940.000	341.000
13	Y<13>	13	5940.000	411.000
14	DUMR<3>	14	5940.000	481.000
15	DUMR<4>	15	5940.000	551.000
16	DUMT<28>	16	5635.000	547.000
17	DUMT<27>	17	5565.000	547.000
18	DUMT<26>	18	5495.000	547.000
19	DUMT<25>	19	5425.000	547.000
20	DUMT<24>	20	5355.000	547.000
21	DUMT<23>	21	5285.000	547.000
22	DUMT<22>	22	5215.000	547.000
23	DUMT<21>	23	5145.000	547.000
24	DUMT<20>	24	5075.000	547.000
25	DUMT<19>	25	5005.000	547.000
26	DUMT<18>	26	4935.000	547.000
27	DUMT<17>	27	4865.000	547.000
28	DUMT<16>	28	4795.000	547.000
29	DUMT<15>	29	4725.000	547.000
30	Y<14>	30	4655.000	547.000
31	Y<15>	31	4585.000	547.000
32	Y<16>	32	4515.000	547.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
33	Y<17>	33	4445.000	547.000
34	Y<18>	34	4375.000	547.000
35	Y<19>	35	4305.000	547.000
36	Y<20>	36	4235.000	547.000
37	Y<21>	37	4165.000	547.000
38	Y<22>	38	4095.000	547.000
39	Y<23>	39	4025.000	547.000
40	Y<24>	40	3955.000	547.000
41	Y<25>	41	3885.000	547.000
42	Y<26>	42	3815.000	547.000
43	Y<27>	43	3745.000	547.000
44	Y<28>	44	3675.000	547.000
45	Y<29>	45	3605.000	547.000
46	Y<30>	46	3535.000	547.000
47	Y<31>	47	3465.000	547.000
48	Y<32>	48	3395.000	547.000
49	Y<33>	49	3325.000	547.000
50	Y<34>	50	3255.000	547.000
51	Y<35>	51	3185.000	547.000
52	Y<36>	52	3115.000	547.000
53	Y<37>	53	3045.000	547.000
54	Y<38>	54	2975.000	547.000
55	Y<39>	55	2905.000	547.000
56	Y<40>	56	2835.000	547.000
57	Y<41>	57	2765.000	547.000
58	Y<42>	58	2695.000	547.000
59	Y<43>	59	2625.000	547.000
60	Y<44>	60	2555.000	547.000
61	Y<45>	61	2485.000	547.000
62	Y<46>	62	2415.000	547.000
63	Y<47>	63	2345.000	547.000
64	Y<48>	64	2275.000	547.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
65	Y<49>	65	2205.000	547.000
66	Y<50>	66	2135.000	547.000
67	Y<51>	67	2065.000	547.000
68	Y<52>	68	1995.000	547.000
69	Y<53>	69	1925.000	547.000
70	Y<54>	70	1855.000	547.000
71	Y<55>	71	1785.000	547.000
72	Y<56>	72	1715.000	547.000
73	Y<57>	73	1645.000	547.000
74	Y<58>	74	1575.000	547.000
75	Y<59>	75	1505.000	547.000
76	Y<60>	76	1435.000	547.000
77	Y<61>	77	1365.000	547.000
78	Y<62>	78	1295.000	547.000
79	Y<63>	79	1225.000	547.000
80	Y <64>	80	1155.000	547.000
81	Y<65>	81	1085.000	547.000
82	Y<66>	82	1015.000	547.000
83	Y<67>	83	945.000	547.000
84	Y<68>	84	875.000	547.000
85	Y<69>	85	805.000	547.000
86	Y<70>	86	735.000	547.000
87	Y<71>	87	665.000	547.000
88	Y<72>	88	595.000	547.000
89	Y<73>	89	525.000	547.000
90	Y<74>	90	455.000	547.000
91	Y<75>	91	385.000	547.000
92	Y<76>	92	315.000	547.000
93	Y<77>	93	245.000	547.000
94	Y<78>	94	175.000	547.000
95	Y<79>	95	105.000	547.000
96	Y<80>	96	35.000	547.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
97	Y<81>	97	-35.000	547.000
98	Y<82>	98	-105.000	547.000
99	Y<83>	99	-175.000	547.000
100	Y<84>	100	-245.000	547.000
101	Y<85>	101	-315.000	547.000
102	Y<86>	102	-385.000	547.000
103	Y<87>	103	-455.000	547.000
104	Y<88>	104	-525.000	547.000
105	Y<89>	105	-595.000	547.000
106	Y<90>	106	-665.000	547.000
107	Y<91>	107	-735.000	547.000
108	Y<92>	108	-805.000	547.000
109	Y<93>	109	-875.000	547.000
110	Y<94>	110	-945.000	547.000
111	Y<95>	111	-1015.000	547.000
112	Y<96>	112	-1085.000	547.000
113	Y<97>	113	-1155.000	547.000
114	Y<98>	114	-1225.000	547.000
115	Y<99>	115	-1295.000	547.000
116	Y<100>	116	-1365.000	547.000
117	Y<101>	117	-1435.000	547.000
118	Y<102>	118	-1505.000	547.000
119	Y<103>	119	-1575.000	547.000
120	Y<104>	120	-1645.000	547.000
121	Y<105>	121	-1715.000	547.000
122	Y<106>	122	-1785.000	547.000
123	Y<107>	123	-1855.000	547.000
124	Y<108>	124	-1925.000	547.000
125	Y<109>	125	-1995.000	547.000
126	Y<110>	126	-2065.000	547.000
127	Y<111>	127	-2135.000	547.000
128	Y<112>	128	-2205.000	547.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
129	Y<113>	129	-2275.000	547.000
130	Y<114>	130	-2345.000	547.000
131	Y<115>	131	-2415.000	547.000
132	Y<116>	132	-2485.000	547.000
133	Y<117>	133	-2555.000	547.000
134	Y<118>	134	-2625.000	547.000
135	Y<119>	135	-2695.000	547.000
136	Y<120>	136	-2765.000	547.000
137	Y<121>	137	-2835.000	547.000
138	Y<122>	138	-2905.000	547.000
139	Y<123>	139	-2975.000	547.000
140	Y<124>	140	-3045.000	547.000
141	Y<125>	141	-3115.000	547.000
142	Y<126>	142	-3185.000	547.000
143	Y<127>	143	-3255.000	547.000
144	Y<128>	144	-3325.000	547.000
145	Y<129>	145	-3395.000	547.000
146	Y<130>	146	-3465.000	547.000
147	Y<131>	147	-3535.000	547.000
148	Y<132>	148	-3605.000	547.000
149	Y<133>	149	-3675.000	547.000
150	Y<134>	150	-3745.000	547.000
151	Y<135>	151	-3815.000	547.000
152	Y<136>	152	-3885.000	547.000
153	Y<137>	153	-3955.000	547.000
154	Y<138>	154	-4025.000	547.000
155	Y<139>	155	-4095.000	547.000
156	Y<140>	156	-4165.000	547.000
157	Y<141>	157	-4235.000	547.000
158	Y<142>	158	-4305.000	547.000
159	Y<143>	159	-4375.000	547.000
160	Y<144>	160	-4445.000	547.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
161	Y<145>	161	-4515.000	547.000
162	Y<146>	162	-4585.000	547.000
163	Y<147>	163	-4655.000	547.000
164	DUMT<14>	164	-4725.000	547.000
165	DUMT<13>	165	-4795.000	547.000
166	DUMT<12>	166	-4865.000	547.000
167	DUMT<11>	167	-4935.000	547.000
168	DUMT<10>	168	-5005.000	547.000
169	DUMT<9>	169	-5075.000	547.000
170	DUMT<8>	170	-5145.000	547.000
171	DUMT<7>	171	-5215.000	547.000
172	DUMT<6>	172	-5285.000	547.000
173	DUMT<5>	173	-5355.000	547.000
174	DUMT<4>	174	-5425.000	547.000
175	DUMT<3>	175	-5495.000	547.000
176	DUMT<2>	176	-5565.000	547.000
177	DUMT<1>	177	-5635.000	547.000
178	DUML<4>	178	-5940.000	551.000
179	DUML<3>	179	-5940.000	481.000
180	Y<148>	180	-5940.000	411.000
181	Y<149>	181	-5940.000	341.000
182	Y<150>	182	-5940.000	271.000
183	Y<151>	183	-5940.000	201.000
184	Y<152>	184	-5940.000	131.000
185	Y<153>	185	-5940.000	61.000
186	Y<154>	186	-5940.000	-9.000
187	Y<155>	187	-5940.000	-79.000
188	Y<156>	188	-5940.000	-149.000
189	Y<157>	189	-5940.000	-219.000
190	Y<158>	190	-5940.000	-289.000
191	Y<159>	191	-5940.000	-359.000
192	Y<160>	192	-5940.000	-429.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
193	DUML<2>	193	-5940.000	-499.000
194	DUML<1>	194	-5940.000	-569.000
195	DUMB<1>	195	-5634.400	-565.000
196	V0	196	-5479.400	-565.000
197	V12	197	-5339.400	-565.000
198	V43	198	-5199.400	-565.000
199	DUMB<2>	199	-5058.700	-565.000
200	VSS	200	-4809.700	-565.000
201	DUMB<3>	201	-4669.700	-565.000
202	LorR	202	-4529.700	-565.000
203	DUMB<4>	203	-4389.700	-565.000
204	DUMB<5>	204	-4249.700	-565.000
205	VDD	205	-3999.200	-565.000
206	DUMB<10>	206	-3859.200	-565.000
207	DUMB<11>	207	-3719.200	-565.000
208	SorC	208	-3579.200	-565.000
209	DUMB<14>	209	-3439.200	-565.000
210	DUMB<15>	210	-3299.200	-565.000
211	EIO2	211	-2815.800	-565.000
212	DUMB<18>	212	-2675.800	-565.000
213	DI<0>	213	-2535.800	-565.000
214	DUMB<21>	214	-2176.300	-565.000
215	DI<1>	215	-2036.300	-565.000
216	DUMB<24>	216	-1676.800	-565.000
217	DI<2>	217	-1536.800	-565.000
218	DUMB<28>	218	-1177.300	-565.000
219	DI<3>	219	-1037.300	-565.000
220	DUMB<32>	220	-677.800	-565.000
221	DUMB<33>	221	-537.800	-565.000
222	DI<4>	222	-397.800	-565.000
223	DUMB<36>	223	-38.300	-565.000
224	DI<5>	224	101.700	-565.000
225	DUMB<40>	225	461.200	-565.000

5.1 PAD Coordinates, continued

PAD NO.	PAD NAME	PIN NAME	X.	Y.
226	DI<6>	226	601.200	-565.000
227	DUMB<44>	227	960.700	-565.000
228	DI<7>	228	1100.700	-565.000
229	DUMB<45>	229	1460.200	-565.000
230	DUMB<46>	230	1600.200	-565.000
231	XCK	231	1740.200	-565.000
232	DUMB<47>	232	1880.200	-565.000
233	DUMB<48>	233	2020.200	-565.000
234	DISPOFF	234	2160.200	-565.000
235	DUMB<49>	235	2300.200	-565.000
236	DUMB<50>	236	2440.200	-565.000
237	LP	237	2580.200	-565.000
238	DUMB<51>	238	2720.200	-565.000
239	EIO1	239	2860.200	-565.000
240	DUMB<52>	240	3343.600	-565.000
241	DUMB<53>	241	3483.600	-565.000
242	DUMB<54>	242	3623.600	-565.000
243	DUMB<55>	243	3763.600	-565.000
244	DUMB<56>	244	3903.600	-565.000
245	FR	245	4113.100	-565.000
246	DUMB<57>	246	4253.100	-565.000
247	DUMB<58>	247	4393.100	-565.000
248	MD	248	4533.100	-565.000
249	DUMB<59>	249	4673.100	-565.000
250	Vss	250	4919.100	-565.000
251	DUMB<60>	251	5063.600	-565.000
252	V43	252	5203.600	-565.000
253	V12	253	5343.600	-565.000
254	V0	254	5483.600	-565.000
255	DUMB<79>	255	5623.600	-565.000
256	DUMR<2>	256	5940.000	-499.000
257	DUMR<1>	257	5940.000	-569.000

6. PIN DESCRIPTION

6.1 Pin Functions

(Segment mode)

CLASSIFICATION	SYM.	NAME	INPUT/ OUTPUT	FUNCTION
Power Supply	VDD	VDD	Input	Logic power supply (+2.5 ~ +5.5V)
Power Supply	GND	GND	Input	Ground
Power Supply	V0R, V0L	V0	Input	Power supply pin for LCD driver voltage
Power Supply	V12R, V12L	V12	Input	Power supply pin for LCD driver voltage
Power Supply	V43R, V43L	V43	Input	Power supply pin for LCD driver voltage
Power Supply	LorR		Input	Direction selection pin for reading display data (1) Set L/R = Vss, data is read sequentially from Y160 to Y1 (2) Set L/R = VDD, data is read sequentially from Y1 to Y160
Control Signal	XCK	Clock1	Input	Clock input pin for taking display data Data is read on the falling edge of the clock pulse
Control Signal	LP	Clock2	Input	Latch pulse input pin for display data Data is latched on the falling edge of the clock pulse
Control Signal	MD	Mode	Input	Mode selection pin (1) When MD = Vss, 4-bit parallel input mode is set (2) When MD = VDD, 8-bit parallel input mode is set
Control Signal	DI0~DI7	Data 0 to Data 7	Input	Input pin for display data (1) In 4-bit mode, input data into DI0~DI3 DI4~DI7 connect to Vss or VDD (2) In 8-bit mode, input data into DI0~DI7

6.1 Pin Functions (Segment mode), continued

CLASSIFICATION	SYM.	NAME	INPUT/ OUTPUT	FUNCTION
Control Signal	FR	AC control	Input	AC signal input for LCD driving waveform (1) The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit (2) Normally inputs a frame inversion signal (3)The LCD driver output pin's output voltage level can be set using the line latch output signal and the FR signal. (4) Trueth table shown in Table 4-1
Control Signal	DISPOFF	Display Off	Input	Control input pin for output deselect level (1)The input signal is level-shifted from logic voltage level to LCD drive voltage level and controls LCD drive circuit (2) Set to Vss, LCD drive output pins are set to Vss (3) Set to Vss, the contents of the line latch are reset, but read the display data in the data latch regardless of condition of DISPLAY, When DISPLAY function is cancelled, the driver outputs deselect level (V12 or V34), then outputs the contents of the data latch on the next falling edge of the LP, That time if DISPLAY removal time can not keep regulation what is shown AC characteristics, can not output the reading data correctly.
Control Signal	EIO1 EIO2	Enable I/O	Input/ Output	Chip selecting enable or providing chip selecting signal (1) Set L/R = Vss, EIO1 is output, EIO2 is input (2) Set L/R = V_{DD}, EIO1 is input, EIO2 is output (3) During output set to "H", while LP*XCK is "H" and after 160-bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK). after which is return to "H". (4) During input, after the LP signal is input, the chip is selected while EI is set to "L", After 160-bits of data have been read, the chip is deselected.
Control Signal	SorC	Mode select	Input	Segment mode/common mode selection pin Set SorC = V_{DD}, segment mode is set
LCD Driver Output	Y1-Y160	Y1... Y160	Output	LCD segment driver output pins

6.1 Pin Functions, continued

(Common mode)

CLASSIFICATION	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
Power Supply	VDD	VDD	Input	Logic power supply (+2.5 ~ +5.5V)
Power Supply	GND	GND	Input	Ground
Power Supply	V0R, V0L	V0	Input	Power supply pin for LCD driver voltage
Power Supply	V12R, V12L	V12	Input	Power supply pin for LCD driver voltage
Power Supply	V43R, V43L	V43	Input	Power supply pin for LCD driver voltage
Power Supply	LorR		Input	Bidirection shift register shift bidirection selection pin Data is shifted left when set to Vss, ans data is shifted right when set to "H".
Control Signal	XCK		Input	Not used XCK is pull-down in common mode, so connect to Vss
Control Signal	LP	Clock2	Input	Bidirectional shift register shift clock pulse input pin Data is shifted on the falling edge of clock pulse
Control Signal	MD	Mode	Input	Mode selection pin (1) When MD = Vss, single mode operation is selected (2) When MD = VDD, dual mode operation is selected
Control Signal	DI7	Data 7	Input	Dual mode data input pin According to the data shift direction of the data shift register, data can be input starting from the 8lst bit. (1) When the chip is used as Dual mode, DI7 will be pull-down. (2) When the chip is used as Single mode DI7 won't pull-down
Control Signal	DI0~DI6	Data 0 to Data 6	Input	Not used Connect to Vss or VDD
Control Signal	FR	AC control	Input	AC signal input for LCD driving waveform (1) The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit (2) Normally inputs a frame inversion signal (3) The LCD driver output pin's output voltage level can be set using the line latch output signal and the FR signal. (4) Trueth table shown in Table 4-2

6.1 Pin Functions (Common mode), continued

CLASSIFICATION	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
Control Signal	DISPOFF	Display Off	Input	Control input pin for output deselect level (1) The input signal is level-shifted from logic voltage level to LCD drive voltage level and controls LCD drive circuit (2) Set to Vss, LCD drive output pins are set to Vss (3) Set to Vss, the contents of the line latch are reset, but read the display data in the data latch regardless of condition of DISPLAY, When DISPLAY function is cancelled, the driver outputs deselect level (V12 or V34), then outputs the contents of the data latch on the next falling edge of the LP, That time if DISPLAY removal time can not keep regulation what is shown AC characteristics, can not output the reading data correctly.
Control Signal	EIO1	Enable I/O	Input/ Output	Bidirectional shift register shift data input/output pin Input pin for right shift, output pin for left shift When EIO1 is used as input pin for right shift, it will be pull-down When EIO1 is used as output pin for left shift, it won't be pull-down
Control Signal	EIO2	Enable I/O	Input/ Output	Bidirectional shift register shift data input/output pin Input pin for left shift, output pin for right shift When EIO2 is used as input pin for left shift, it will be pull-down When EIO2 is used as output pin for right shift, it won't be pull-down
Control Signal	SorC	Mode Select	Input	Segment mode/common mode selection pin Set SorC = Vss, "L", common mode is set
LCD driver output	Y1-Y160	Y1... Y160	Output	LCD segment driver output pins

6.2 Functional Operations

6.2.1 Truth Table

Table 6-1 (Segment mode)

FR	LATCH DATA	DISPOFF	DRIVER OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V43
L	H	H	Vss
H	L	H	V12
H	H	H	V0
X	X	L	Vss

Here, Vss < V43 < V12 < V0, H: V_{DD} (+2.5 ~ +5.5V), L: Vss(0V), X : Don't care

Note: There are two kinds of power supply (logic level voltage, LCD drive voltage) for LCD driver, Please supply regular voltage which assigned by specification for each power pin. X should be VDD or Vss, avoiding floating

Table 6-2 (Common mode)

FR	LATCH DATA	DISPOFF	DRIVER OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	Vss
X	X	L	Vss

Here, Vss < V43 < V12 < V0, H: V_{DD} (+2.5 ~ +5.5V), L: Vss (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD drive voltage) for LCD driver, Please supply regular voltage which assigned by specification for each power pin. X should be VDD or Vss, avoiding floating

Table 6-3 (Segment Mode)

A. 4-bit parallel mode

MD	LorR	EIO1	EIO2	Data Input	Figure of Clock						
					40clock	39clock	38clock	------	3clock	2clock	1clock
L	L	Output	Input	DI0	Y1	Y5	Y9	----	Y149	Y153	Y157
				DI1	Y2	Y6	Y10	----	Y150	Y154	Y158
				DI2	Y3	Y7	Y11	----	Y151	Y155	Y159
				DI3	Y4	Y8	Y12	----	Y152	Y156	Y160
L	H	Input	Output	DI0	Y160	Y156	Y152	----	Y12	Y8	Y4
				DI1	Y159	Y155	Y151	----	Y11	Y7	Y3
				DI2	Y158	Y154	Y150	----	Y10	Y6	Y2
				DI3	Y157	Y153	Y149	----	Y9	Y5	Y1

B. 8-bit parallel mode

MD	LorR	EIO1	EIO2	Data Input	Figure of Clock						
					20clock	19clock	18clock	------	3clock	2clock	1clock
H	L	Output	Input	DI0	Y1	Y9	Y17	----	Y137	Y145	Y153
				DI1	Y2	Y10	Y18	----	Y138	Y146	Y154
				DI2	Y3	Y11	Y19	----	Y139	Y147	Y155
				DI3	Y4	Y12	Y20	----	Y140	Y148	Y156
				DI4	Y5	Y13	Y21	----	Y141	Y149	Y157
				DI5	Y6	Y14	Y22	----	Y142	Y150	Y158
				DI6	Y7	Y15	Y23	----	Y143	Y151	Y159
				DI7	Y8	Y16	Y24	----	Y144	Y152	Y160
H	H	Input	Output	DI0	Y160	Y152	Y144	----	Y24	Y16	Y8
				DI1	Y159	Y151	Y143	----	Y23	Y15	Y7
				DI2	Y158	Y150	Y142	----	Y22	Y14	Y6
				DI3	Y157	Y149	Y141	----	Y21	Y13	Y5
				DI4	Y156	Y148	Y140	----	Y20	Y12	Y4
				DI5	Y155	Y147	Y139	----	Y19	Y11	Y3
				DI6	Y154	Y146	Y138	----	Y18	Y10	Y2
				DI7	Y153	Y145	Y137	----	Y17	Y9	Y1

(Common Mode)

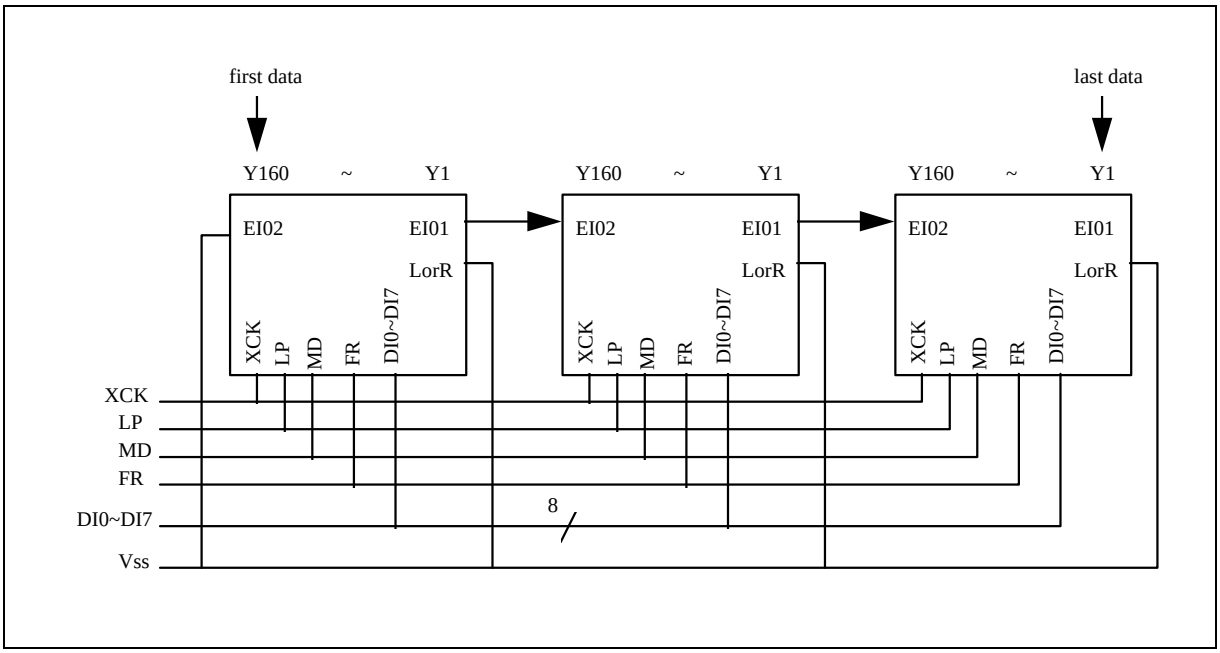
MD	LorR	Data Transfer Direction	EIO1	EI02	DI7
L (Single)	L(shift to left)	Y160 to Y1	Output	Input	X
	H(shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L(shift to left)	Y160 to Y81 Y80 to Y1	Output	Input	Input
	H(shift to right)	Y1 to Y80 Y81 to Y160	Input	Output	Input

Here: L: Vss (0V), H: VDD (+2.5 ~ +5.5V), X: don't care

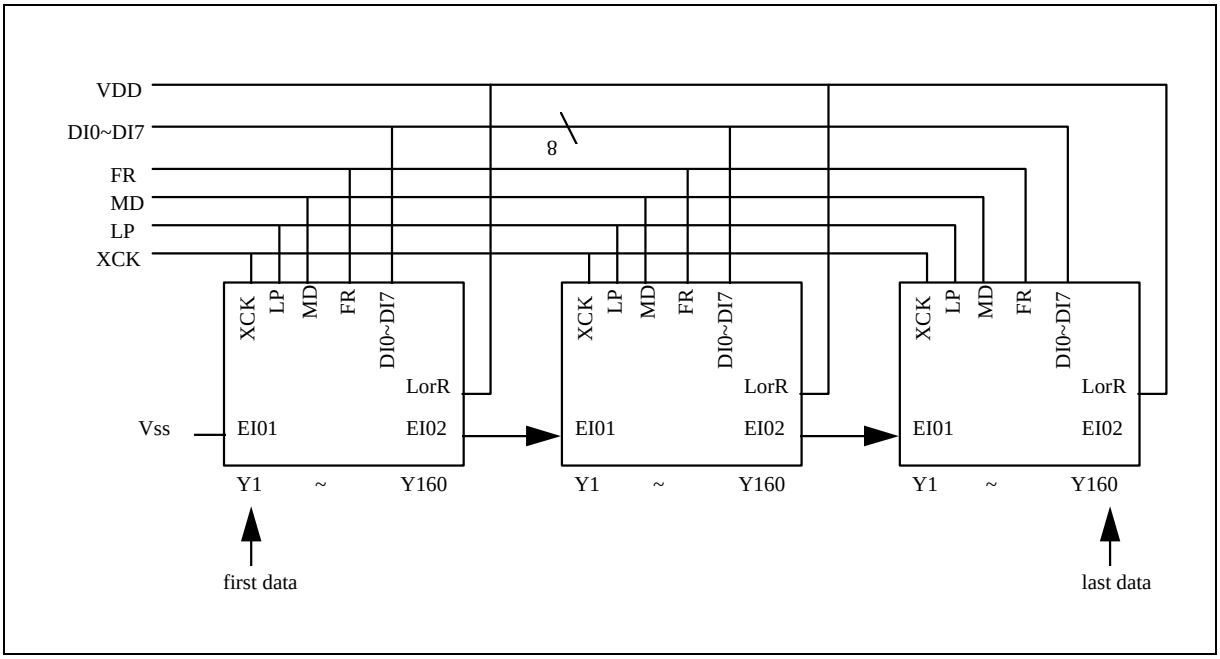
Note: Don' t care means fixed to "H" or "L", avoiding floating.

6.2.2 Connection Examples of Plural Segment Drivers

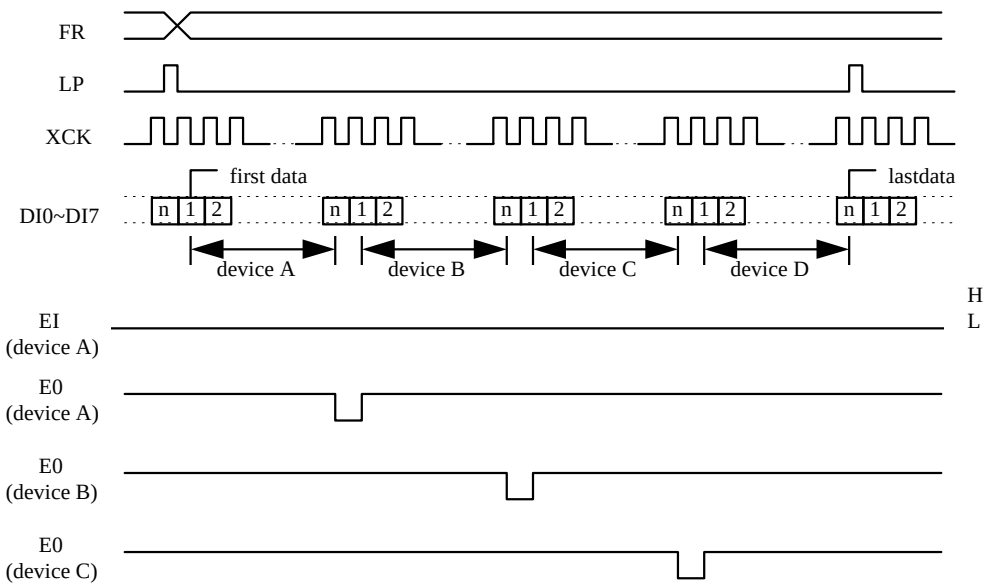
(1) Case of LorR = "L"



(2) Case of LorR = "H"



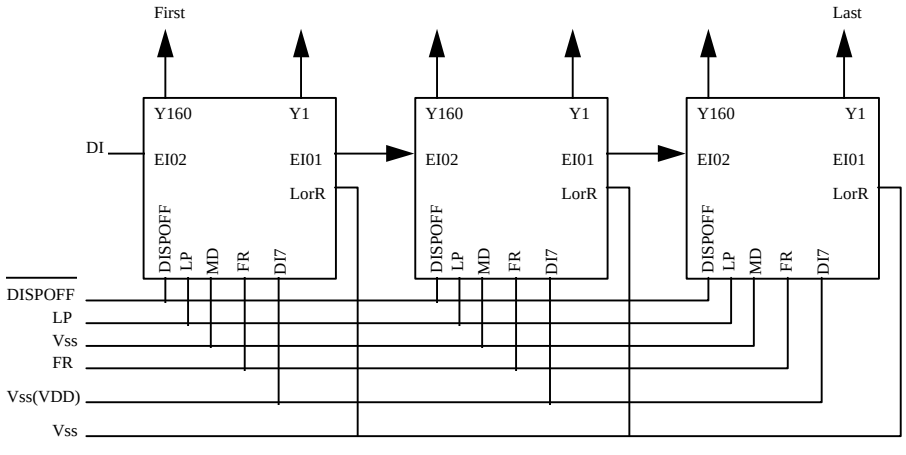
6.2.3 Timing Chart 0f 4-Device Cascade Connection of Segment Drivers



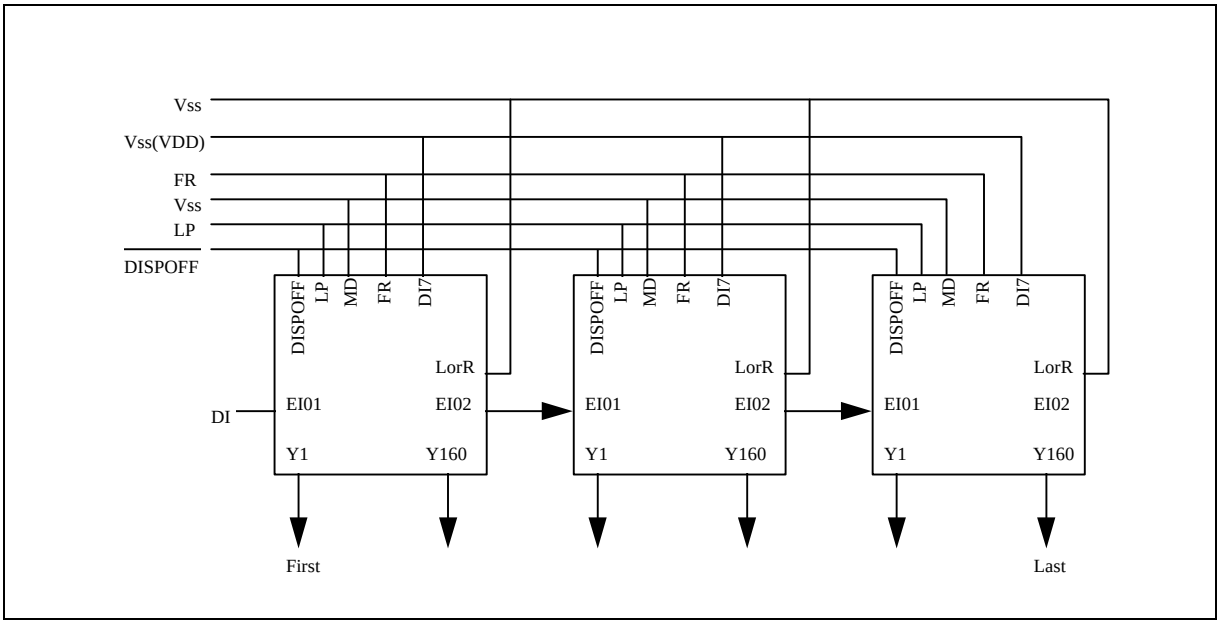
Note: n: 4-bit parallel mode 40
8-bit parallel mode 20

6.2.4 Connection Examples of Plural Common Drivers

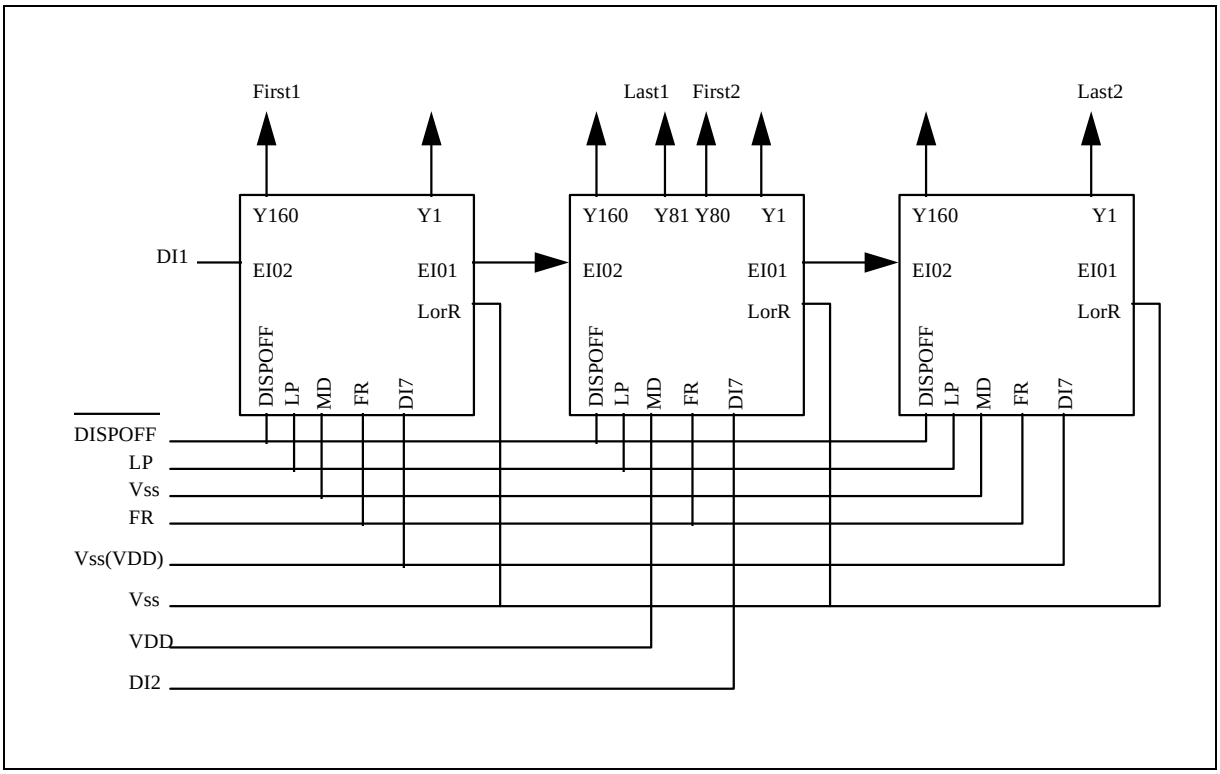
(1) Single Mode (Shifting toward left)



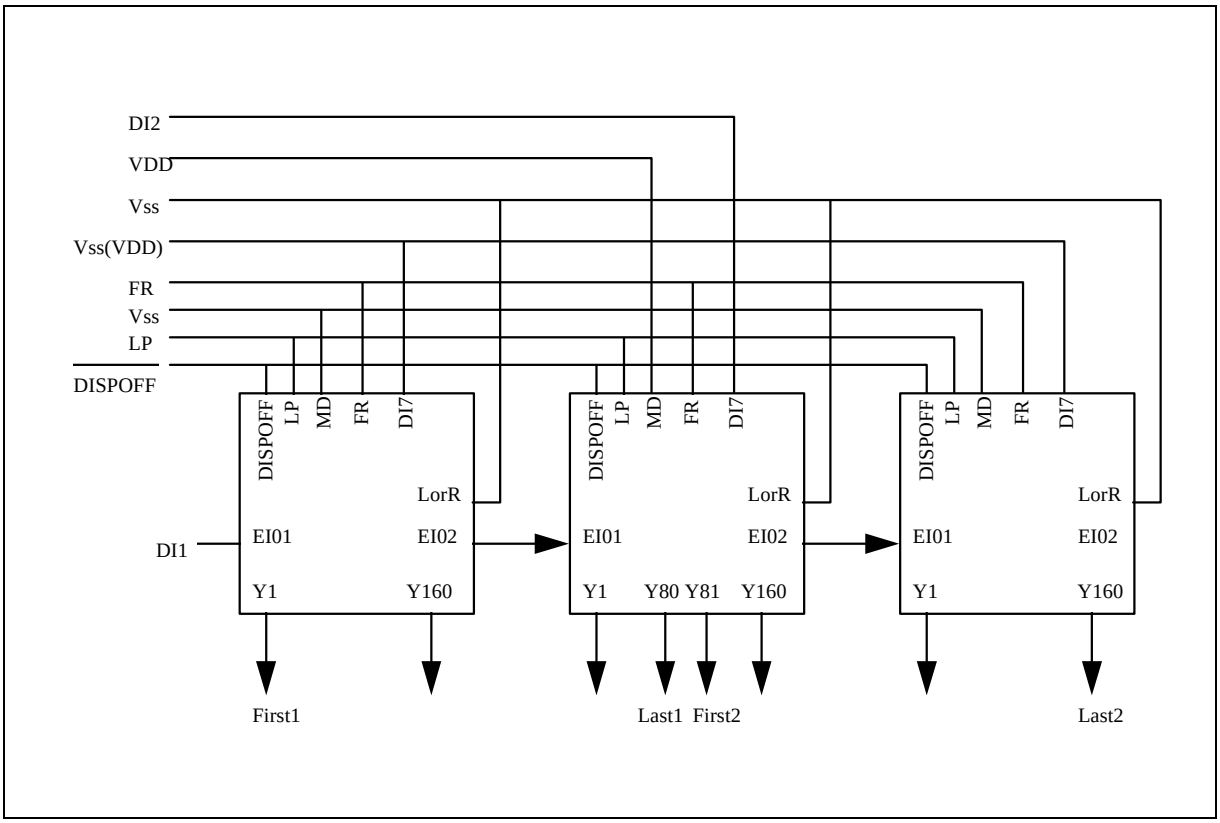
(2) Single Mode (Shifting toward right)



(3) Dual Mode (Shifting toward left)



(4) Dual Mode (Shifting toward right)



7. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Logical Circuit Voltage	V_{DD}	-0.3 to +7.0	V	
LCD drive Circuit Voltage	V0	-0.3 to +32	V	
Input Logic Voltage	V12	-0.3 to V0+0.3	V	
Input Drive Voltage	V43	-0.3 to V0+0.3	V	
Input logic Voltage	V43	-0.3 to V_{DD} +0.3	V	
Storage Temperature	T_{STG}	-45 to +125	°C	

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. RECOMMENDED OPERATING CONDITIONS

PARAMETR	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (1)	VDD	+2.5		+5.5	V
Supply Voltage (2)	V0	+10		+30	V
Operating Temperature	TOPT	0		+70	°C

Note: Ensure that voltage Vss < V43 < V12 < V0

9. ELECTRICAL CHARACTERISTICS

9.1 DC Characteristics

VDD = 2.5V to 5.5V, V0 = +10V to 30V; TA = 0 to 70° C

(Segment Mode)

PARAMETER	SYM.	APPLICABLE PIN	MIN.	TYP.	MAX.	UNIT	CONDITION	NOTES
Input Voltage	VIH	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF	0.8 VDD			V		
Input Voltage	VIL	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			0.2 VDD	V		
Output Voltage	VOH	EIO1, EIO2	VDD -0.4			V	IOH = -0.4 mA	
Output Voltage	VOL	EIO1, EIO2			+0.4	V	IOL = 0.4 mA	
Input Leagake Current	ILIH	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			+10	μA	VI = VDD	
Input Leakage Current	ILIL	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			-10	μA	VI = Vss	
Output Resistance	RON	Y1 ~ Y160		1.0	1.5	KΩ	Δon = 0.5V V0 = +30V	
Output Resistance	RON	Y1 ~ Y160		1.5	2.0	KΩ	Δon = 0.5V V0 = +20V	
Stand-by Current	ISTA	Vss			50	μA		1
Consumed Current (1) (deselect)	IDD1	VDD			2	mA		2
Consumed Current (2) (select)	IDD2	VDD			7	mA		3
Current Consumption	I0	V0			0.9	mA		4

Notes:
(1) VDD = +5.0V, V0 = +30V, VIH = VDD, VIL = Vss.
(2) VDD = +5.0V, V0 = +30V, Fxck = 8 MHz, No-load, EI = VDD.
The input data is turned over by data taking clock (4-bit parallel input mode)
(3) VDD = +5.0V, V0 = +30V, Fxck = 8 MHz, No-load, EI = Vss
The input data is turned over by data taking clock (4-bit parallel input mode)
(4) VDD = +5.0V, V0 = +30V, Fxck = 8 MHz, Flp = 19.2K, Ffr = 80 Hz, No-load
The input data is turned over by data taking clock (4-bit parallel input mode)

(Common Mode)

PARAMETER	SYM.	APPLICABLE PIN	MIN.	TYP.	MAX.	UNIT	CONDITION	NOTES
Input Voltage	V_{IH}	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF	0.8 V_{DD}			V		
Input Voltage	V_{IL}	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			0.2 V_{DD}	V		
Output Voltage	V_{OH}	EIO1, EIO2	V_{DD} -0.4			V	I_{OH} = -0.4 mA	
Output Voltage	V_{OL}	EIO1, EIO2			+0.4	V	I_{OL} = 0.4 mA	
Input Leagake Current	I_{LIH}	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			+10	µA	VI = V_{DD}	
Input Leakage Current	I_{LIL}	DI0~DI7, XCK, LP, LorR, FR, MD, EI01, EI02, DISPOFF			-10	µA	VI = Vss	
Input Pull-down Current	P_{DL}	DI7, XCK, EI01, EI02			100	µA	VI = V_{DD}	
Output Resistance	R_{ON}	Y1 ~ Y160		1.0	1.5	KΩ	Δon = 0.5V V0 =+30V	
Output Resistance	R_{ON}	Y1 ~ Y160		1.5	2.0	KΩ	Δon = 0.5V V0 =+20V	
Stand-by Current	I_{STA}	Vss			50	µA		1
Consumed Current (1) (deselect)	I_{DD}	V_{DD}			80	µA		2
Current Consumption	I0	V0			130	µA		2

Notes:

(1) V_{DD} = +5.0V, V0 = +30V, Vi = Vss

(2) V_{DD} = +5.0V, V0 = +30V, Flp = 19.2 KHz, Ffr = 80 Hz
case 0f 1/240 duty operation, No-load

9.2 AC Characteristics

(Segment Mode)

V_{SS} = 0, V_{DD} = +2.5 ~ +5.5V, V0 = +10V ~ +30V, T_A = 0 to 70°C

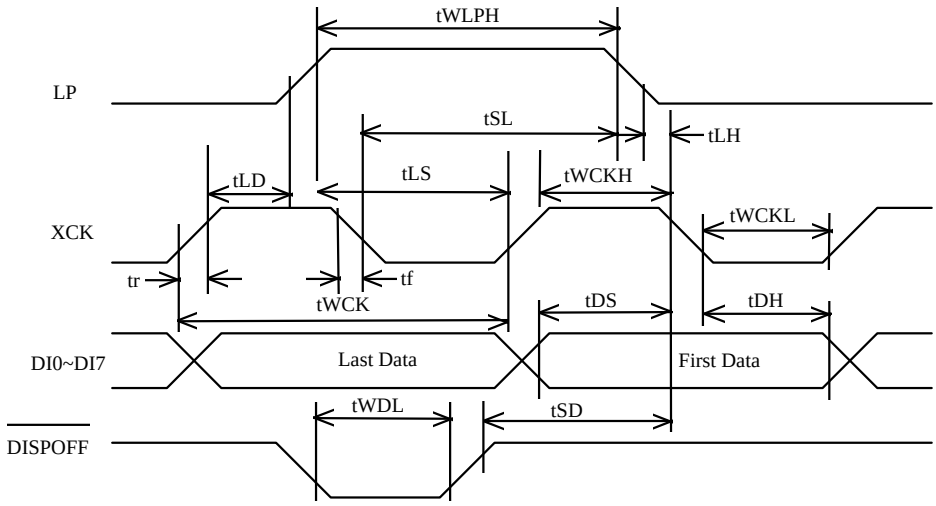
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Shift Clock Period *1	twck	Tr, Tf <= 11 nS	125		nS
Shift Clock “H” Pulse Width	twckH		51		nS
Shift Clock “L” Pulse Width	twckL		51		nS
Data Setup Time	tDS		30		nS
Data Hold Time	tDH		40		nS
Latch Pulse “H” Pulse Width	tWLPH		51		nS
Shift Clock Rise to Latch Pulse Rise Time	tLD		0		nS
Shift Clock fall to Latch Pulse Fall Time	tSL		51		nS
Latch Pulse Rise to Shift Clock Rise Time	tLS		51		nS
Latch Pulse Fall to Shift Clock Fall Time	tLH		51		nS
Input Signal Rise Time *2	tr			50	nS
Input Signal Fall Time *2	tf			50	nS
Enable Setup Time	tS		36		nS
DISPLAYOFF Removal Time	tSD		100		nS
DISPOFF “L” Pulse Width	tWDL		1.2		µS
Output Delay Time (1)	tD	CL = 15 pF		78	nS
Output Delay Time (2)	tpd1, tpd2	CL = 15 pF		1.2	µS
Output Delay Time (3)	tpd3	CL = 15 pF		1.2	µS

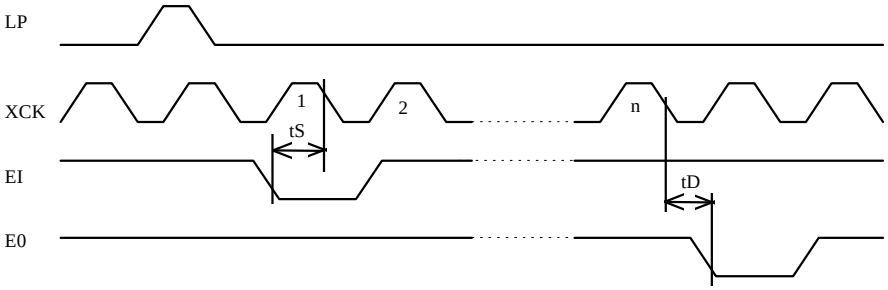
Notes:

(1) Take the cascade connection into consideration.

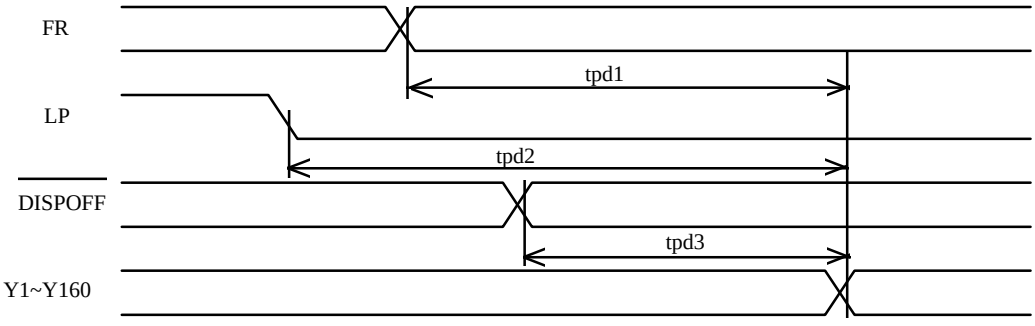
(2) (twck-twckH-twckL)/2 is maximum in the case of high speed operation

(Timing Characteristics of Segment Mode)





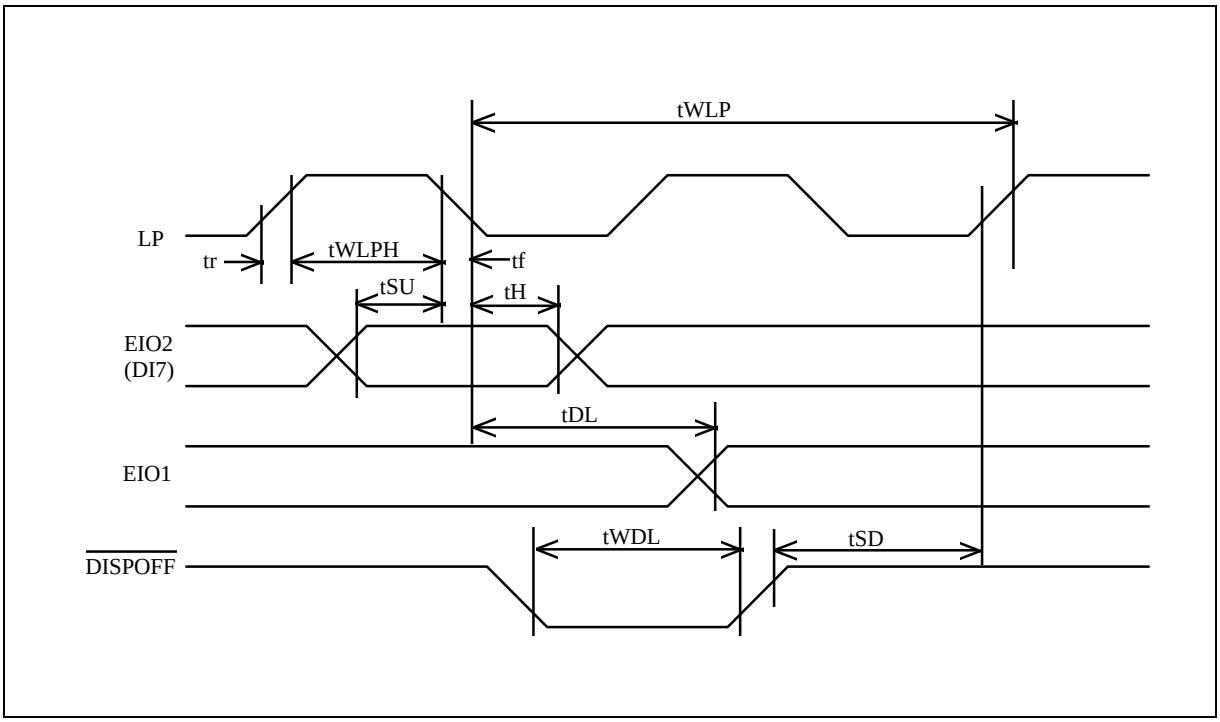
Note: n: 4-bit parallel mode 40
8-bit parallel mode 20

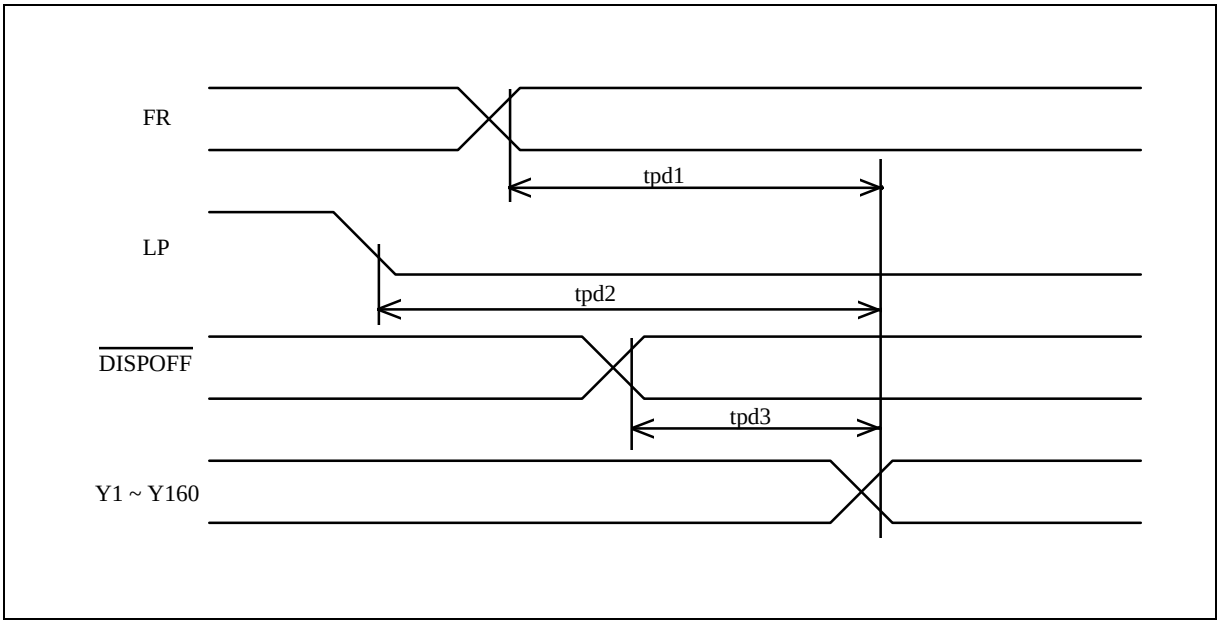


(Common Mode)

Vss = 0, V_{DD} = +2.5 ~ +5.5V, V0 = +10V ~ +30V, T_A = 0 to 70°C

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Shift Clock Period *1	twlp	Tr, Tf <= 20 nS	250		nS
Shift Clock "H" Pulse Width	twlpH	V_{DD} = +5.0V (+- 10%)	15		nS
Shift Clock "H" Pulse Width	twlpH	V_{DD} = +2.5V ~ +4.5V	30		nS
Data Setup Time	tSU		30		nS
Data Hold Time	tH		50		nS
Input Signal Rise Time	tr			50	nS
Input Signal Fall Time	tf			50	nS
DISPLAYOFF Removal Time	tSD		100		nS
DISPOFF "L" Pulse Width	tWDL		1.2		µS
Output Delay Time (1)	tD	CL = 15 pF		200	nS
Output Delay Time (2)	tpd1, tpd2	CL = 15 pF		1.2	µS
Output Delay Time (3)	tpd3	CL = 15 pF		1.2	µS





Note: LorR = "L"

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