512Kx32 SRAM / FLASH MODULE

*PRELIMINARY**

FEATURES

- Access Times of 25ns (SRAM) and 70, 90ns (FLASH)
- Packaging
  - 66 pin, PGA Type, 1.385" square HIP, Hermetic Ceramic HIP (Package 402)
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2). Package to be developed.
- 512Kx32 SRAM
- 512Kx32 5V Flash
- Organized as 512Kx32 of SRAM and 512Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

FLASH MEMORY FEATURES

- 100,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WSF512K32-XH2X

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{FWE_2}$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{SWE_2}$	I/O14	I/O25	$\overline{SWE_4}$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{FWE_4}$	I/O29
A14	I/O11	I/O12	A7	I/O27	I/O28
A16	A10	$\overline{OE}$	A12	A4	A1
A11	A9	A17	$\overline{SWE_1}$	A5	A2
A0	A15	$\overline{FWE_1}$	A13	A6	A3
A18	VCC	I/O7	A8	$\overline{FWE_3}$	I/O23
I/O0	$\overline{FCS}$	I/O6	I/O16	$\overline{SWE_3}$	I/O22
I/O1	$\overline{SCS}$	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{SWE}_{1-4}$	SRAM Write Enables
$\overline{SCS}$	SRAM Chip Select
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected
$\overline{FWE}_{1-4}$	Flash Write Enables
$\overline{FCS}$	Flash Chip Select

BLOCK DIAGRAM

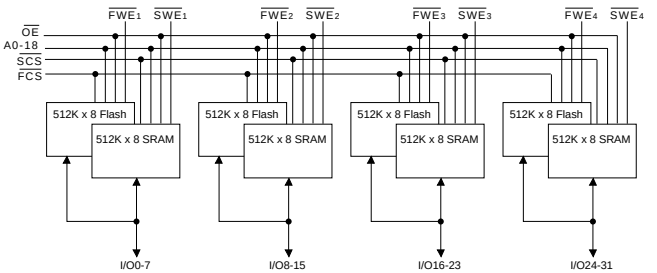
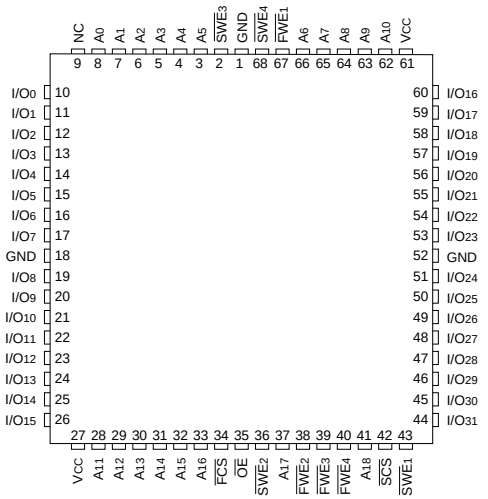
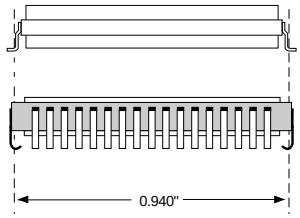


FIG. 2 PIN CONFIGURATION FOR WSF512K32-XG2TX

TOP VIEW



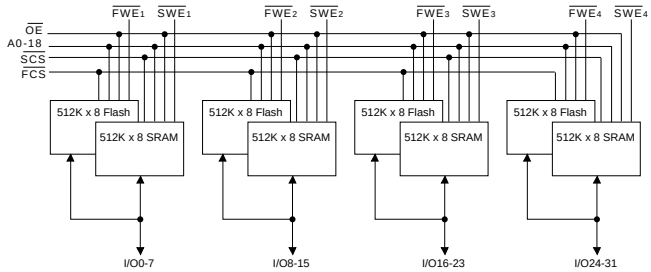


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{SWE}_{1-4}$	SRAM Write Enables
$\overline{SCS}$	SRAM Chip Select
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected
$\overline{FWE}_{1-4}$	Flash Write Enables
$\overline{FCS}$	Flash Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	7.0	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

NOTE:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

SRAM TRUTH TABLE

$\overline{SCS}$	$\overline{OE}$	$\overline{SWE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

NOTE:
1. $\overline{FCS}$ must remain high when $\overline{SCS}$ is low.

CAPACITANCE

(T_A = +25°C)

Test	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	80	pF
F/S $\overline{WE}_{1-4}$ Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	30	pF
F/S $\overline{CS}$ Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	50	pF
D_{0-31} Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	30	pF
A_{0-18} Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	80	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
SRAM Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{SCS}$ = V_{IL}, $\overline{OE}$ = $\overline{FCS}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		550	mA
Standby Current	I_{SB}	$\overline{FCS}$ = $\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		90	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V
Flash V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{FCS}$ = V_{IL}, $\overline{OE}$ = $\overline{SCS}$ = V_{IH}		250	mA
Flash V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCS}$ = V_{IL}, $\overline{OE}$ = $\overline{SCS}$ = V_{IH}		300	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 12.0mA, V_{CC} = 4.5		0.45	V
Flash Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Flash Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} -0.4		V
Flash Low V_{CC} Lock Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC CHARACTERISTICS

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25 Min	 Max	Unit
Read Cycle Time	tRC	25		ns
Address Access Time	tAA		25	ns
Output Hold from Address Change	tOH	0		ns
Chip Select Access Time	tACS		25	ns
Output Enable to Output Valid	tOE		15	ns
Chip Select to Output in Low Z	tCLZ[1]	3		ns
Output Enable to Output in Low Z	tOLZ[1]	0		ns
Chip Disable to Output in High Z	tCHZ[1]		12	ns
Output Disable to Output in High Z	tOHZ[1]		12	ns

1. This parameter is guaranteed by design but not tested.

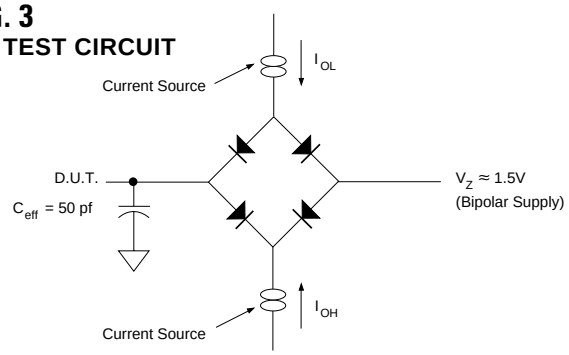
SRAM AC CHARACTERISTICS

(VCC = 5.0V, TA = -55°C to +125°C)

Parameter Write Cycle	Symbol	-25 Min	 Max	Unit
Write Cycle Time	tWC	25		ns
Chip Select to End of Write	tCW	20		ns
Address Valid to End of Write	tAW	20		ns
Data Valid to End of Write	tDW	15		ns
Write Pulse Width	tWP	20		ns
Address Setup Time	tAS	0		ns
Address Hold Time	tAH	0		ns
Output Active from End of Write	tOW[1]	3		ns
Write Enable to Output in High Z	tWHZ[1]		15	ns
Data Hold from Write Time	tDH	0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

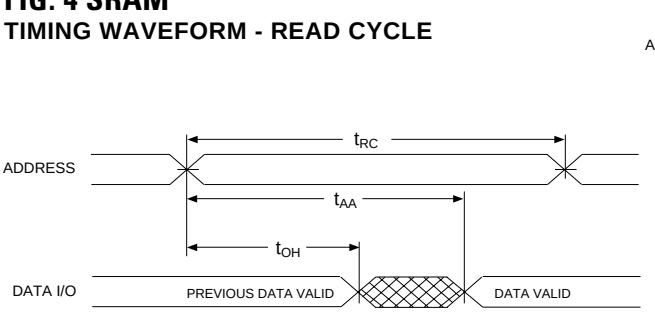


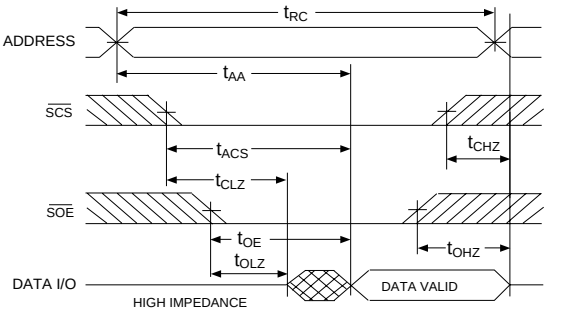
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	VIL = 0, VIH = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75\ \Omega$.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

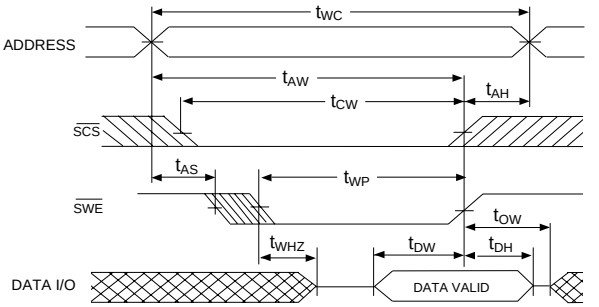
FIG. 4 SRAM
TIMING WAVEFORM - READ CYCLE





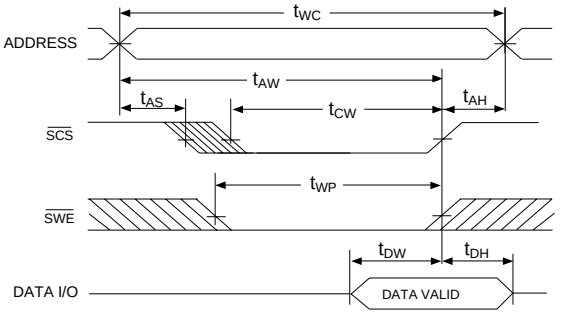
READ CYCLE 1, ($\overline{SCS}$ = $\overline{OE}$ = V_{IL}, $\overline{SWE}$ = $\overline{FCS}$ = V_{IH})

FIG. 5 SRAM
WRITE CYCLE - $\overline{SWE}$ CONTROLLED



WRITE CYCLE 1, $\overline{SWE}$ CONTROLLED ($\overline{FCS}$ = V_{IH})

FIG. 6 SRAM
WRITE CYCLE - $\overline{SCS}$ CONTROLLED



WRITE CYCLE 2, $\overline{SCS}$ CONTROLLED ($\overline{FCS}$ = V_{IH})

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{FWE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		45		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		45		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300	µs
Chip and Sector Erase Time (2)	t_{WHWH2}			15		15	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		µs
V_{CC} Set-up Time		t_{VCS}	50		50		µs
Chip Programming Time				11		11	sec
Output Enable Setup Time		t_{OES}	0		0		ns
Output Enable Hold Time (4)		t_{OEH}	10		10		ns
Chip Erase Time (3)				64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7ns.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and $\overline{Data}$ Polling.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		90		ns
Address Access Time	t_{AVQV}	t_{ACC}		70		90	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		70		90	ns
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		35		35	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20	ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20	ns
Output Hold from Address, $\overline{FCS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		ns

1. Guaranteed by design, not tested.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{FCS}$ CONTROLLED

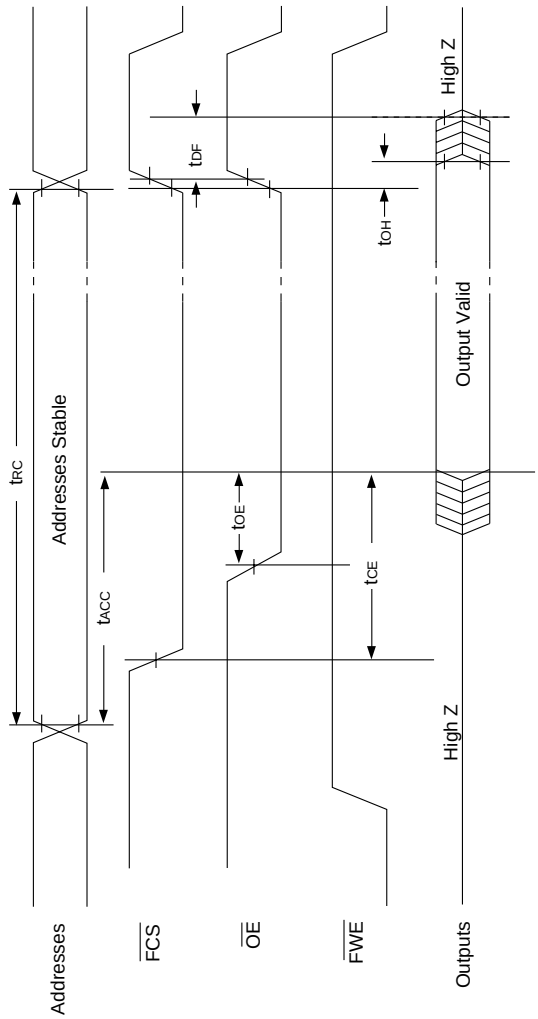
(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		ns
$\overline{FWE}$ Setup Time	t_{WLEL}	t_{WS}	0		0		ns
$\overline{FCS}$ Pulse Width	t_{ELEH}	t_{CP}	45		45		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		45		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		ns
$\overline{FCS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		20		ns
Duration of Programming Operation (1)	t_{WHWH1}			300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15	sec
Read Recovery Time	t_{GHEL}		0		0		ns
Chip Programming Time				11			sec
Chip Erase Time (3)				64			sec

NOTES:

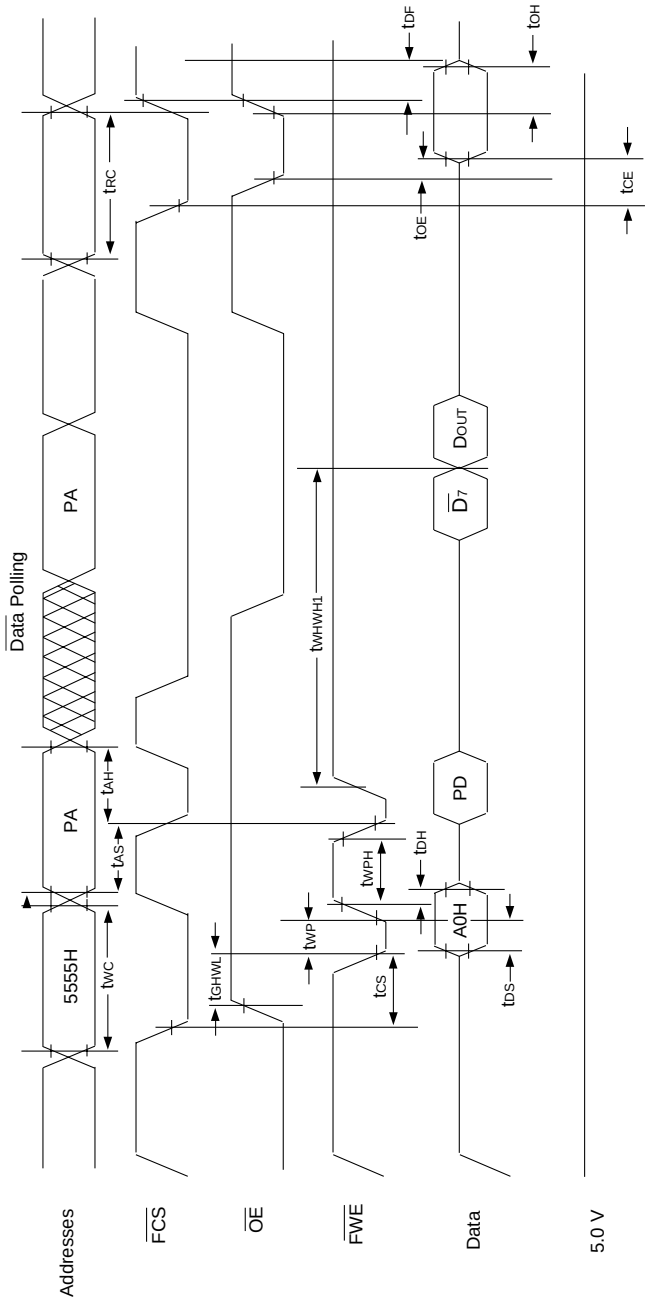
1. Typical value for t_{WHWH1} is 7ns.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIG. 7
AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS



NOTE: $\overline{SCS}$ = V_{IH}

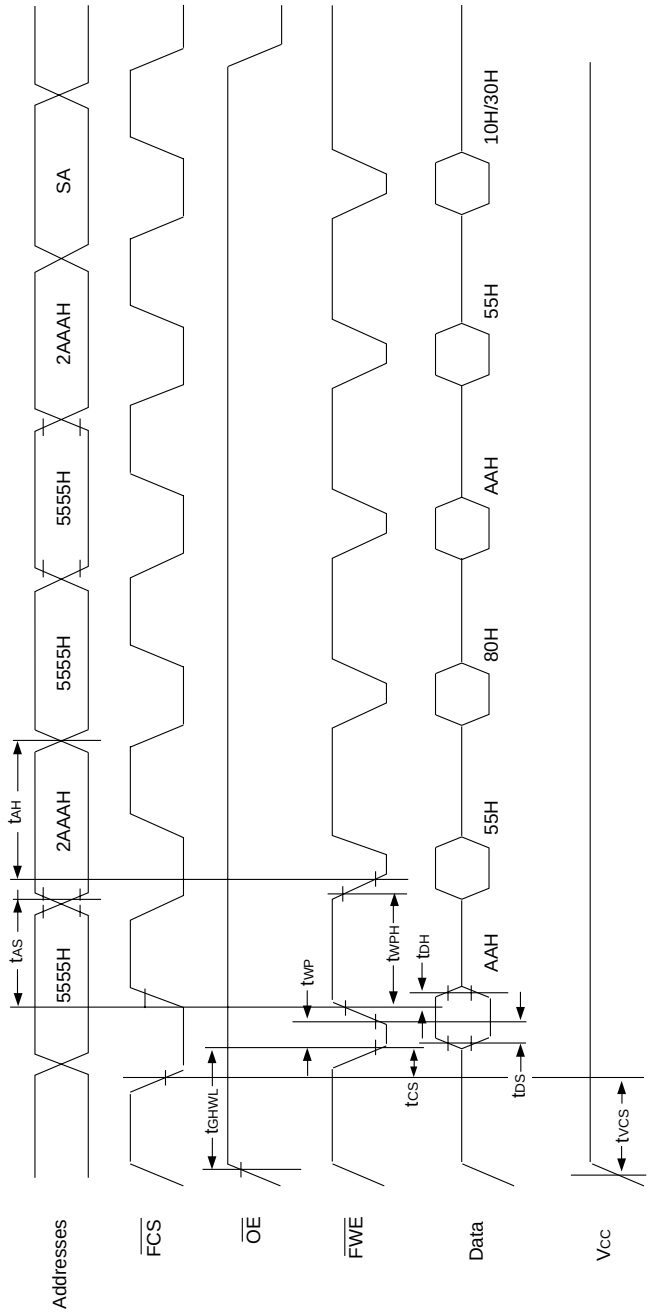
FIG. 8
WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY $\overline{FWE}$ CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. $\overline{SCS}$ = VIH

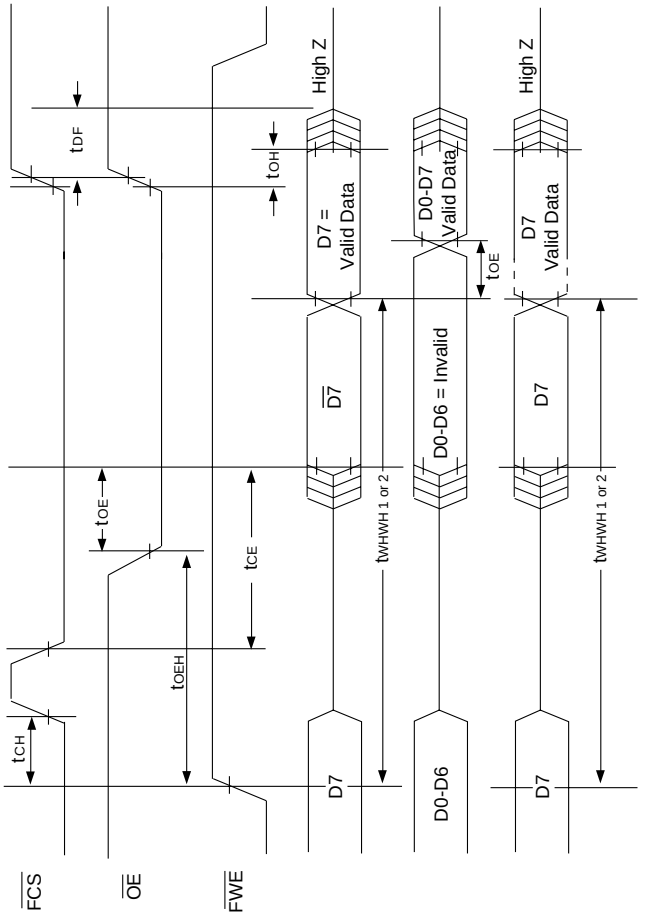
FIG. 9
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



NOTES:

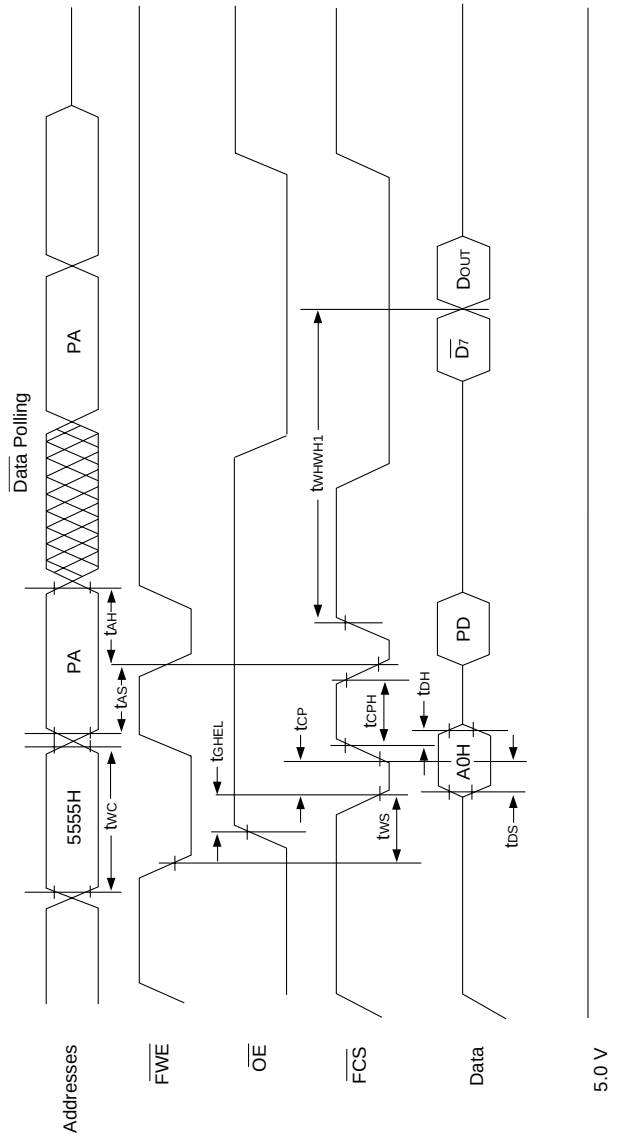
1. SA is the sector address for Sector Erase.
2. $\overline{SCS}$ = V_{IH}

FIG. 10
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY



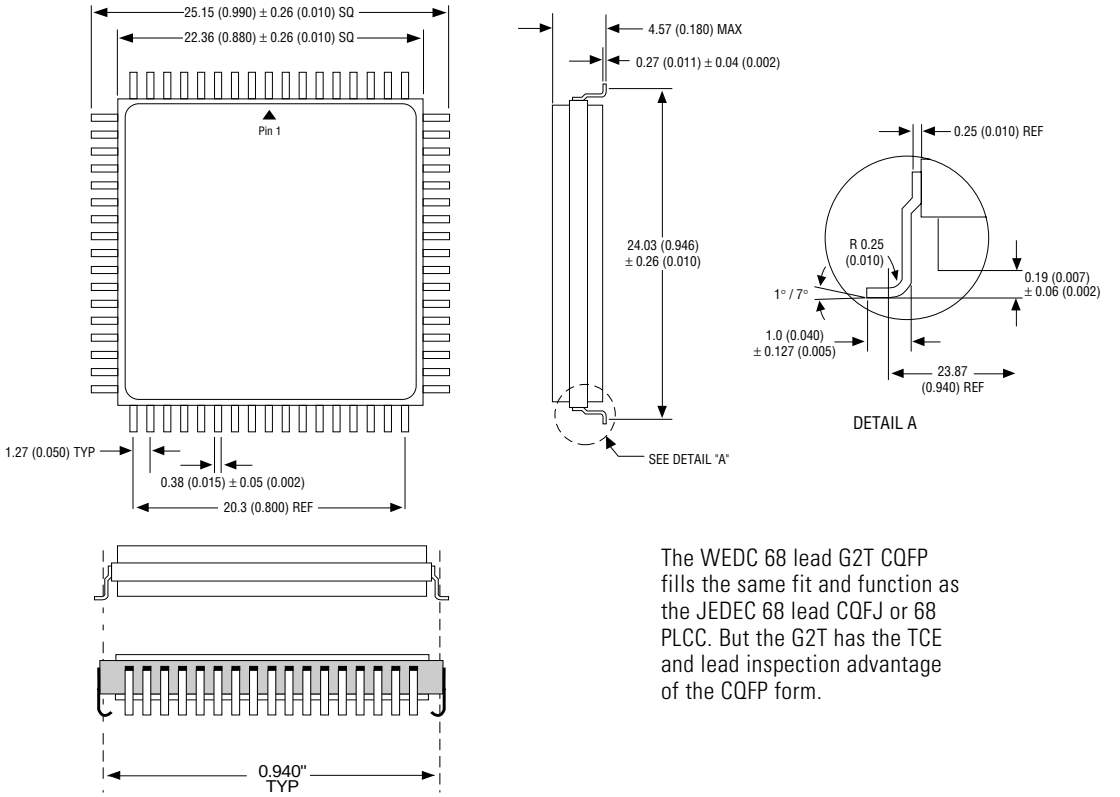
NOTE: $\overline{\text{SCS}}$ = V_{IH}

FIG. 11
WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, $\overline{CS}$ CONTROLLED



NOTES:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.
6. $\overline{SCS}$ = VIH

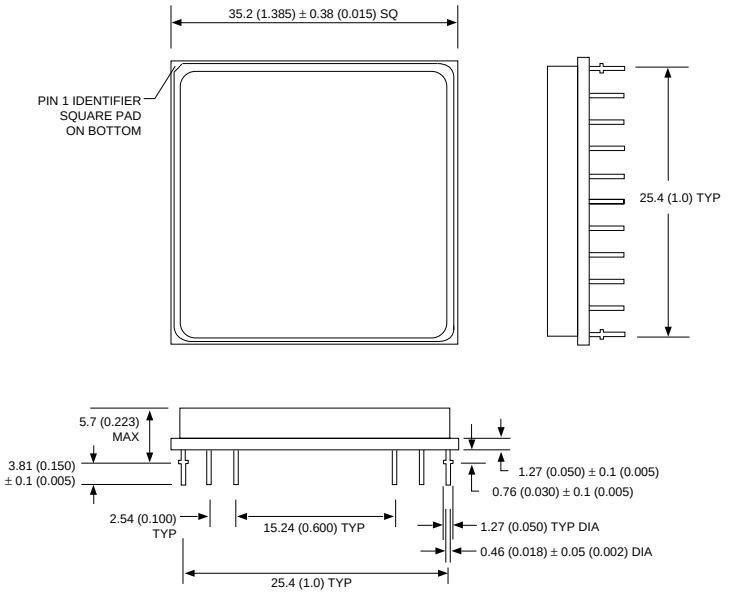
PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S F 512K32 - XX X X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:

M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

PACKAGE TYPE:
H2 = Ceramic Hex In-line Package, HIP (Package 402)
G2T = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 509)

ACCESS TIME (ns)
29 = 25ns SRAM and 90ns FLASH
27 = 25ns SRAM and 70ns FLASH

ORGANIZATION, 512K x 32 SRAM and Flash

Flash

SRAM

WHITE ELECTRONIC DESIGNS CORP.