32Kx32 EEPROM MODULE, SMD 5962-94614

FEATURES

- Access Times of 90, 120, 150ns
- MIL-STD-883 Compliant Devices Available
- Packaging:
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880 inch) square, 3.56mm (0.140 inch) height (Package 510). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
- Data Retention at 25°C, 10 Years
- Write Endurance, 10,000 Cycles
- Organized as 32Kx32; User Configurable 64Kx16 or 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS, 10mA Standby Typical
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

FIG. 1 PIN CONFIGURATION FOR WE32K32N-XH1X

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
NC	A11	NC	NC	A4	A1
NC	A12	$\overline{WE}_1$	A8	A5	A2
NC	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-14	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

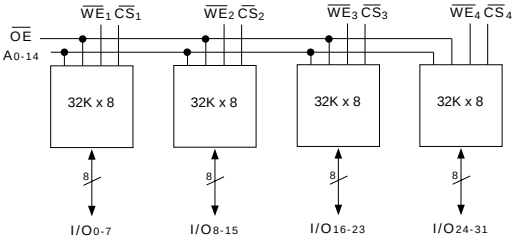
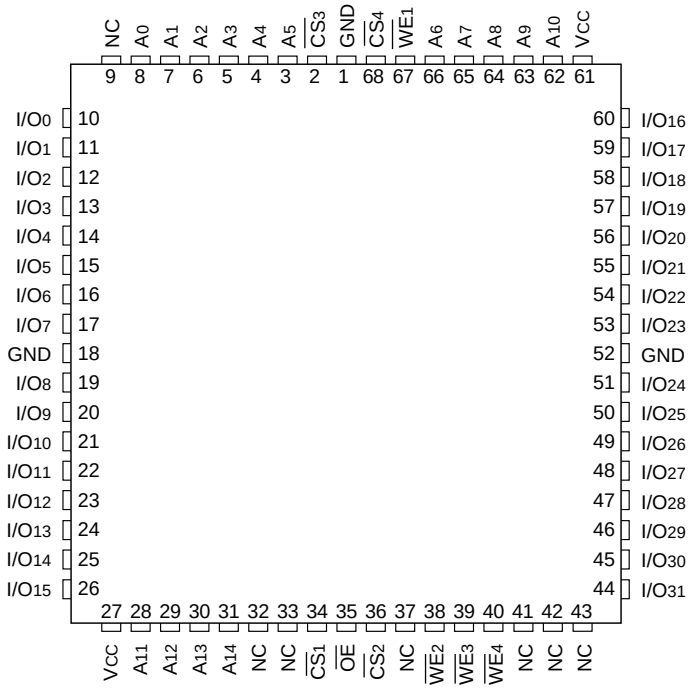


FIG. 2 PIN CONFIGURATION FOR WE32K32-XG2UX

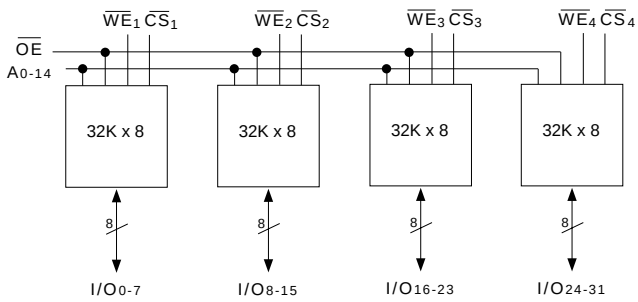
TOP VIEW

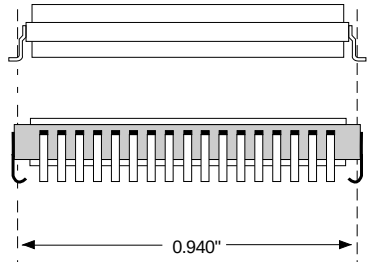


PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-14}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM





The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to +6.25	V
Voltage on $\overline{OE}$ and A9		-0.6 to +13.5	V

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

(T_A = 25° C)

Parameter	Symbol	Condition	Max	Unit
Address Input Capacitance $\overline{OE}$ Capacitance	C_{AD} C_{OE}	V_{IN} = 0V, f = 1.0MHz	50	pF
$\overline{CS}_{1-4}$ Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
$\overline{WE}_{1-4}$ Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

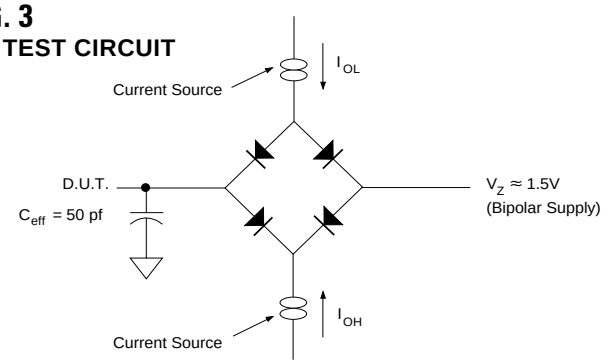
DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-90		-120		-150		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	$I_{LO\ x\ 32}$	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current x 32 Mode	$I_{CC\ x\ 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		250		200		150	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		2.5		2.5		2.5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5V		0.45		0.45		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 3
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{WE}$ or $\overline{CS}$ with $\overline{CS}$ or $\overline{WE}$ low. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

WRITE CYCLE		-90		-120		-150		
Write Cycle Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write Cycle Time, TYP = 6ms	t_{WC}		10		10		10	ms
Address Set-up Time	t_{AS}	0		30		30		ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	100		150		150		ns
Chip Select Set-up Time	t_{CS}	0		0		0		ns
Address Hold Time	t_{AH}	50		100		100		ns
Data Hold Time	t_{DH}	0		10		10		ns
Chip Select Hold Time	t_{CSH}	0		0		0		ns
Data Set-up Time	t_{DS}	50		100		100		ns
Write Pulse Width High	t_{WPH}	50		50		50		ns
Output Enable Set-up Time	t_{OES}	10		10		10		ns
Output Enable Hold Time	t_{OEH}	10		10		10		ns

FIG. 4
WRITE WAVEFORMS
WE CONTROLLED

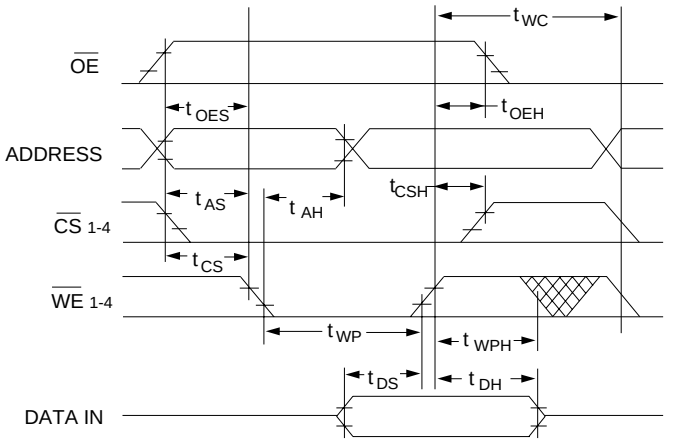
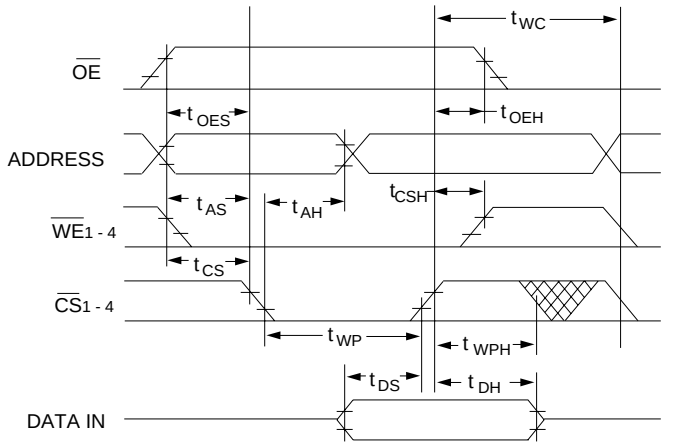


FIG. 5
WRITE WAVEFORMS
CS CONTROLLED



READ

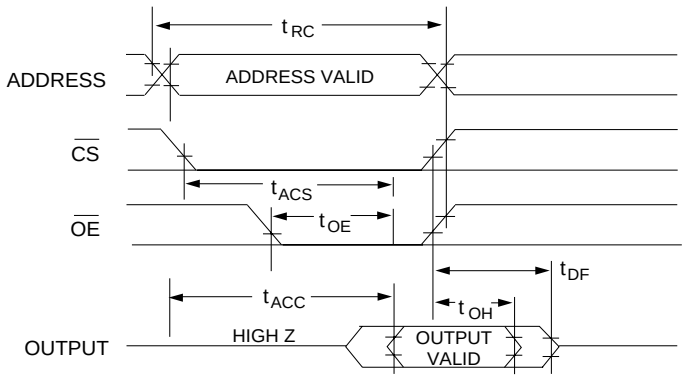
The WE32K32-XHX stores data at the memory location determined by the address pins. When $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This 2 line control prevents bus contention.

AC READ CHARACTERISTICS (See Figure 6)

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

READ CYCLE Parameter	Symbol	-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		150		ns
Address Access Time	t_{ACC}		90		120		150	ns
$\overline{CS}$ Access Time	t_{ACS}		90		120		150	ns
Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	0		0		0		ns
Output Enable to Output Valid	t_{OE}		50		85		85	ns
Chip Select or OE to Output in High Z	t_{DF}		50		70		70	ns

FIG. 6
READ WAVEFORMS



NOTES:
1. $\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
2. t_{CHZ}, t_{OHZ} are specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5pF).
3. All I/O transitions are measured ±200 mV from steady state with loading as specified in "Load Test Circuits."

DATA POLLING

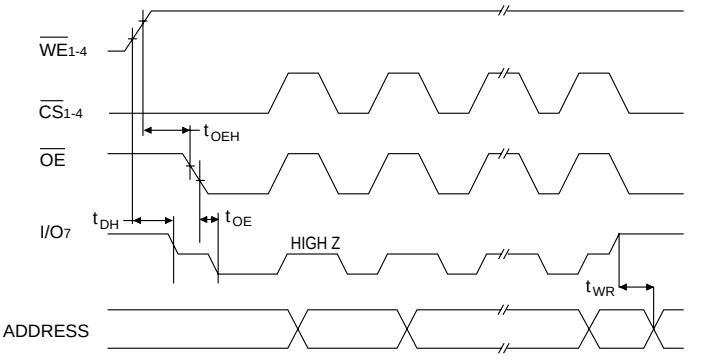
The WE32K32-XXX offers a data polling feature which allows a faster method of writing to the device. Figure 7 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D_7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t_{DH}	10		ns
$\overline{OE}$ Hold Time	t_{OEH}	10		ns
$\overline{OE}$ To Output Valid	t_{OE}		100	ns
Write Recovery Time	t_{WR}	0		ns

FIG. 7
DATA POLLING WAVEFORMS



PAGE WRITE OPERATION

The WE32K32-XXX has a page write operation that allows one to 64 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A5 at each write cycle. In this manner a page of up to 64 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

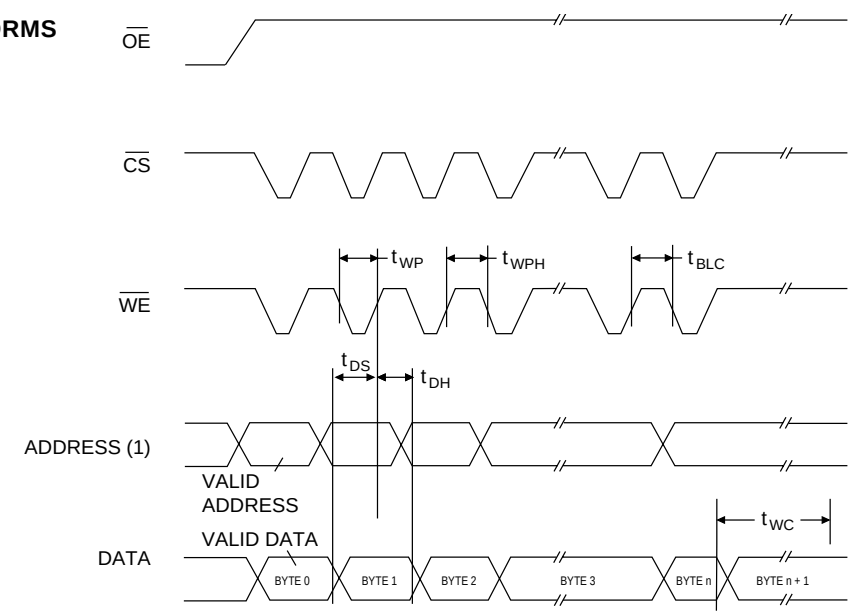
After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

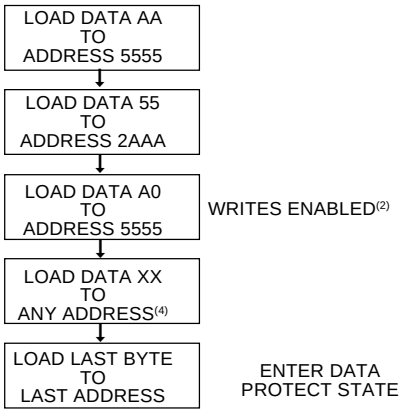
PAGE MODE WRITE CHARACTERISTICS Parameter	Symbol	-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6ms	t_{WC}		10		10		10	ms
Data Set-up Time	t_{DS}	50		100		100		ns
Data Hold Time	t_{DH}	0		10		10		ns
Write Pulse Width	t_{WP}	100		150		150		ns
Byte Load Cycle Time	t_{BLC}		150		150		150	µs
Write Pulse Width High	t_{WPH}	50		50		50		ns

FIG. 8
PAGE WRITE WAVEFORMS



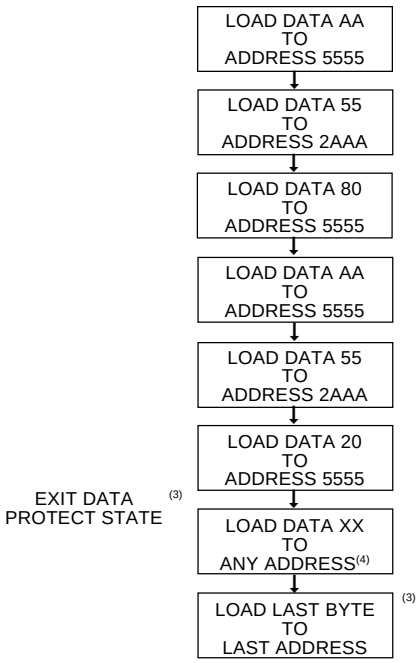
NOTE:
1. Decoded Address Lines must be valid for the duration of the write.

FIG. 9
SOFTWARE BLOCK DATA PROTECTION ENABLE ALGORITHM(1)



NOTES:
1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{14} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.

FIG. 10
SOFTWARE BLOCK DATA PROTECTION DISABLE ALGORITHM(1)



NOTES:
1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{14} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WE32K32-XXX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of t_{WC}. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 32KByte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WE32K32-XXX. These are included to improve reliability during normal operation:

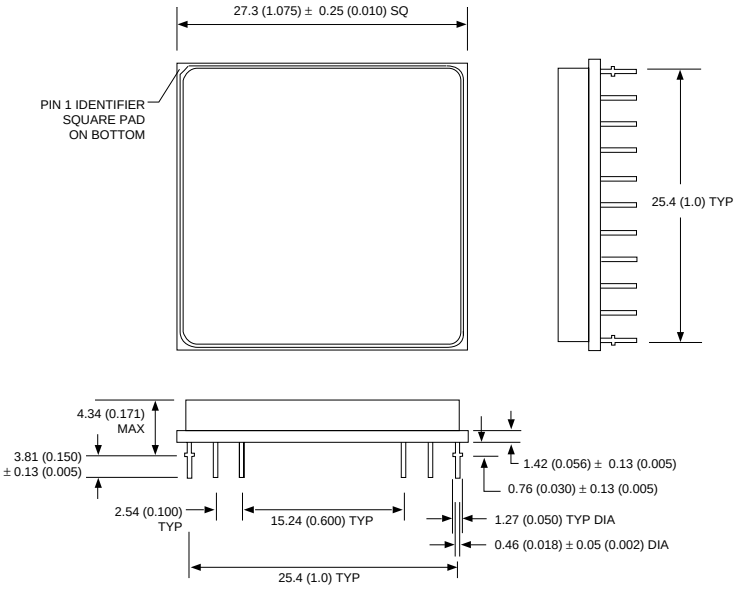
a) V_{CC} power on delay
As V_{CC} climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.

b) V_{CC} sense
While below 3.8V typical write cycles are inhibited.

c) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

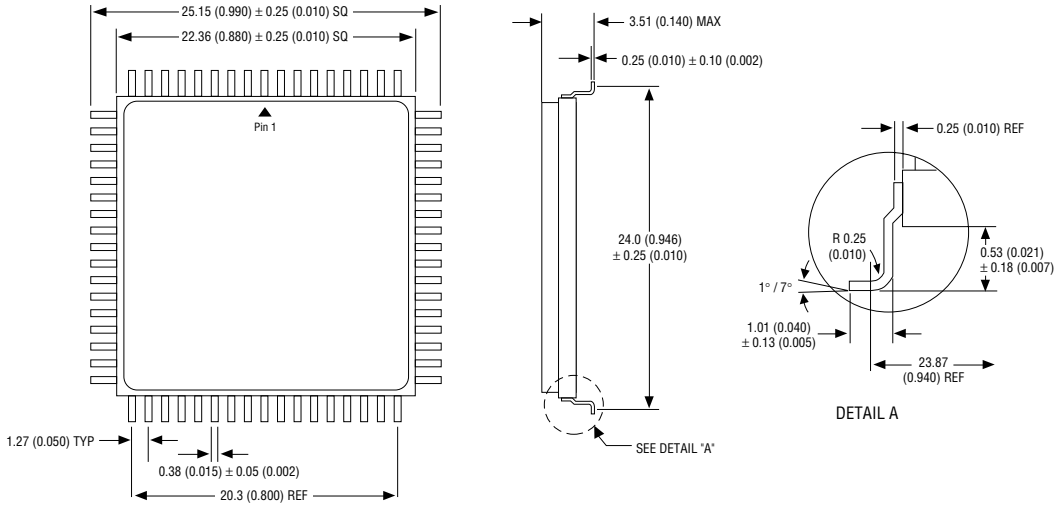
d) Noise filter
Pulses of <8ns (typ) on $\overline{WE}$ or $\overline{CS}$ will not initiate a write cycle.

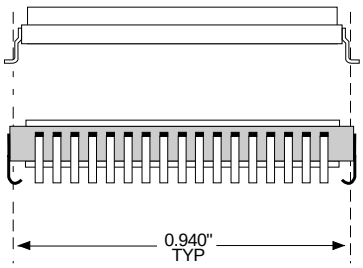
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)





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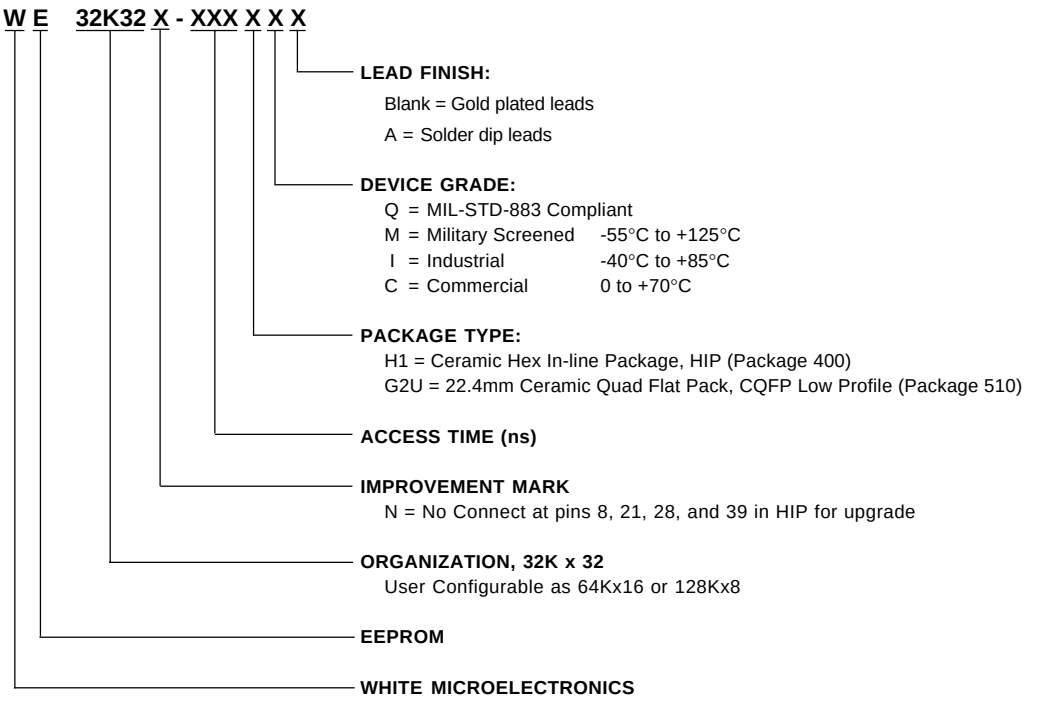
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
32K x 32 EEPROM Module	150ns	66 pin HIP (H1)	5962-94614 01HXX
32K x 32 EEPROM Module	120ns	66 pin HIP (H1)	5962-94614 02HXX
32K x 32 EEPROM Module	90ns	66 pin HIP (H1)	5962-94614 03HXX
32K x 32 EEPROM Module	150ns	68 lead CQFP/J (G2U)	5962-94614 01HZX
32K x 32 EEPROM Module	120ns	68 lead CQFP/J (G2U)	5962-94614 02HZX
32K x 32 EEPROM Module	90ns	68 lead CQFP/J (G2U)	5962-94614 03HZX