RISC 603e Monolithic MICROPROCESSOR

*PRELIMINARY**

The WEDMC64603R-XXX is part of a family of reduced instruction set computing (RISC) microprocessors which is offered by WEDC at extended temperature ranges. The WEDMC64603R-XXX is offered in both the Industrial (-40°C to +85°C) and Military (-55°C to +125°C) temperature ranges.

Available in a ceramic 255 Pin Ball Grid Array (CBGA) and a 255 Pin Ceramic Column Grid Array (CCGA) package, the WEDMC64603R-XXX is well suited for embedded applications such as missile, aerospace, flight computers, fire control and other rugged critical systems.

The processor can issue an d retire three instructions per clock cycle into five independent execution units. The processor has a 2.5 volt core voltage and a 3.3 volt I/O voltage along with an independent 16-Kbyte instruction and data caches.

OVERVIEW

The WEDMC64603R-XXX is a low-power implementation of the PowerPC™ microprocessor family of reduced instruction set computing (RISC) microprocessors. The WEDMC64603R-XXX implements the 32-bit portion of the PowerPC architecture specification, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating- point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The WEDMC64603R-XXX provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the WEDMC64603R-XXX to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The WEDMC64603R-XXX is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the WEDMC64603R-XXX makes completion appear sequential.

The WEDMC64603R-XXX integrates five execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603e-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The WEDMC64603R-XXX provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least-recently used (LRU) replacement algorithm. The WEDMC64603R-XXX also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The WEDMC64603R-XXX has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The WEDMC64603R-XXX provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The WEDMC64603R-XXX uses an advanced, 2.5/3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

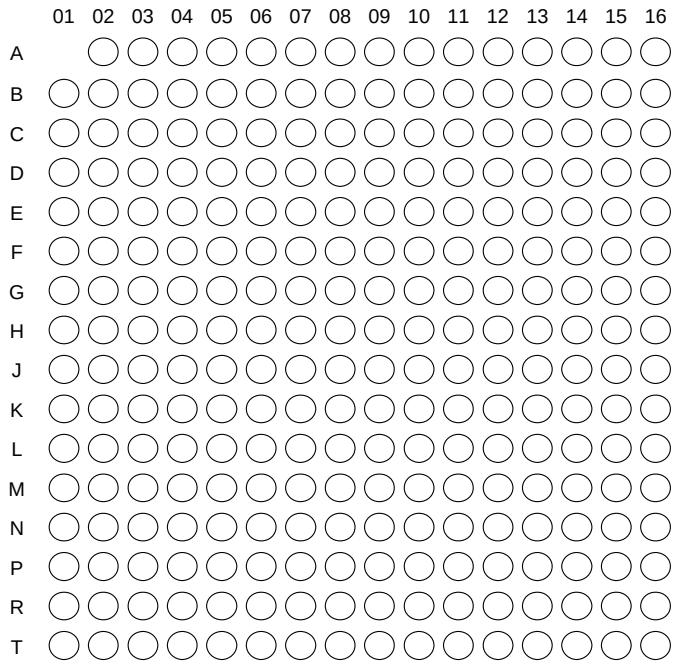
FEATURES

- High-performance, superscalar microprocessor
  - As many as three instructions issued and retired per clock
  - As many as five instructions in execution per clock
  - Single-cycle execution for most instructions
  - Pipelined FPU for all single-precision and most double-precision operations
- Five independent execution units and two register files
  - BPU featuring static branch prediction
  - A 32-bit IU
  - Fully IEEE 754-compliant FPU for both single- and double-precision operations
  - LSU for data transfer between data cache and GPRs and FPRs
  - SRU that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
  - Thirty-two GPRs for integer operands
  - Thirty-two FPRs for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16-Kbyte data cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - 16-Kbyte instruction cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 64-entry, two-way set-associative ITLB
  - A 64-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions
- Integrated power management
  - Low-power 2.5/3.3-volt design
  - Internal processor/bus clock multiplier that provides 2/1, 2.5/1, 3/1, 3.5/1, 4/1, 4.5/1, 5/1, 5.5/1, and 6/1 ratios
  - Three power saving modes: doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

FIG. 1 PINOUT OF THE WEDMC64603R-XXX, 255 CBGA PACKAGE AS VEIWED FROM THE TOP SURFACE

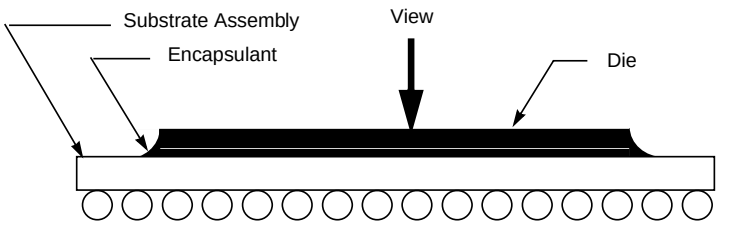
Part A shows the pinout of the 255 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Not to Scale

Part B



PINOUT LISTING

Signal Name	Pin Number	Active	I/O
A[0–31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0–3]	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE[0–1]	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0–31]	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0–31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0–7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK[1]	D11	—	Input
L2_TSTCLK[1]	D12	—	Input
LSSD_MODE[1]	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
NC (No-Connect)	B07, B08, C03, C06, C08, D05, D06, H04, J16	—	—
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0–3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
RSRV	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input

PINOUT LISTING (continued)

Signal Name	Pin Number	Active	I/O
$\overline{TA}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{TBST}$	A14	Low	I/O
TC[0–1]	A02, A03	High	Output
TCK	C11	—	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{TEA}$	H13	Low	Input
$\overline{TLBISYNC}$	C04	Low	Input
TMS	B11	High	Input
$\overline{TRST}$	C10	Low	Input
$\overline{TS}$	J13	Low	I/O
TSIZ[0–2]	A13, D10, B12	High	Output
TT[0–4]	B13, A15, B16, C14, C15	High	I/O
$\overline{WT}$	D02	Low	Output
VDD[2]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
VOLTDETGND[3]	F03	Low	Output

NOTES:

1. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
3. NC (No-Connect) in the PID6-603e internally tied to GND in PID7v-603e and PID7t-603e package to indicate to the power supply that a low-voltage processor is present.

ELECTRICAL AND THERMAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	-0.3	2.75	V
PLL supply voltage	AV_{DD}	-0.3	2.75	V
I/O supply voltage	OV_{DD}	-0.3	3.6	V
Input voltage	V_{IN}	-0.3	5.5	V
Storage temperature range	T_{STG}	-55	150	°C

NOTES:

1. Functional and tested operating conditions are given in Recommended Operating Conditions Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{IN} must not exceed OVdd by more than 0.3V at any time including during power-on reset.
3. **Caution:** OV_{DD} must not exceed Vdd/AVdd by more than 1.2V at any time including during power-on reset.
4. **Caution:** V_{DD}/AV_{DD} must not exceed OVdd by more than 0.4V at any time including during power-on reset.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	2.375	2.625	V
PLL supply voltage	AV_{DD}	2.375	2.625	V
I/O supply voltage	OV_{DD}	3.135	3.465	V
Input voltage	V_{IN}	GND	5.5	V
Die-junction temperature	T_J	0	105	°C

NOTE:

These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θJC	0.095	°C/W
CBGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θJB	3.5	°C/W

DC ELECTRICAL SPECIFICATIONS

(V_{DD} = AV_{DD} = 2.5V ±5%, OV_{DD} = 3.3V ±5%, GND = 0V)

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK) (1,2)	V_{IH}	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current, V_{IN} = 3.465V (1,2)	I_{IN}	—	30	µA
V_{IN} = 5.5V (1,2)	I_{IN}	—	300	µA
Hi-Z (off-state) leakage current, V_{IN} = 3.465V (1,2)	I_{TSI}	—	30	µA
V_{IN} = 5.5V (1,2)	I_{TSI}	—	300	µA
Output high voltage, I_{OH} = -7mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 7mA	V_{OL}	—	0.4	V
Capacitance, V_{IN} = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) (3)	C_{IN}	—	10.0	pF
Capacitance, V_{IN} = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) (3)	C_{IN}	—	15.0	pF

NOTES:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OVdd and Vdd vary by either ±5% or -5%).
3. Capacitance is periodically sampled rather than 100% tested.

POWER CONSUMPTION

	Processor (CPU) Frequency				
	200MHz	233MHz	266MHz	300MHz	Unit
Full-On Mode (DPM Enabled)					
Typical	2.5	3.0	3.5	4.0	W
Maximum	4.0	4.6	5.3	6.0	W
Doze Mode					
Typical	1.7	1.8	2.0	2.1	W
Nap Mode					
Typical	120	140	160	180	mW
Sleep Mode					
Typical	110	123	135	150	mW
Sleep Mode—PLL and DLL Disabled					
Typical	60	60	60	60	mW
Sleep Mode—PLL and SYSCLK Disabled					
Typical	25	25	25	25	mW
Maximum	60	60	80	100	mW

NOTES:

1. These values apply for all PLL_CFG[0-3] settings and do not include output driver power (OV_{DD}) or analog supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically ≤10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW.
2. Typical power is an average value measured at V_{DD} = AV_{DD} = 2.5V, OV_{DD} = 3.3V in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at V_{DD} = 2.625V using a worst case instruction mix.

AC ELECTRICAL CHARACTERISTICS

This section provides the AC electrical characteristics for the PID7t-603e. These specifications are for 200, 233, 266 and 300 MHz processor speed grades. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. All timings are specified respective to the rising edge of SYSCLK. PLL_CFG signals should be set prior to power up and not altered afterwards.

CLOCK AC TIMING SPECIFICATIONS

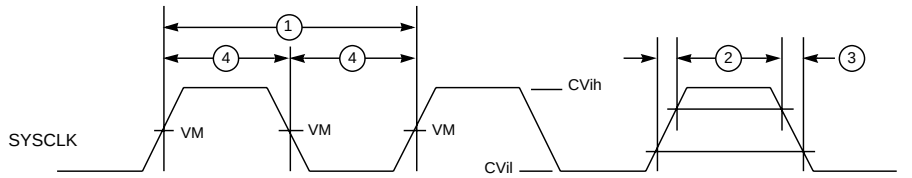
(V_{DD} = AV_{DD} = 2.5V ±5%, OV_{DD} = 3.3V ±5%, GND = 0V)

Num	Characteristics	200MHz		233MHz		266MHz		300MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Processor frequency (1)	150	200	180	233	180	266	180	300	MHz
	VCO frequency (1)	300	400	360	466	360	532	360	600	MHz
	SYSCLK frequency (1)	33.3	66.67	33.3	75	33.3	75	33.3	75	MHz
1	SYSCLK cycle time	13.3	30	13.3	30	13.3	30	13.3	30	ns
2, 3	SYSCLK rise and fall time (2)	—	2	—	2	—	2	—	2	ns
4	SYSCLK duty cycle measured at 1.4V (3)	40	60	40	60	40	60	40	60	%
	SYSCLK jitter (4)	—	±150	—	±150	—	±150	—	±150	ps
	Internal PLL relock time (3,5)	—	100	—	100	—	100	—	100	µs

NOTES:

1. Caution: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for the SYSCLK input are measured from 0.4 to 2.4V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Cycle-to-cycle jitter, and is guaranteed by design. The total input jitter (short term and long term combined) must be under ±150 ps to guarantee the input/output timing.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD}, OV_{DD}, AV_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100µs) during the power-on reset sequence.

FIG. 2 SYSCLK INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4 V)

INPUT AC TIMING SPECIFICATIONS[1]

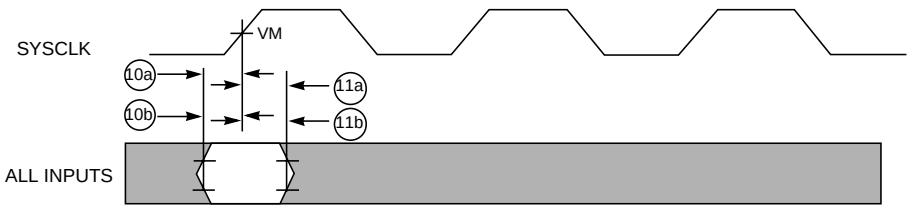
(V_{DD} = AV_{DD} = 2.5V ±5%, OV_{DD} = 3.3V ±5%, GND = 0V)

Num	Characteristics	200MHz		233, 266, 300MHz		Unit
		Min	Max	Min	Max	
10a	Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup) (2)	2.5	—	2.5	—	ns
10b	All Other Inputs Valid to SYSCLK (Input Setup) (3)	4.0	—	3.5	—	ns
10c	Mode Select Inputs Valid to $\overline{\text{HRESET}}$ (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$) (4,5,6,7)	8	—	8	—	tsysclk
11a	SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold) (2)	1.0	—	1.0	—	ns
11b	SYSCLK to All Other Inputs Invalid (Input Hold) (3)	1.0	—	1.0	—	ns
11c	$\overline{\text{HRESET}}$ to Mode Select Inputs Invalid (Input Hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$) (4,6,7)	0	—	0	—	ns

NOTES:

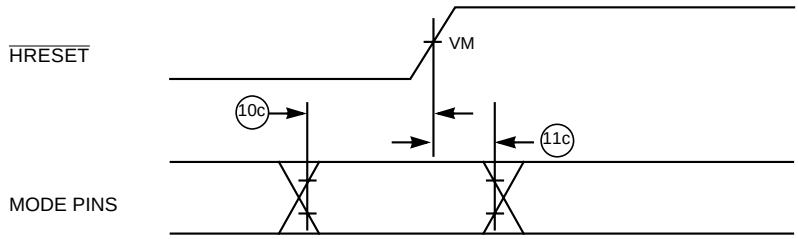
1. Input specifications are measured from the TTL level (0.8 to 2.0V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Address/Data/Transfer Attribute input signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TC[0–1], $\overline{\text{TBST}}$, TSIZ[0–2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].
3. All other input signals are composed of the following—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 5).
5. tsysclk is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Guaranteed by design and are not tested.
7. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.

FIG. 3 INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4 V)

FIG. 4 MODE SELECT INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4 V)

OUTPUT AC TIMING SPECIFICATIONS[1]

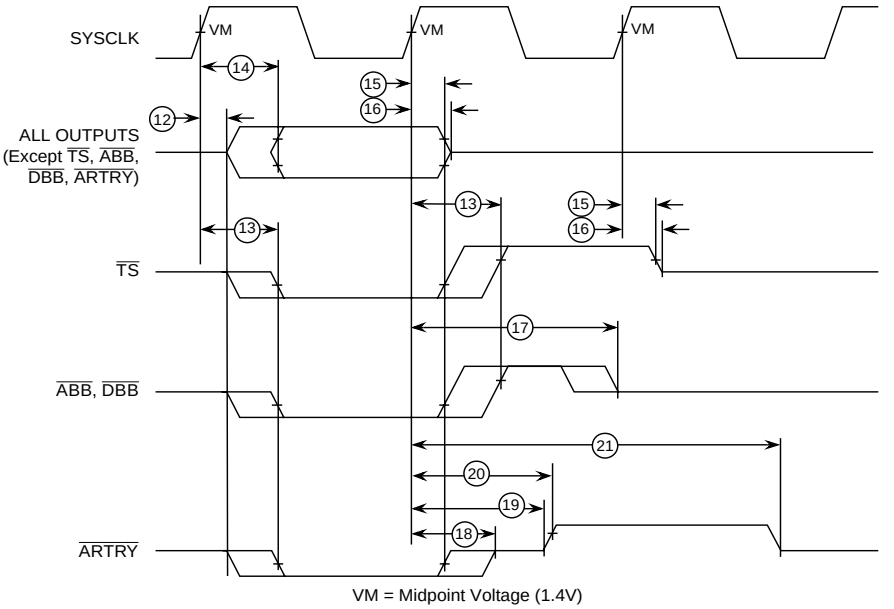
(V_{DD} = AV_{DD} = 2.5V ±5%, OV_{DD} = 3.3V ±5%, GND = 0V, C_L = 50 pF; *unless otherwise noted*)

Num	Characteristics	200MHz Min	200MHz Max	233, 266, 300MHz Min	233, 266, 300MHz Max	Unit
12	SYSCLK to Output Driven (Output Enable Time)	1.0	—	1.0	—	ns
13a	SYSCLK to Output Valid (5.5V to 0.8V—$\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (3)	—	9.0	—	9.0	ns
13b	SYSCLK to Output Valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (5)	—	8.0	—	8.0	ns
14a	SYSCLK to Output Valid (5.5V to 0.8V—all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (3)	11.0	—	11.0	—	ns
14b	SYSCLK to Output Valid (all except TS, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (5)	—	9.0	—	9.0	ns
15	SYSCLK to Output Invalid (Output Hold) (2)	1.0	—	1.0	—	ns
16	SYSCLK to Output High Impedance (all except $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	8.5	—	8.0	ns
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$ High Impedance after precharge (4,6)	—	1.0	—	1.0	tsysclk
18	SYSCLK to $\overline{ARTRY}$ High Impedance before precharge	—	8.0	—	7.5	ns
19	SYSCLK to $\overline{ARTRY}$ Precharge Enable (2,4,7)	0.2*tsysclk +1.0	—	0.2*tsysclk +1.0	—	ns
20	Maximum Delay to $\overline{ARTRY}$ Precharge (4,7)	—	1.0	—	1.0	tsysclk
21	SYSCLK to $\overline{ARTRY}$ High Impedance After Precharge (5,7)	—	2.0	—	2.0	tsysclk

NOTES:

1. All output specifications are measured from the 1.4V of the rising edge of SYSCLK to TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin.
2. This minimum parameter assumes C_L = 0 pF.
3. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5V CMOS levels instead of 3.3V CMOS levels).
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
5. Output signal transitions from GND to 2.0V or Vdd to 0.8V.
6. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
7. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.

FIG. 5 OUTPUT TIMING DIGRAM



VM = Midpoint Voltage (1.4V)

JTAG AC TIMING SPECIFICATIONS

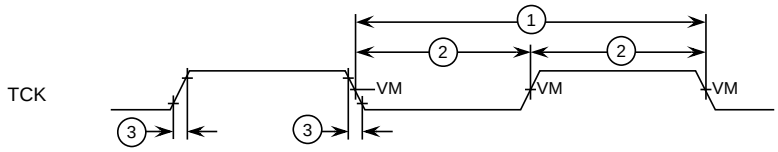
(V_{DD} = AV_{DD} = 2.5V ±5%, OV_{DD} = 3.3V ±5%, GND = 0V, C_L = 50 pF; *unless otherwise noted*)

Num	Characteristics	Min	Max	Unit
	TCK frequency of operation	0	16	MHz
1	TCK cycle time	62.5	—	ns
2	TCK clock pulse width measured at 1.4V	25	—	ns
3	TCK rise and fall times	0	3	ns
4	$\overline{TRST}$ setup time to TCK rising edge (1)	13	—	ns
5	$\overline{TRST}$ assert time	40	—	ns
6	Boundary scan input data setup time (2)	6	—	ns
7	Boundary scan input data hold time (2)	27	—	ns
8	TCK to output data valid (3)	4	25	ns
9	TCK to output high impedance (3)	3	24	ns
10	TMS, TDI data setup time	0	—	ns
11	TMS, TDI data hold time	25	—	ns
12	TCK to TDO data valid	4	24	ns
13	TCK to TDO high impedance	3	15	ns

NOTES:

1. $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

FIG. 6 JTAG CLOCK INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4V)

FIG. 7 $\overline{TRST}$ TIMING DIAGRAM

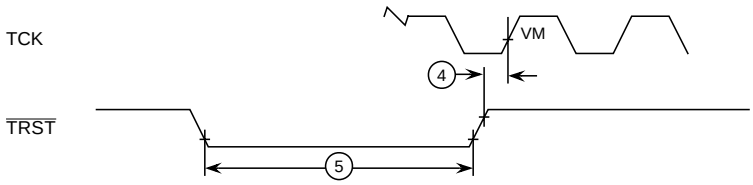


FIG. 8 BOUNDARY-SCAN TIMING DIAGRAM

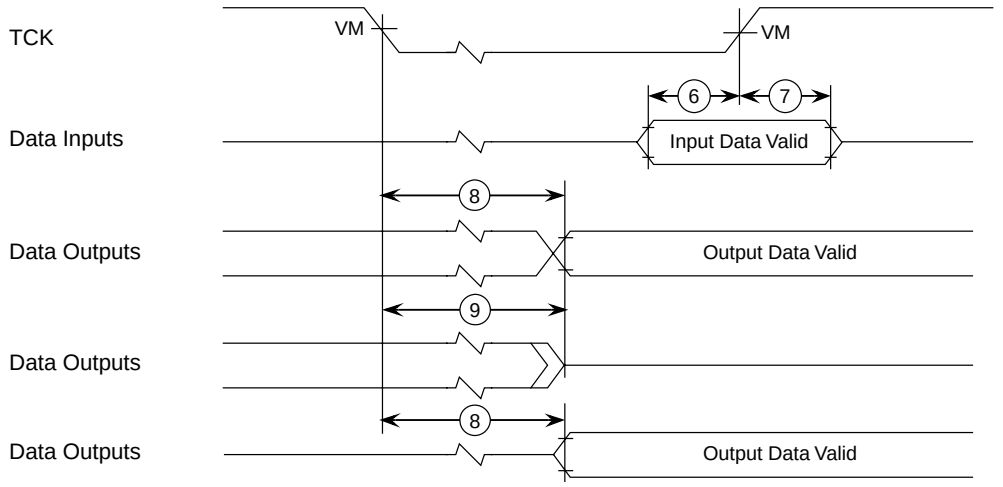
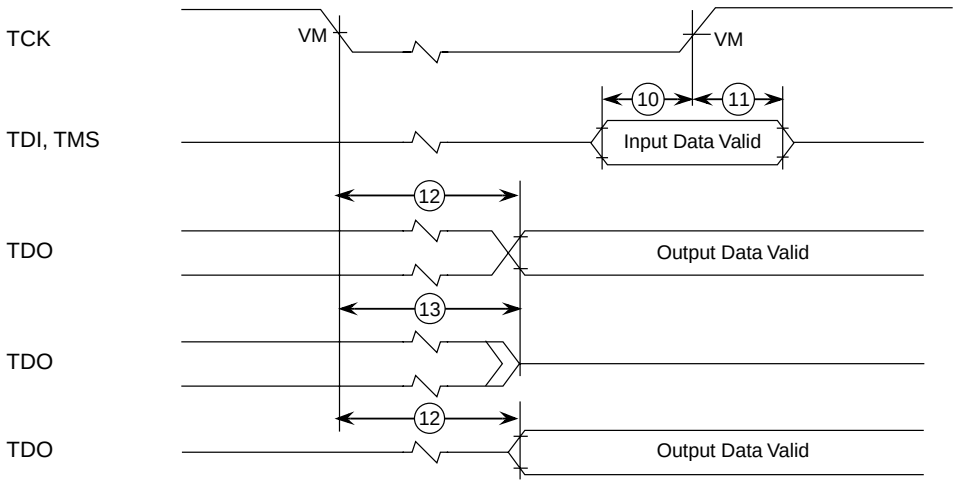


FIG. 9 TEST ACCESS PORT TIMING DIAGRAM



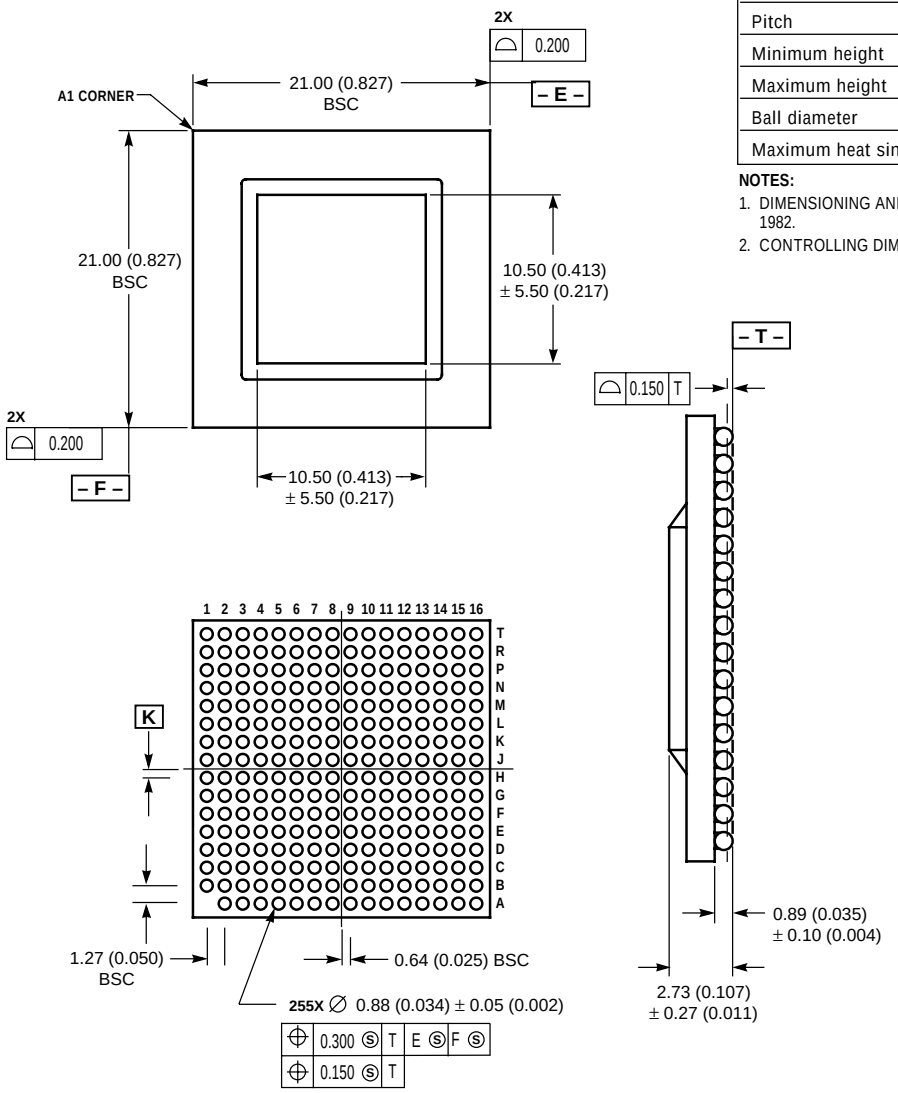
PACKAGE DIMENSION: 255 CERAMIC BALL GRID ARRAY (CBGA)

PACKAGE DESCRIPTION

Package Outline	21mm x 21mm
Interconnects	255
Pitch	1.27mm (50mil)
Minimum height	2.45mm (0.096")
Maximum height	3.00mm (0.118")
Ball diameter	0.89mm (35mil)
Maximum heat sink force	10 lbs

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982.
2. CONTROLLING DIMENSION: MILLIMETER.



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

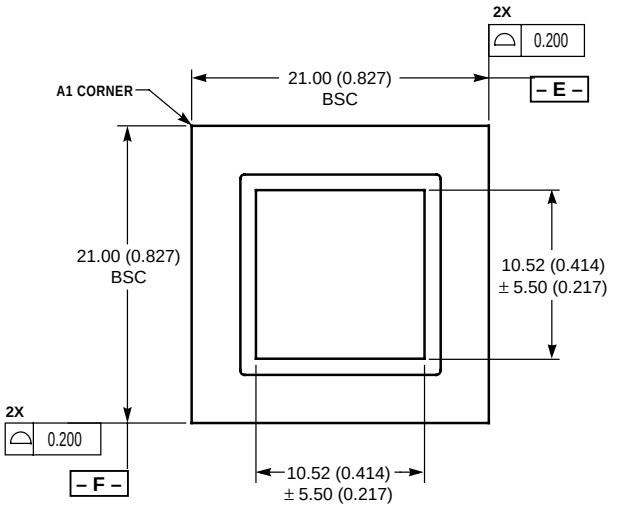
PACKAGE DIMENSION: 255 CERAMIC COLUMN GRID ARRAY (CCGA)

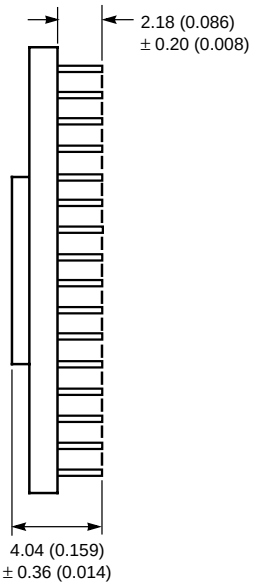
PACKAGE DESCRIPTION

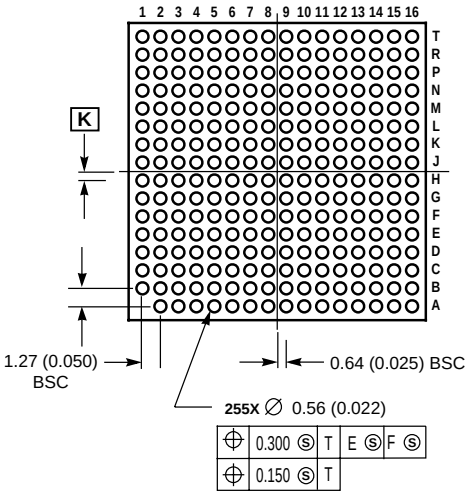
Package Outline	21mm x 21mm
Interconnects	255
Pitch	1.27mm (50mil)
Minimum height	3.65mm (0.144")
Maximum height	4.39mm (0.173")
Column diameter	0.56mm (0.022")
Maximum heat sink force	10 lbs

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982.
2. CONTROLLING DIMENSION: MILLIMETER.







ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

SYSTEM DESIGN INFORMATION

The 603e PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MCM is shown for nominal frequencies.

PLL CONFIGURATION

PLL_CFG[0-3]	Sample Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 25 MHz	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz	Bus 75 MHz
0100	2x	2x						133 (266)	150 (300)
0101	2x	4x			80 (320)	100 (400)	120 (600)		
0110	2.5x	2x					150 (300)	166 (333)	187 (375)
1000	3x	2x				150 (300)	180 (360)	200 (400)	225 (450)
1110	3.5x	2x			140 (280)	175 (350)	210 (420)	233 (466)	263 (525)
1010	4x	2x		133 (266)	160 (320)	200 (400)	240 (480)	267 (533)	300 (600)
0111	4.5x	2x		150 (300)	180 (360)	225 (450)	270 (540)	300 (600)	
1011	5x	2x		166 (333)	200 (400)	250 (500)	300 (600)		
1001	5.5x	2x	137 (275)	183 (366)	220 (440)	275 (550)			
1101	6x	2x	150 (300)	200 (400)	240 (480)	300 (600)			
0011	PLL bypass								
1111	Clock off								

NOTES:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not supported, see "Clock AC Specifications" for valid SYSCLK and VCO frequencies.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.

   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the MCM regardless of the SYSCLK input.

PLL POWER SUPPLY FILTERING

The AVdd power signal is provided on the WEDMC64603R-XXX to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 10. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible. The 0.1 µF capacitor should be closest to the AVdd pin, followed by the 10 µF capacitor, and finally the 10 Ω resistor to Vdd. These traces should be kept short and direct.

DECOUPLING RECOMMENDATIONS

Due to the WEDMC64603R-XXX's dynamic power management feature, large address and data buses, and high operating frequencies, the WEDMC64603R-XXX can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the WEDMC64603R-XXX system, and the WEDMC64603R-XXX itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd and OVdd pin of the WEDMC64603R-XXX. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 mF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd or OVdd pin. Suggested values for the Vdd pins—220 pF (ceramic), 0.01 µF (ceramic), and 0.1 µF (ceramic). Suggested values for the OVdd pins—0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

CONNECTION RECOMMENDATIONS

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, and GND pins of the WEDMC64603R-XXX.

PULL-UP RESISTOR REQUIREMENTS

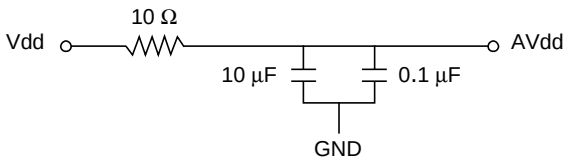
The WEDMC64603R-XXX requires high-resistive (weak: 10 KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the WEDMC64603R-XXX or other bus master. These signals are—$\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the WEDMC64603R-XXX has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 KΩ–10 KΩ) if they are used by the system. These signals are—$\overline{APE}$, $\overline{DPE}$, and $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the WEDMC64603R-XXX must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the WEDMC64603R-XXX. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are—A[0–31], AP[0–3], TT[0–4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

FIG. 10 PLL POWER SUPPLY FILTER CIRCUIT



THERMAL MANAGEMENT INFORMATION

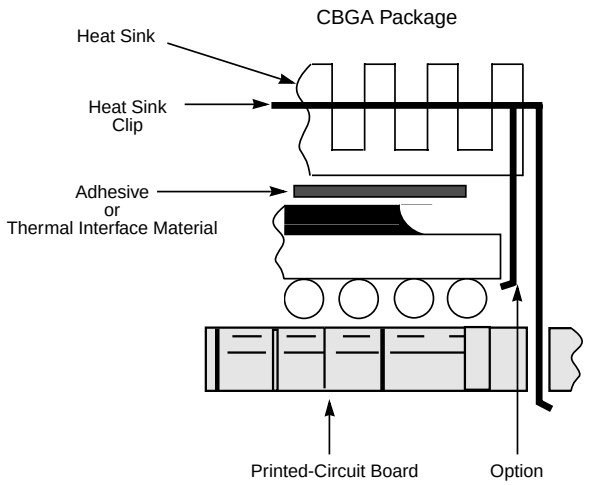
This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (CBGA package); see Figure 12. This spring force should not exceed 5.5 pounds of force.

The board designer can choose between several types of heat sinks to place on the WEDMC64603R-XXX. There are several commercially-available heat sinks for the WEDMC64603R-XXX provided by the following vendors:

Chip Coolers Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979	800-227-0254 (USA/Canada) 401-739-7600
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502	818-842-7277
Thermalloy 2021 W. Valley View Lane P.O. Box 810839 Dallas, TX 75731	214-243-4321
Wakefield Engineering 60 Audubon Rd. Wakefield, MA 01880	617-245-5900
Aavid Engineering One Kool Path Laconia, NH 03247-0440	603-528-3400

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

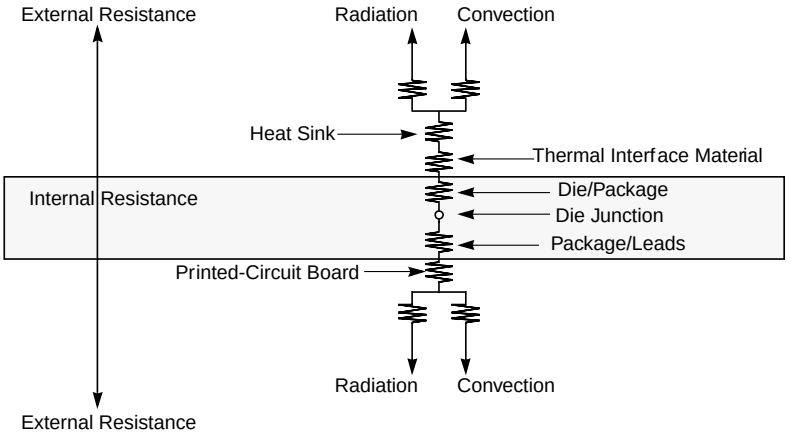
FIG. 11 PACKAGE EXPLODED CROSS-SECTIONAL VIEW WITH SEVERAL HEAT SINK OPTIONS



INTERNAL PACKAGE CONDUCTION RESISTANCE

For this packaging technology the intrinsic thermal conduction resistance (shown in Package Thermal Characteristics) versus the external thermal resistance paths are shown in Figure 12 for a package with an attached heat sink mounted to a printed-circuit board.

FIG. 12 PACKAGE WITH HEAT SINK MOUNTED TO A PRINTED CIRCUITY BOARD



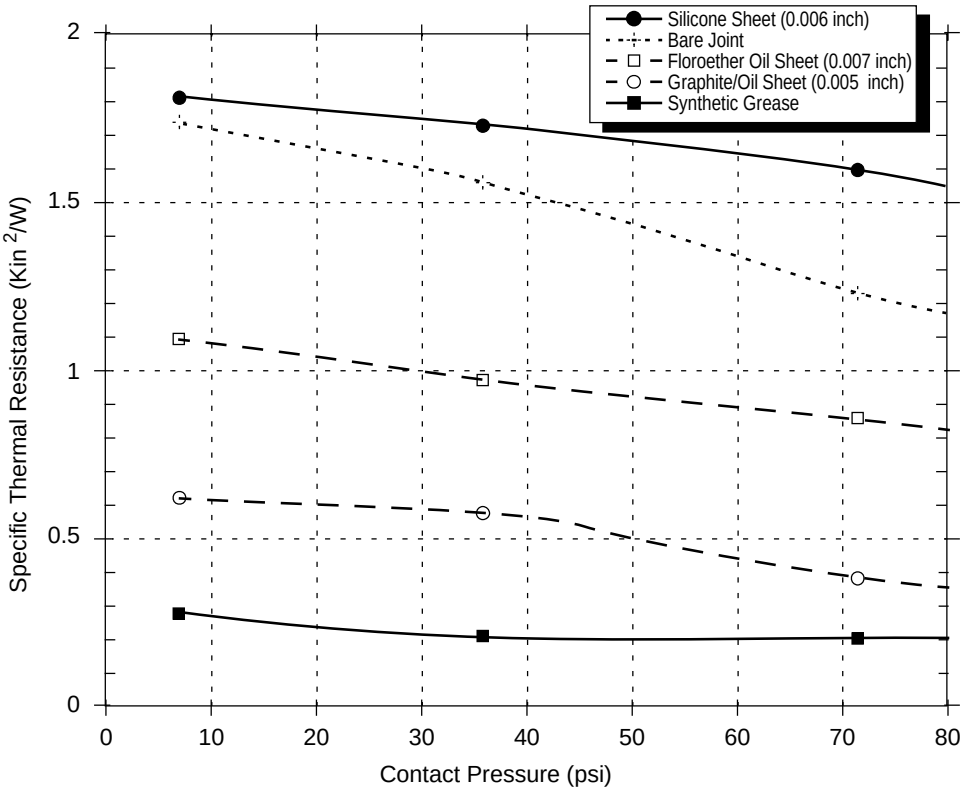
(Note the internal versus external package resistance)

ADHESIVES AND THERMAL INTERFACE MATERIALS

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 13 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 11). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

FIG. 13 THERMAL PERFORMANCE OF SELECT THERMAL INTERFACE MATERIAL



The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation Dow-Corning Electronic Materials PO Box 0997 Midland, MI 48686-0997	517-496-4000
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4850	617-935-4850
Thermagon Inc. 3256 West 25th Street Cleveland, OH 44109-1668	216-741-7659
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067	860-571-5100
AI Technology (e.g. EG7655) 1425 Lower Ferry Rd. Trent, NJ 08618	609-882-2332

The following section provides a heat sink selection example using one of the commercially available heat sinks.

HEAT SINK SELECTION EXAMPLE

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in the Recommended Operating Temperatures. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CQFP package θ_{jc} = 0.095, and a power consumption (P_d) of 3.0 watts, the following expression for T_j is obtained:

Die-junction temperature:

$$T_j = 30°C + 5°C + (0.095°C/W + 1.0°C/W + R_{sa}) * 3.0\ W$$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 14.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.095°C/W + 1.0°C/W + 7°C/W) * 3.0\ W,$$

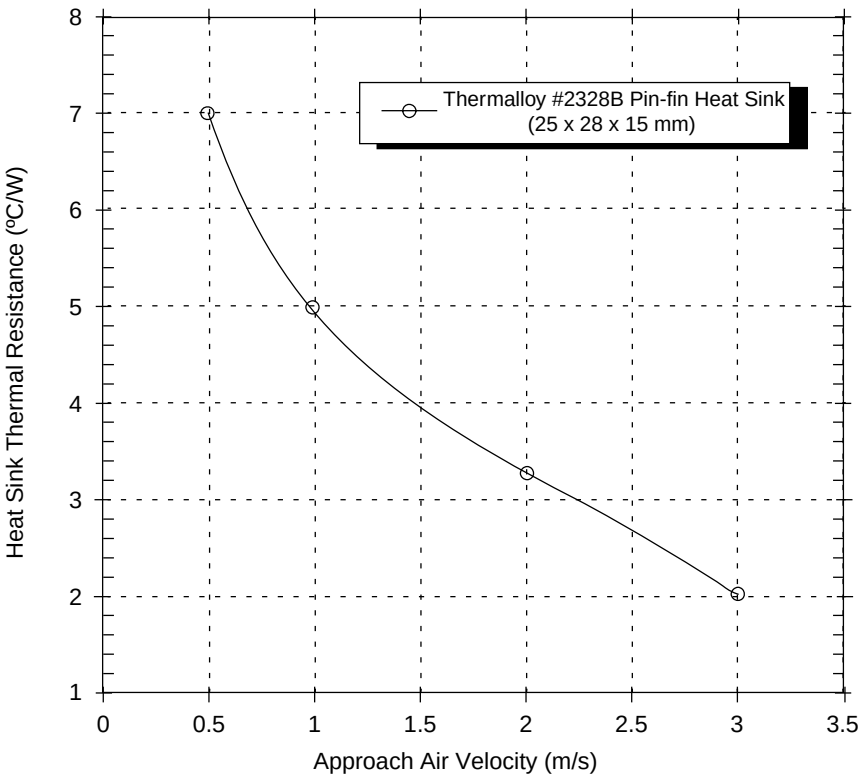
resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

FIG. 14 THERMALLOY #2328B HEAT SINK-TO-AMBIENT THERMAL RESISTANCE VERSUS AIRFLOW VELOCITY



ORDERING INFORMATION