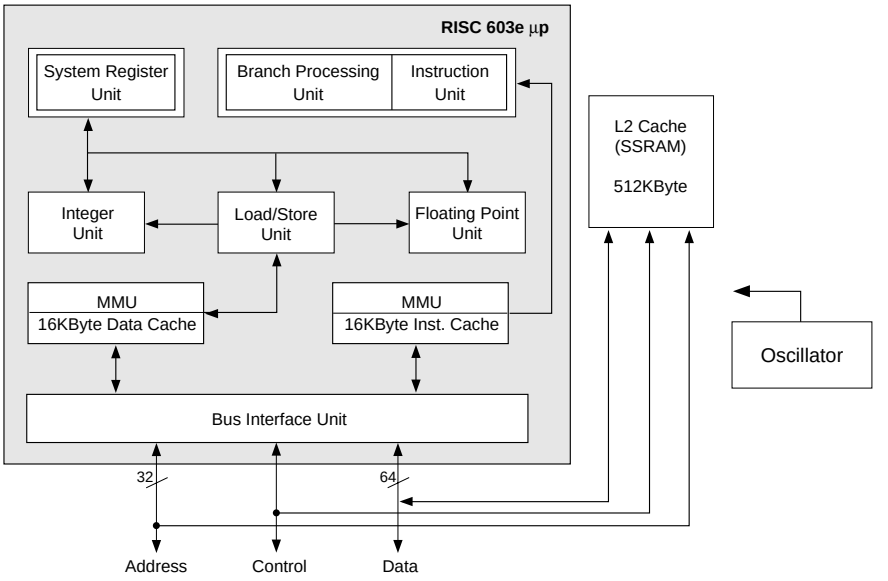
RISC 603e MODULE, SECONDARY L2 CACHE *ADVANCED **

MAIN FEATURES

- Based on RISC 603e 3.3V Microprocessor
- Processor Clock Frequencies: 66.6, 80, 100 MHz
- Bus Clock Frequencies: Up to 66.6 MHz
- 32-bit Address Bus/64-bit Data Bus
- Built-in Oscillator
- Primary Cache: Dual 16KByte (Instructions and Data)
- Secondary L2 Cache: 512KByte (64Kx72)
- Packaging:
  - 240 lead, Hermetic CQFP (31mm square)
- Footprint compatible with 603e µp CQFP package
- Single 3.3V ±5% Power Supply.
- Industrial and Military Screeening.
- In-System Testability and Debugging through Boundary Scan Capability (JTAG)
- Built-in decoupling caps and Multiple Power and Ground pins for low noise operation, Separate Power and Ground planes to Improve Noise Immunity.

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1
BLOCK DIAGRAM



DESCRIPTION

■ RISC 603e Microprocessor.

- High-performance, superscalar microprocessor
  - As many as 3 instructions issued and retired per clock
  - As many as 5 instructions issued and retired per clock
  - Single-cycle execution for most instructions
  - Pipelined Floating-Point Unit (FPU) for all single-precision and most double-precision operations
- Five independent execution units and two register files
  - Branch Processing Unit (BPU) featuring static branch prediction
  - A 32-bit Instruction Unit (IU)
  - Fully IEEE 754-compliant FPU for both single- and double-precision operations
  - Load/Store Unit (LSU) for data transfer between data cache and GPRs and FPRs
  - System Register Unit (SRU) that executes condition register (CR), special purpose register (SPR) instruc tions, and integer add/compare instructions
  - Thirty-two General Purpose Registers (GPRs) for integer operands
  - Thirty-two Floating-Point Registers (FPRs) for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instruc tions per clock from the instruction cache
  - A 6-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16KByte data cache–four-way set-associative, physically addressed; Least Recently Used (LRU) replacement algorithm
  - 16KByte instruction cache–four-way set-associative, physically addressed; Least Recently Used (LRU) replacement algorithm
  - Cache write-back or write-through operation program-able on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4KByte page size, variable block size, and 256MByte segment size
  - A 64-entry, two-way set-associative Instruction Translation Lookaside Buffer (ITLB)
  - A 64-entry, two-way set-associative Data Translation Lookaside Buffer (DTLB)
  - 4-entry data and instruction Block Address Translation (BAT) arrays providing 128KByte to 256MByte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32 or 64-bit split transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of order bus transactions
- Integrated power management
  - Low power 3.3V design
  - Selectable internal processor/bus clock multiplier that provides 1/1, 1.5/1, 2/1, 2.5/1, 3/1, 3.5/1, and 4/1 ratios
  - Three power saving modes: doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through boundary-scan capability (JTAG)

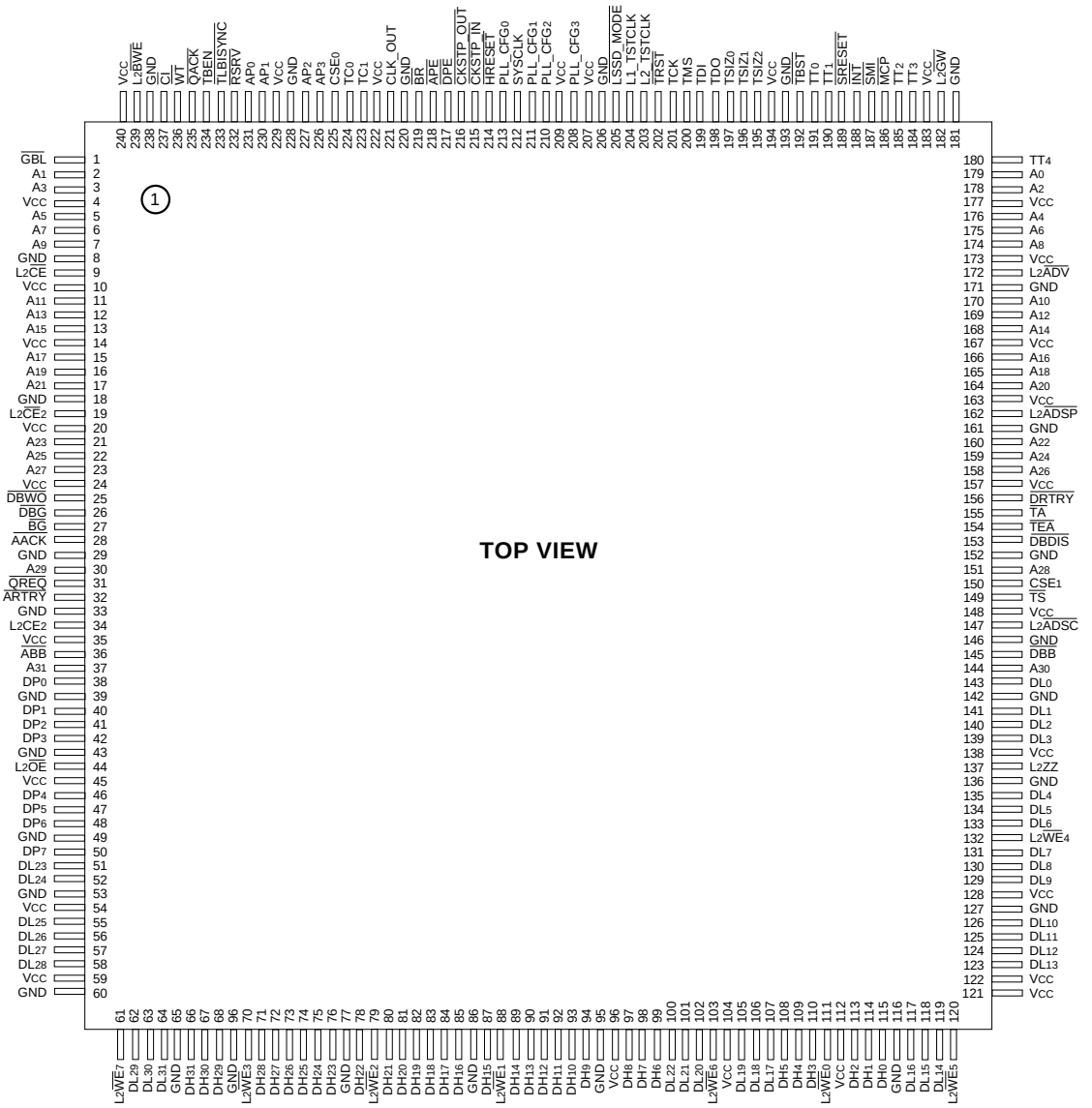
■ Secondary L2 Cache.

- 512KByte Secondary Cache
- Organized as 64Kx72
- 66 MHz Zero wait state performance (2-1-1-1 Burst)

■ Oscillator

- Supply the System Clock frequency (Bus Clock) choice of 16.6, 33.3 or 66.6 MHz
- Externally accessible on pin 212 (SYSCLK)

FIG. 2 PIN CONFIGURATION FOR WC64P603EV-XQ3X, 240 PIN CQFP (Q3)



Note: L2xx are specific secondary cache signals.

SIGNAL INDEX

Pin	Symbol	Signal Name	Type	Description
179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	A_{0-31}	Address Bus	I/O	As an output, represents the physical address of the data to be transferred. As an input, represents the physical address of a snoop operation.
115,114,113,110,109, 108, 99, 98, 97, 94, 93, 92,91,90,89,87,85,84, 83,82,81,80,78,76,75, 74,73,72,71,68,67,66	DH_{0-31}	Data Bus High	I/O	Represents the state of data, during a data write operation as an output, or during a data read operation as an input.
143,141,140,139,135, 134,133,131,130,129, 126,125,124,123,119, 118,117,107,106,105, 102,101,100,51,52,55, 56, 57, 58, 62, 63, 64	DL_{0-31}	Data Bus Low	I/O	Represents the state of data, during a data write operation as an output, or during a data read operation as an input.
28	$\overline{AACK}$	Address Acknowledge	Input	If asserted, indicates that the address phase of a transaction is complete.
36	$\overline{ABB}$	Address Bus Busy	I/O	As an input, if asserted, the 603e is the address bus master. As an output, if asserted, the addres bus is in use.
231, 230, 227, 226	AP_{0-3}	Address Bus Parity	I/O	As an output, represents odd parity for each of 4 bytes of the physical address for a transaction. As an input, represents odd parity for each of 4 bytes of the physical address for snooping operations.
218	$\overline{APE}$	Address Parity Error	Output	If asserted, indicates incorrect address bus parity detected on a snoop ($\overline{GBL}$ asserted).
32	$\overline{ARTRY}$	Address Retry	I/O	As an output, if asserted, indicates that the 603e detects a condition in which a snoop address tenure must be retried. As an input, if asserted and if the 603e is the address bus master indicates that the 603e must retry the preceding address tenure and immediately negate $\overline{BR}$ (if asserted).
27	$\overline{BG}$	Bus Grant	Input	May, with the proper qualification, assume mastership of the address bus.
219	$\overline{BR}$	Bus Request	Output	Request mastership of the address bus.
237	$\overline{CI}$	Cache Inhibit	Output	If asserted, indicates that a single-beat transfer will not be cached.
221	CLK_OUT	Test Clock	Output	Provides PLL clock output for PLL testing and monitoring.
215	$\overline{CKSTP\_IN}$	Checkstop Input	Input	Must terminate operation by internally gating off all clocks, and release all outputs (except $\overline{CKSTP\_OUT}$) to the high impedance state.
216	$\overline{CKSTP\_OUT}$	Checkstop Output	Output	If asserted, indicates that the 603e has detected a checkstop condition and has ceased operation.
225, 150	CSE_{0-1}	Cache Set Entry	Output	If asserted, represents the cache replacement set element for the current transaction reloading into or writing out of the cache.
145	$\overline{DBB}$	Data Bus Busy	I/O	As an output, if asserted, indicates that the 603e is the data bus master. As an input, if asserted, indicates that another device is bus master.
153	$\overline{DBDIS}$	Data Bus Disable	Input	If asserted, indicates that the 603e (for a write transaction) must release data bus and the data bus parity to high impedance during the following cycle.
26	$\overline{DBG}$	Data Bus Grant	Input	If asserted, indicates that the 603e may, with the proper qualification, assume mastership of the data bus.
25	$\overline{DBWO}$	Data Bus Write Only	Input	If asserted, indicates that the 603e may run data bus tenure for an outstanding write address even if a read address is pipelined before the write address.
38, 40, 41, 42, 46, 47, 48, 50	DP_{0-7}	Data Bus Parity	I/O	As an output, represents odd parity for each of 8 bytes of data write transactions. As an input, represents odd parity for each byte of read data.
217	$\overline{DPE}$	Data Parity Error	Output	Incorrect data bus parity.
156	$\overline{DRTRY}$	Data Retry	Input	If asserted, indicates that the 603e must invalidate the data from the previous read operation.
1	$\overline{GBL}$	Global	I/O	As an output, if asserted, indicates that a transaction is global. As an input, if asserted, indicates that a transaction must be snooped by the 603e.
214	$\overline{HRESET}$	Hard Reset	Input	Initiates a complete hard reset operation which causes a reset exception.
188	$\overline{INT}$	Interrupt	Input	If asserted, the 603e initiates an interrupt if bit EE of MSR register is set, otherwise, the 603e ignores the interrupt.
205	$\overline{LSSD\_MODE}$		Input	LSSD test control signal for factory use only.

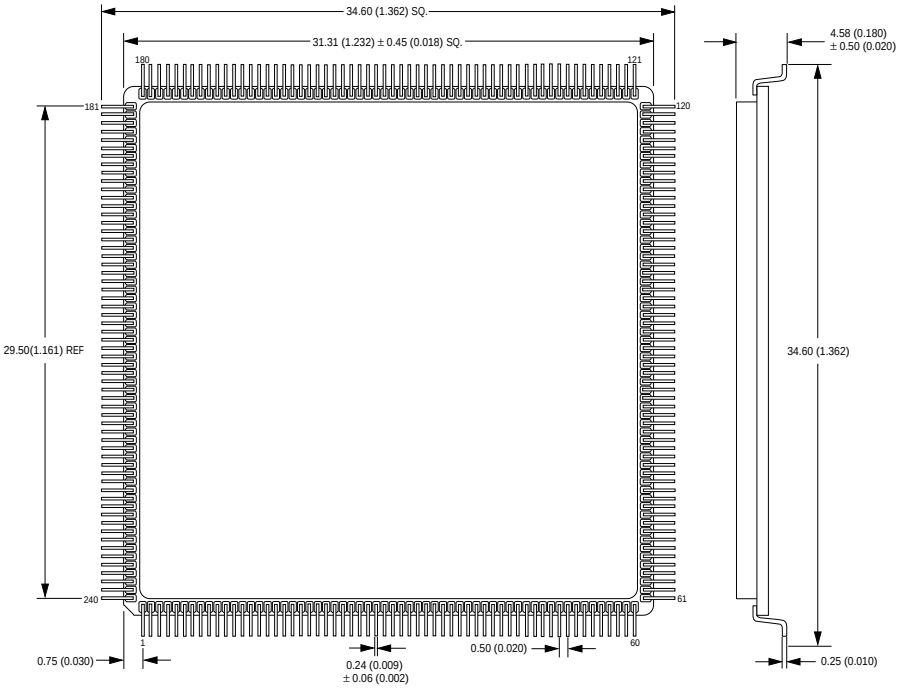
SIGNAL INDEX (continued)

Pin	Symbol	Signal Name	Type	Description
204	L1_TSTCLK		Input	LSSD test control signal for factory use only.
203	L2_TSTCLK		Input	LSSD test control signal for factory use only.
186	$\overline{MCP}$	Machine Check Interrupt	Input	If asserted, the 603e initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set.
213, 211, 210, 208	PLL_CFG0-3	PLL Configuration	Input	Configures the operation of the PLL and the internal processor clock frequency.
235	$\overline{QACK}$	Quiescent Acknowledge	Input	If asserted, all bus activity that requires snooping has terminated or paused and the 603e may enter a quiescent (low power) state.
31	$\overline{QREQ}$	Quiescent Request	Output	If asserted,the 603e is requesting all normal bus activity to enter a quiescent (low power) state. Once the 603e has entered a quiescent state, it no longer snoops bus activity.
232	$\overline{RSRV}$	Reservation	Output	Represents the state of the reservation coherency bit in the reservation address register that is used by the lwarx and stwcx instructions.
187	$\overline{SMI}$	System Management Interrupt	Input	If asserted,the 603e initiates a system management interrupt operation if the bit EE of MSR register is set, otherwise, the 603e ignores the interrupt.
189	$\overline{SRESET}$	Soft Reset	Input	Initiates processing for reset exception.
212	SYSCLK	System Clock	Output	Represents the primary clock input for the 603e, and the bus clock frequency for 603e bus operation.
155	$\overline{TA}$	Transfer Acknowledge	Input	If asserted, indicates that a single-beat data transfer completed successfully or that a data beat in a burst transfer completed successfully.
234	TBEN	Timebase Enable	Input	If asserted, indicates that the timebase should continue clocking.
192	$\overline{TBST}$	Transfer Burst		As an output, if asserted, indicates that a burst transfer is in progress As an input, used when snooping for single-beat reads (read with no intent to cache).
224, 223	TC0-1	Transfer Code	Output	When asserted, represents a special encoding for the transfer in progress.
201	TCK	Test Clock	Input	Clock signal for the Boundary Scan Test Access Port (TAP).
199	TDI	Test Data Input	Input	Test Data Input for the TAP.
198	TDO	Test Data Output	Output	Test Data Output for the TAP.
154	$\overline{TEA}$	Transfer Error Acknowledge	Input	If asserted, indicates that a bus error occurred which causes a machine check exception.
233	$\overline{TLBISYNC}$	TLBI Sync	Input	If asserted, indicates that instruction execution should stop after execution of a **tlbsync** instruction.
200	TMS	Test Mode Select	Input	Selects the principal operations of the test-support circuitry.
202	$\overline{TRST}$	Test Reset	Input	Provides an asynchronous reset of the TAP controller.
197, 196, 195	TSIZ0-2	Transfer Size	Output	For memory accesses, these signals along with $\overline{TBST}$ indicate the data transfer size for the current bus operation.
149	$\overline{TS}$	Transfer Start	I/O	As an output, indicates the beginning of a memory bus transaction and the address bus and transfer attribute signals are valid. As an input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$).
191, 190, 185 184, 180	TT0-4	Transfer Type	I/O	Type of transfer in progress.
236	$\overline{WT}$	Write-Through	Output	If asserted, indicates that a single-beat transaction is write-through.
111, 89, 79, 70, 132, 120, 103, 61	L2$\overline{WE}$0-7	Synchronous Byte Write Enables	Input	These active Low inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of the SYSCLK. A byte write enable is Low for a Write Cycle and High for a Read Cycle. L2$\overline{WE}$0 controls DL0-7 L2$\overline{WE}$4 controls DH0-7 L2$\overline{WE}$1 controls DL8-5 L2$\overline{WE}$5 controls DH8-5 L2$\overline{WE}$2 controls DL16-23 L2$\overline{WE}$6 controls DH16-23 L2$\overline{WE}$3 controls DL24-31 L2$\overline{WE}$7 controls DH24-31 Data I/Os are tristated if either of these inputs are low and L2$\overline{BWE}$ is Low.
239	L2$\overline{BWE}$	Byte Write Enable	Input	This active Low input permits byte write operations and must meet the setup and hold times around the rising edge of SYSCLK.
182	L2$\overline{GW}$	Global Write	Input	This active Low input allows a full 72-bit Write to occur independent of the L2$\overline{BWE}$ and L2$\overline{WE}$x lines and must meet the setup and hold times around the rising edge of SYSCLK.
9	L2$\overline{CE}$	Synchronous Chip Enable	Input	This active Low input is used to enable the device and conditions the internal use of L2$\overline{ADSP}$. This input is sampled only when a new external address is loaded.

SIGNAL INDEX (continued)

Pin	Symbol	Signal Name	Type	Description
19	L2$\overline{CE}$2	Synchronous Chip Enable	Input	This active Low input is used to enable the device. This input is sampled only when a new external address is loaded.
137	L2ZZ	Snooze Enable	Input	This active High asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
34	L2CE2	Synchronous Chip Enable	Input	This active High input is used to enable the device. This input is sampled only when a new external address is loaded.
44	L2$\overline{OE}$	Output Enable	Input	This active Low asynchronous input enables the data I/O output drivers.
172	L2$\overline{ADV}$	Synchronous Address Advance	Input	This active Low input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A High on this pin effectively causes wait states to be generated (no address advance). This pin must be High at the rising edge of the first clock after an L2$\overline{ADSP}$ cycle is initiated if a Write cycle is desired (to ensure use of correct address).
162	L2$\overline{ADSP}$	Synchronous Address Status Processor	Input	This active Low input interrupts ongoing burst, causing a new external address to be registered. A Read is performed using the new address, independent of the byte write enables and L2$\overline{ADSC}$ but dependent upon L2$\overline{CE}$ being Low.
147	L2$\overline{ADSC}$	Synchronous Address Status Controller	Input	This active Low input interrupts ongoing burst, causing a new external address to be registered. A Read or Write is performed using the new address if L2$\overline{CE}$ is Low. L2$\overline{ADSC}$ is also used to place the memory into power-down state when L2$\overline{CE}$ is High.

FIG. 3 240 PIN, CERAMIC QUAD FLAT PACK, CQFP (Q3)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION