RISC 603e MONOLITHIC MICROPROCESSOR *PRELIMINARY**

FEATURES

- Processor Clock Frequencies of 80MHz and 100MHz
- Military Operating Temperature Range
- Packaging:
  - 240 lead 31.31mm Ceramic Quad Flatpack, CQFP
- High-performance, superscalar microprocessor
  - As many as 3 instructions issued and retired per clock
  - As many as 5 instructions in execution per clock
  - Single-cycle execution for most instructions
  - Pipelined Floating-Point Unit (FPU) for all single-precision and most double-precision operations
- Five independent execution units and two register files
  - Branch Processing Unit (BPU) featuring static branch prediction
  - A 32-bit Instruction Unit (IU)
  - Fully IEEE 754-compliant FPU for single- and double-precision operations
  - Load/Store Unit (LSU) for data transfer between data cache and GPRs and FPRs
  - System Register Unit (SRU) that executes condition register (CR), special purpose register (SPR) instructions, and integer add/compare instructions
  - Thirty-two General Purpose Registers (GPRs) for integer operands
  - Thirty-two Floating-Point Registers (FPRs) for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16KByte data cache–four-way set-associative, physically addressed; Least Recently Used (LRU) replacement algorithm
  - 16KByte instruction cache–four-way set-associative, physically addressed; Least Recently Used (LRU) replacement algorithm
  - Cache write-back or write-through operation programable on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4KByte page size, variable block size, and 256MByte segment size
  - A 64-entry, two-way set-associative Instruction Translation Lookaside Buffer (ITLB)
  - A 64-entry, two-way set-associative Data Translation Lookaside Buffer (DTLB)
  - 4-entry data and instruction Block Address Translation (BAT) arrays providing 128KByte to 256MByte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32 or 64-bit split transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions
- Integrated power management
  - Low power 3.3V design
  - Selectable internal processor/bus clock multiplier that provides 1/1, 1.5/1, 2/1, 2.5/1, 3/1, 3.5/1, and 4/1 ratios
  - Three power saving modes: doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through boundary-scan capability (JTAG)

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 BLOCK DIAGRAM

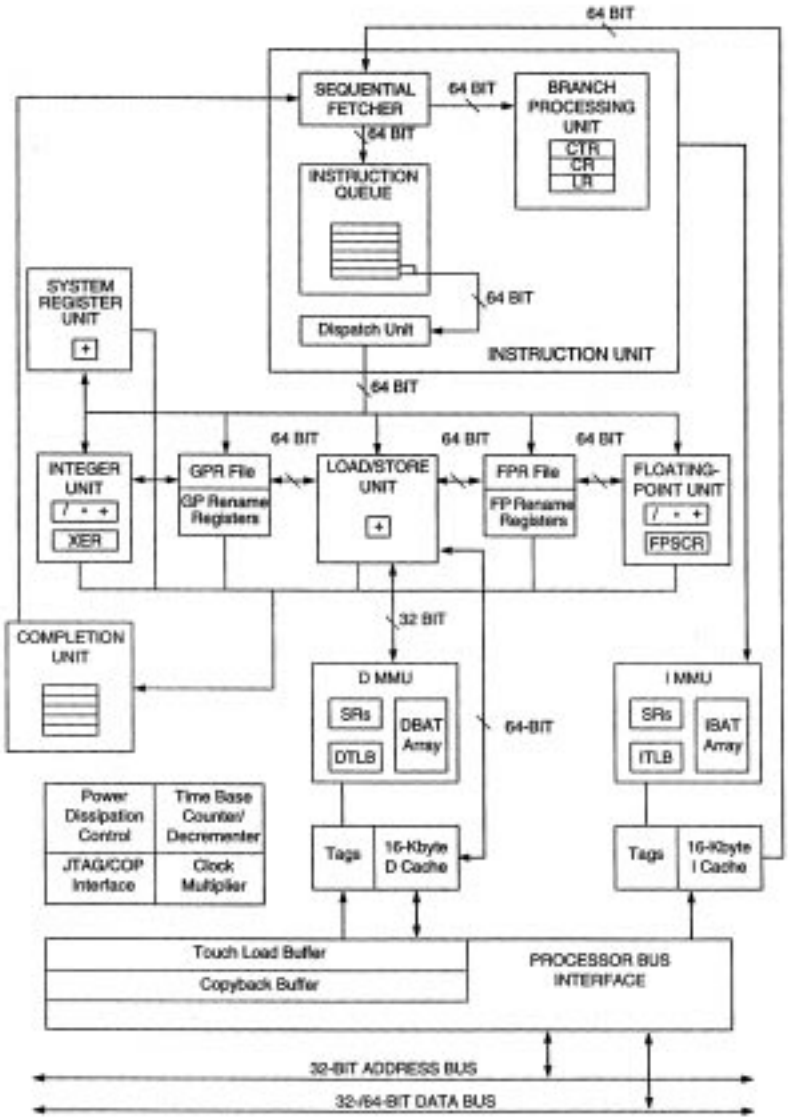
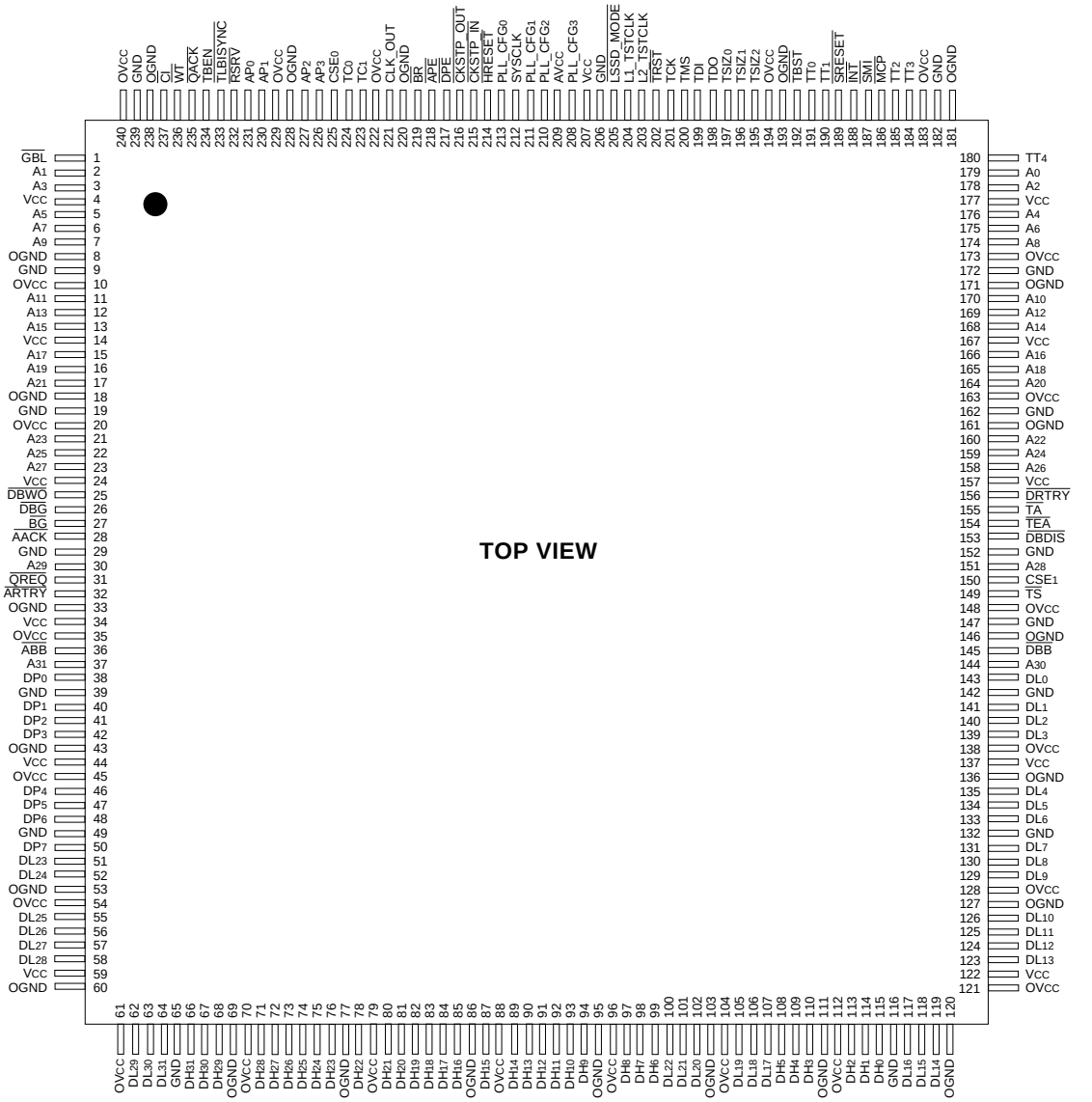


FIG. 2 PIN CONFIGURATION FOR WMC64P603EV-XQ3M, 240 PIN CQFP (Q3)



PINOUT LISTINGS FOR CQFP PACKAGE

Pin	Symbol	Signal Name	Type	Active
179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	A_{0-31}	Address Bus	I/O	High
28	$\overline{AACK}$	Address Acknowledge	Input	Low
36	$\overline{ABB}$	Address Bus Busy	I/O	Low
231, 230, 227, 226	AP_{0-3}	Address Bus Parity	I/O	High
218	$\overline{APE}$	Address Parity Error	Output	Low
32	$\overline{ARTRY}$	Address Retry	I/O	Low
209	AVcc	Address Power Supply	Input	High
27	$\overline{BG}$	Bus Grant	Input	Low
219	$\overline{BR}$	Bus Request	Output	Low
237	$\overline{CI}$	Cache Inhibit	Output	Low
221	CLK_OUT	Test Clock	Output	–
215	$\overline{CKSTP\_IN}$	Checkstop Input	Input	Low
216	$\overline{CKSTP\_OUT}$	Checkstop Output	Output	Low
225, 150	CSE_{0-1}	Cache Set Entry	Output	High
145	$\overline{DBB}$	Data Bus Busy	I/O	Low
153	$\overline{DBDIS}$	Data Bus Disable	Input	Low
26	$\overline{DBG}$	Data Bus Grant	Input	Low
25	$\overline{DBWO}$	Data Bus Write Only	Input	Low
115,114,113,110,109,108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83 ,82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66	DH_{0-31}	Data Bus High	I/O	High
143,141,140,139,135,134,133,131,130, 129,126,125,124,123,119,118,117,107, 106,105,102,101,100, 51, 52, 55, 56, 57, 58, 62, 63, 64	DL_{0-31}	Data Bus Low	I/O	High
38, 40, 41, 42, 46, 47, 48, 50	DP_{0-7}	Data Bus Parity	I/O	High
217	$\overline{DPE}$	Data Parity Error	Output	Low
156	$\overline{DRTRY}$	Data Retry	Input	Low
1	$\overline{GBL}$	Global	I/O	Low
9, 19, 29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	GND	Ground	–	–
214	$\overline{HRESET}$	Hard Reset	Input	Low
188	$\overline{INT}$	Interrupt	Input	Low
205	$\overline{LSSD\_MODE}$ (1)		Input	Low
204	L1_TSTCLK (1)		Input	–
203	L2_TSTCLK (1)		Input	–
186	$\overline{MCP}$	Machine Check Interrupt	Input	Low
8, 18, 33,43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	OGND	Ground	–	–
10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	OVcc (2)	Power Supply	–	–
213, 211, 210, 208	PLL_CFG_{0-3}	PLL Configuration	Input	High
235	$\overline{QACK}$	Quiescent Acknowledge	Input	Low
31	$\overline{QREQ}$	Quiescent Request	Output	Low

PINOUT LISTINGS FOR CQFP PACKAGE (continued)

Pin	Symbol	Signal Name	Type	Active
232	$\overline{\text{RSRV}}$	Reservation	Output	Low
187	$\overline{\text{SMI}}$	System Management Interrupt	Input	Low
189	$\overline{\text{SRESET}}$	Soft Reset	Input	Low
212	SYSCLK	System Clock	Input	–
155	$\overline{\text{TA}}$	Transfer Acknowledge	Input	Low
234	TBEN	Timebase Enable	Input	High
192	$\overline{\text{TBST}}$	Transfer Burst	I/O	Low
224, 223	$\text{TC}_{0\text{-}1}$	Transfer Code	Output	High
201	TCK	Test Clock	Input	–
199	TDI	Test Data Input	Input	High
198	TDO	Test Data Output	Output	High
154	$\overline{\text{TEA}}$	Transfer Error Acknowledge	Input	Low
233	$\overline{\text{TLBISYNC}}$	TLBI Sync	Input	Low
200	TMS	Test Mode Select	Input	High
202	$\overline{\text{TRST}}$	Test Reset	Input	Low
197, 196, 195	$\text{TSIZ}_{0\text{-}2}$	Transfer Size	Output	High
149	$\overline{\text{TS}}$	Transfer Start	I/O	Low
191, 190, 185, 184, 180	$\text{TT}_{0\text{-}4}$	Transfer Type	I/O	High
4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	Vcc (2)	Power Supply	–	–
236	$\overline{\text{WT}}$	Write-Through	Output	Low

NOTES:

1. These are tested signals for factory use only and must be pulled up to Vcc for normal machine operation.
2. OVcc inputs supply power to the I/O drivers and Vcc inputs supply power to the procerssor core.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	-55	+150	°C
Input Voltage	V_{IN}	-0.3	5.5	V
Supply Voltage	V_{CC}	-0.3	4.0	V

NOTES:

1. Functional operating conditions are given in AC and DC electrical specifica tions. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Input voltage must not be > than the supply voltage by more than 2.5V at all times including during power-on reset.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
CQFP Package Thermal Resistance, junction-to-case (typical)	θ_{JC}	2.2	°C/W
BGA Package Thermal Resistance, junction-to-case	θ_{JC}	2.1	°C/W

DC ELECTRICAL SPECIFICATIONS

(V_{CC} = 3.3 ±5.0% V DC, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Units
Input High Voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V
Input Low Voltage (all inputs except SYSCLK)	V_{OL}	GND	0.8	V
SYSCLK Input High Voltage	CV_{IH}	2.4	5.5	V
SYSCLK Input Low Voltage	CV_{IL}	GND	0.4	V
Input Leakage Current, V_{IN} = 3.465V (1)	I_{IN}	–	10	µA
V_{IN} = 5.5V (1)	I_{IN}	–	245	µA
High-Z (Off State) Leakage Current, V_{IN} = 3.465V (1)	I_{TSI}	–	10	µA
V_{IN} = 5.5V (1)	I_{TSI}	–	245	µA
Output Low Voltage, I_{OL} = 14mA	V_{OL}	–	0.4	V
Output High Voltage, I_{OH} = -9mA	V_{OH}	2.4	–	V
Capacitance, V_{IN} = 0V, f = 1MHz (2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{IN}	–	10.0	pF
Capacitance, V_{IN} = 0V, f = 1MHz (2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{IN}	–	10.0	pF

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. This parameter is guaranteed by design but not tested.

ELECTRICAL CHARACTERISTICS

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the Phase Lock Loop Configuration signals. All timings are specified respective to the rising edge of SYSCLK.

CLOCK AC SPECIFICATIONS

The following table provides the clock AC timing specifications as defined in Figure 4.

CLOCK AC TIMING SPECIFICATIONS

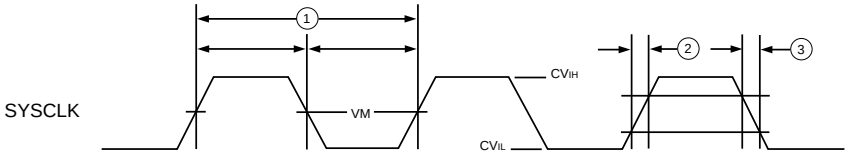
(V_{CC} = 3.3 ±5.0% V DC, T_A = -55°C to +125°C)

Num	Characteristics	80MHz		100MHz		Unit
		Min	Max	Min	Max	
	Processor Frequency (5)	40	80	50	100	MHz
	VCO Frequency (5)	100	200	100	200	MHz
	SYSCLK (Bus) Frequency	16.67	66.67	16.67	66.67	MHz
1	SYSCLK Cycle Time	15.0	60.0	15.0	60.0	ns
2, 3	SYSCLK Rise and Fall Time (1)	–	2.0	–	2.0	ns
4	SYSCLK Duty Cycle Measured at 1.4V (3)	40.0	60.0	40.0	60.0	%
8	SYSCLK Jitter (2)	–	±150	–	±150	ps
9	Internal PLL Relock Time (3, 4)	–	100	–	100	µs

NOTES:

1. Rise and fall times for all SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter, and is guaranteed by design.
3. Timing is guaranteed by design and characterization, and is not tested.
4. PLL relock time is the maximum amount of time required for PLL lock after stable Vcc and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100µs) during the power-on reset sequence.
5. **Caution:** The SYSCLK frequency and Phase Lock Loop Configuration settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

FIG. 3 SYSCLK INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4V)

INPUT AC TIMING SPECIFICATIONS

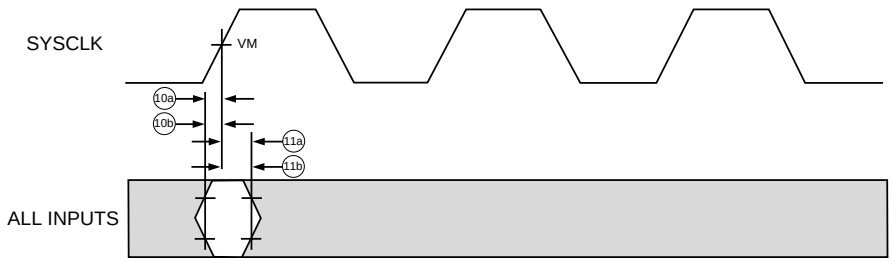
(V_{CC} = 3.3 ±5.0% V DC, T_A = -55°C to +125°C)

Num	Characteristics	80MHz		100MHz		Unit
		Min	Max	Min	Max	
10a	Address/Data/Transfer Attribute Inputs valid to SYSCLK (input setup) (2)	3.0	–	2.5	–	ns
10b	All other inputs to SYSCLK (input setup) (3)	5.0	–	4.5	–	ns
10c	Mode Select Inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$) (4, 5, 6, 7)	8 x t_{SYS}	–	8 x t_{SYS}	–	ns
11a	SYSCLK to Address/Data/TransferAttribute Inputs invalid (input hold) (2)	1.0	–	1.0	–	ns
11b	SYSCLK to all other inputs invalid (input hold) (3)	1.0	–	1.0	–	ns
11c	$\overline{\text{HRESET}}$ to Mode Select Inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$) (4, 6, 7)	0	–	0	–	ns

NOTES:

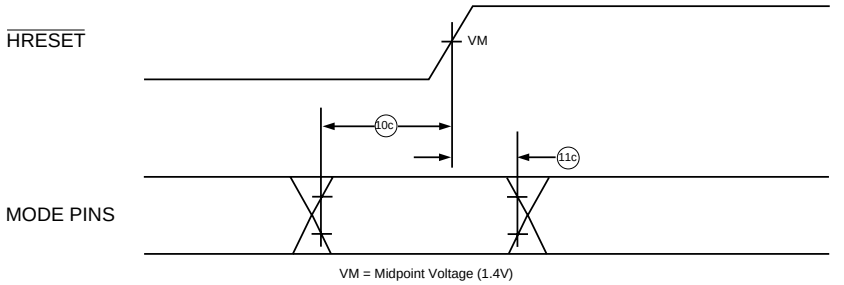
1. All input specifications are measured from TTL level (0.8 or 2.0V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 5.
2. Address/Data/Transfer Attribute Input Signals are composed of the following: A0-A31, AP0-AP3, TT0-TT4, TC0-TC1, $\overline{\text{TBST}}$, TSIZ0-TSIZ2, GBL, DH0-DH31, DP0-DP7.
3. All other input signals are composed of the following: $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, BG, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$. See Figure 4.
5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds (ns).
6. These values are guaranteed by design but not tested.
7. This specification is for configuration mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100µs) during the power-on reset sequence.

FIG. 4 INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4V)

FIG. 5 MODE SELECT INPUT TIMING DIAGRAM



OUTPUT AC TIMING SPECIFICATIONS

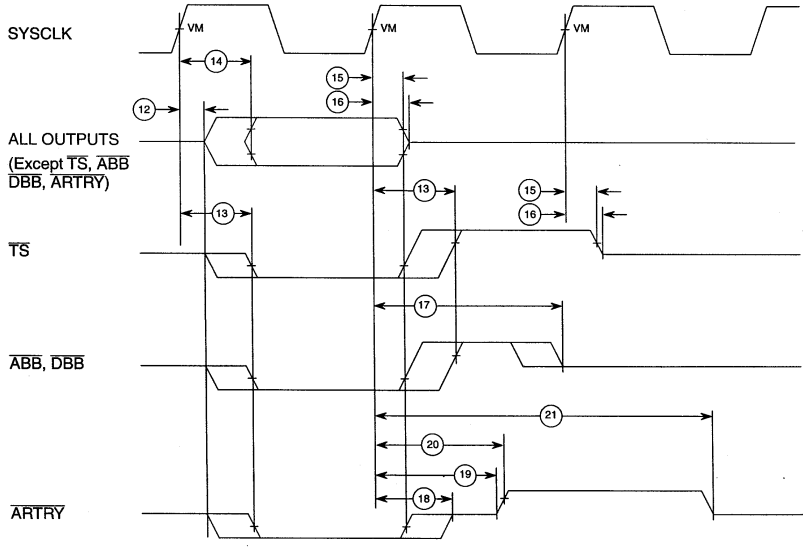
(V_{CC} = 3.3 ±5.0% V DC, T_A = -55°C to +125°C)

Num	Characteristics	80MHz		100MHz		Unit
		Min	Max	Min	Max	
12	SYSCLK to output driven (Output Enable Time)	1.0	–	1.0	–	ns
13a	SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (4)	–	11.0	–	10.0	ns
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (6)	–	10.0	–	9.0	ns
14a	SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (4)	–	13.0	–	12.0	ns
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) (6)	–	11.0	–	10.0	ns
15	SYSCLK to output invalid (output hold) (3)	1.5	–	1.5	–	ns
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	9.5	–	8.5	ns
17	$\overline{SYSCLK}$ to $\overline{ABB}$, $\overline{DBB}$ high impedance after precharge (5, 7)	–	1.2	–	1.2	t_{SYS}
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	9.0	–	8.0	ns
19	SYSCLK to $\overline{ARTRY}$ precharge enable (3, 5, 8)	0.2 x t_{SYS} +1.0	–	0.2 x t_{SYS} +1.0	–	ns
20	Maximum delay to $\overline{ARTRY}$ precharge (5, 8)	–	1.2	–	1.2	t_{SYS}
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge (5, 8)	–	2.25	–	2.25	t_{SYS}

NOTES:

1. All output specifications are measured from 1.4V of the rising edge of SYSCLK to the TTL level (0.8V or 2.0V) of the signal in question. Both input and output timings are measured at the pin. See Figure 5.
2. All maximum timing specifications assume C_L = 0 pF.
3. This minimum parameter assume C_L = 0 pF.
4. SYSCLK to output valid (5.5V to 0.8V) includes the extra delay associated with discharging the external voltage from 5.5V to 0.8V instead of from Vcc to 0.8V (5V CMOS levels instead of 3.3V CMOS levels).
5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Output signal transitions from GND to 2.0V or Vcc to 0.8V.
7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{SYSCLK}.
8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}.

FIG. 6 OUTPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4 V)

JTAG AC TIMING SPECIFICATIONS (INDEPENDENT OF SYSCLK)

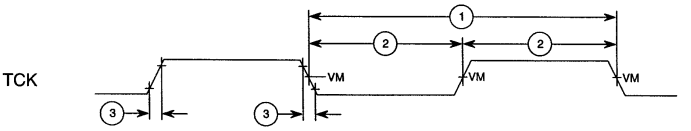
(V_{CC} = 3.3 ±5.0% V DC, T_A = -55°C to +125°C)

Num	Characteristic	Min	Max	Units
	TCK Frequency of Operation	0	16	MHz
1	TCK Cycle Time	62.5	–	ns
2	TCK Clock Pulse Width measured at 1.4V	25	–	ns
3	TCK Rise and Fall Times	0	3	ns
4	$\overline{TRST}$ Setup Time to TCK Rising Edge (1)	13	–	ns
5	$\overline{TRST}$ Assert Time	40	–	ns
6	Boundary Scan Input Data Setup Time (2)	6	–	ns
7	Boundary Scan Input Data Hold Time (2)	27	–	ns
8	TCK to Output Data Valid (3)	4	25	ns
9	TCKK to Output High Impedance (3)	3	24	ns
10	TMS, TDI Data Setup Time	0	–	ns
11	TMS, TDI Data HoldTime	25	–	ns
12	TCK to TDO Data Valid	4	24	ns
13	TCK to TDO High Impedence	3	15	ns

NOTES:

1. TRST is an asynchronous signal. The setup time is for test purposes.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

FIG. 7 JTAG CLOCK INPUT TIMING DIAGRAM



VM = Midpoint Voltage (1.4 V)

FIG. 8 $\overline{\text{TRST}}$ TIMING DIAGRAM

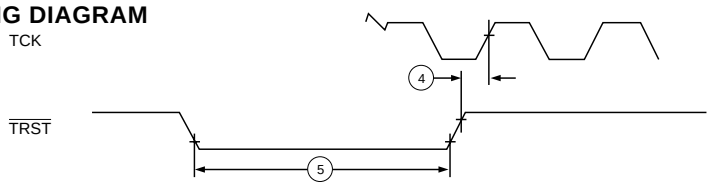


FIG. 9 BOUNDARY SCAN TIMING DIAGRAM

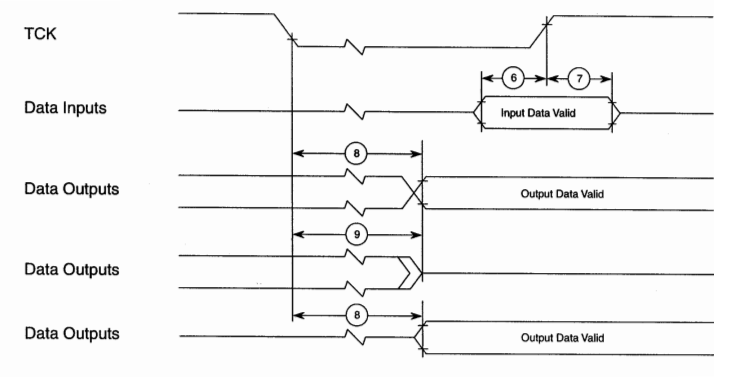
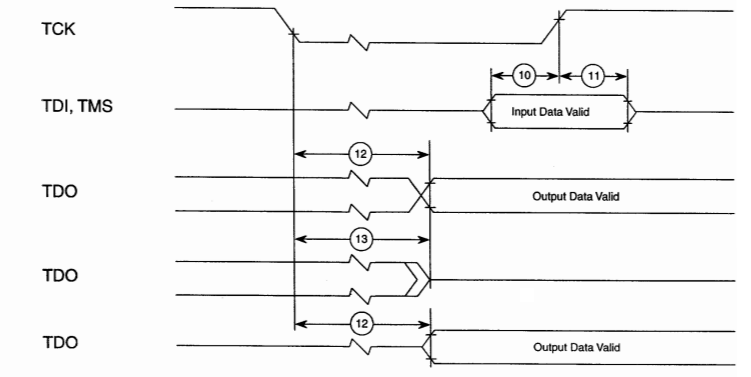
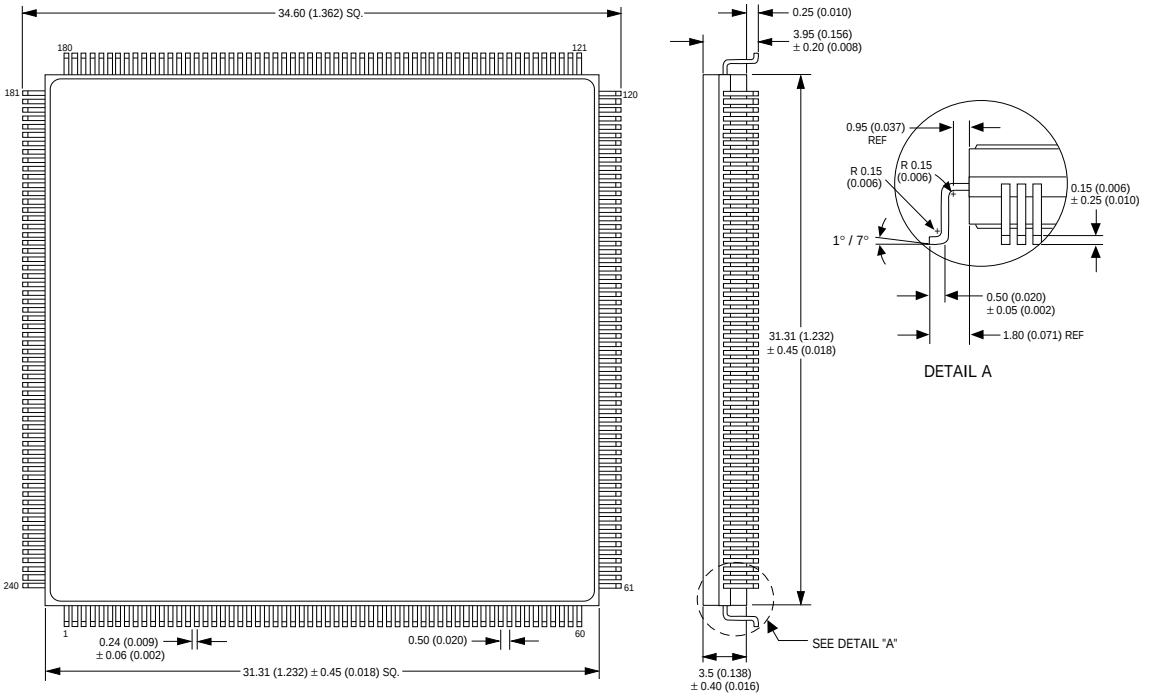


FIG. 10 TEST ACCESS PORT TIMING DIAGRAM



PACKAGE DIMENSION 240 PIN, CERAMIC QUAD FLAT PACK, CQFP (Q3)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION