512Kx36 Synchronous Pipeline Burst SRAM

*PRELIMINARY**

FEATURES

- Fast clock speed: 200, 166, 150 & 133MHz
- Fast access times: 2.5ns, 3.5ns, 3.8ns & 4.0ns
- Fast $\overline{\text{OE}}$ access times: 2.5ns, 3.5ns, 3.8ns 4.0ns
- Available with 1.5ns setup and 0.5ns hold times or 1.0ns setup and hold times.
- Single +3.3V power supply (V$_{DD}$)
- Seperate +3.3V or +2.5V isolated output buffer supply (V$_{DDQ}$)
- Snooze Mode for reduced-power standby
- Single-cycle deselect
- Common data inputs and data outputs
- Individual Byte Write control and Globa Write
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 119-bump BGA package
- Low capacitive bus loading
- Available in either single $\overline{\text{CE}}$ or three CE configuration
- IEEE 1149.1 JTAG Compatible Boundary Scan (available on single $\overline{\text{CE}}$ version only)

DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 16Mb SyncBurst SRAMs integrate two 512K x 18 SRAMs into a single BGA package to provide 512K x 36 configuration. All synchronous inputs pass through registers controlled by a positive - edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{\text{CE}}$), burst control inputs ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$, $\overline{\text{ADV}}$), byte write enables ($\overline{\text{BW}}$0-3) and global write ($\overline{\text{GW}}$). Asynchronous inputs include the output enable ($\overline{\text{OE}}$), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. Write Cycles can be from one to four bytes wide, as controlled by the write control inputs. Burst operation can be initiated with either address status processor ($\overline{\text{ADSP}}$) or address status controller ($\overline{\text{ADSC}}$) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input ($\overline{\text{ADV}}$).

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1

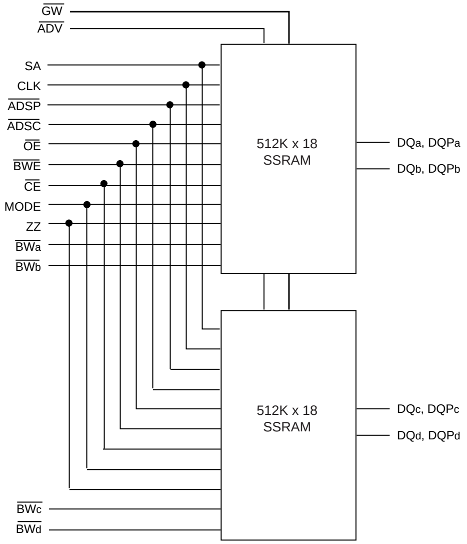
PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7
A	V$_{DDQ}$	SA	SA	$\overline{\text{ADSP}}$	SA	SA	V$_{DDQ}$
B	NC	SA	SA	$\overline{\text{ADSC}}$	SA	SA	NC
C	NC	SA	SA	V$_{DD}$	SA	SA	NC/$\overline{\text{CE}}_2$*
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	$\overline{\text{CE}}$	Vss	DQb	DQb
F	V$_{DDQ}$	DQc	Vss	$\overline{\text{OE}}$	Vss	DQb	V$_{DDQ}$
G	DQc	DQc	$\overline{\text{BWc}}$	$\overline{\text{ADV}}$	$\overline{\text{BWb}}$	DQb	DQb
H	DQc	DQc	Vss	$\overline{\text{GW}}$	Vss	DQb	DQb
J	V$_{DDQ}$	V$_{DD}$	NC	V$_{DD}$	NC	V$_{DD}$	V$_{DDQ}$
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{\text{BWd}}$	NC	$\overline{\text{BWa}}$	DQa	DQa
M	V$_{DDQ}$	DQd	Vss	$\overline{\text{BWE}}$	Vss	DQa	V$_{DDQ}$
N	DQd	DQd	Vss	SA1	Vss	DQa	DQa
P	DQd	DQPd	Vss	SA0	Vss	DQPa	DQa
R	NC	SA	MODE	V$_{DD}$	NC	SA	NC/CE$_2$*
T	NC	NC	SA	SA	SA	NC	ZZ
U	V$_{DDQ}$	TMD	TDI	TCK	TDO	NC	V$_{DDQ}$

* Enable on pins C7 and R7 are options for the three CE density only.

BLOCK DIAGRAM



PIN DESCRIPTION

x36	Symbol	Type	Description
CLK	Input	Pulse	The system clock input. All of the SSRAM inputs are sampled on the rising edge of the clock.
4P 4N 2A, 2C, 2R, 2B 3A, 3B, 3C, 3T 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R	SA_0 SA_1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 5G 3G 3L	BWa BWb BWc BWd	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. BWa controls DQa's and DQPa; BWb controls DQb's and DQPb; BWc controls DQc's and DQPc; BWd controls DQd's and DQPd.
4M	BWE	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
4H	GW	Input	Global Write: This active LOW input allows a full 36- bit WRITE to occur independent of the BWE and BWx lines and must meet the setup and hold times around the rising edge of CLK.
4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	CE	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP. CE is sampled only when a new external address is loaded.
7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
4F	OE	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
4G	ADV	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV must be HIGH at the rising edge of the first clock after an ADSP cycle is initiated.
4A	ADSP	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC, but dependent upon CE, CE_2 and CE_2. ADSP is ignored if CE is HIGH. Powerdown state is entered if CE_2 is LOW or CE_2 is HIGH .
4B	ADSC	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE is LOW. ADSC is also used to place the chip into power-down state when CE is HIGH.
3R	MODE	Input	Mode: This input selects the burst sequence. A LOW on MODE selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa's; Byte "b" is DQb's; Byte "c" is DQc's; Byte "d" is DQd's. Input data must meet setup and hold times around rising edge of CLK.
6P 6D 2D 2P	DQPa DQPb DQPc DQPd	Input/ Output	Byte "a" Parity is DQPa; Byte "b" Parity is DQPb; Byte "c" Parity is DQPc; Byte "d" Parity is DQPd.
2J, 4C, 4J, 4R, 5R, 6J	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M 1U 7A, 7F, 7J, 7M, 7U	V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Ground: GND.
2U	TMS	Input	Scan Test Mode Select
3U	TDI	Input	Scan Test Data In
4U	TDO	Output	Scan Test Data Out
5U	TCK	Input	Scan Test Clock

INTERLEAVED BURST TABLE (MODE = NC OR HIGH)

First Address External	Second Address Internal	Third Address Internal	Fourth Address Internal
X...X00	X...X01	X...X10	X...X11
X...X01	X....X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

INTERLEAVED BURST TABLE (MODE = LOW)

First Address External	Second Address Internal	Third Address Internal	Fourth Address Internal
X...X00	X...X01	X...X10	X...X11
X...X01	X....X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

Function	Address Used	$\overline{CE}$	$\overline{CE_2}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle,Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle,Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle,Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle,Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle,Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE,Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTES:

1. X means "Don't Care." — means active LOW. H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means any one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE - WRITE COMMANDS

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte “a”	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BWa}$ through $\overline{BWd}$, any one or more bytes may be written.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply relative to V_{SS}	-0.5V to +4.6V
Voltage on V_{DDQ} Supply relative to V_{SS}	-0.5V to +4.6V
VIN (DQx)	-0.5V to V_{DDQ} +0.5V
VIN (Inputs)	-0.5V to V_{DD} +0.5V
Storage Temperature (BGA)	+55°C to +125°C
Short Circuit Output Current	100 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1)Voltage	V_{IH}		2.0	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.8	V	1
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq V_{DD}$	-1.0	1.0	mA	2
Ouptut Leakage Current	I_{LO}	Output(s) disabled, $0V \leq V_{IN} \leq V_{DD}$	-1.0	1.0	mA	
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	V	1
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	0.4	V	1
Supply Voltage	V_{DD}		3.135	3.6	V	1
Isolated Output Buffer Supply	V_{DDQ}		3.134	3.6	V	

NOTES:
1. All voltages referenced to Vss (GND).
2. MODE has an internal pull-up, and input leakage = ±10IiA.

DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	200* MHz	166 MHz	150 MHz	133 MHz	Units	Notes
Power Supply Current: Operating	I_{DD}	Device selected; All inputs $\leq V_{IL}$ or 3 V_{IH}; Cycle time 3 t_{KC} MIN; V_{DD} = MAX; Outputs open		TBD	700	620	560	mA	1,2,3
CMOS Standby	I_{SB2}	Device deselected; V_{DD} = MAX; All inputs $\leq V_{SS}$ + 0.2 or V_{DD} - 0.2; All inputs static; CLK frequency = 0	10	20	20	20	20	mA	2,3
TTL Standby	I_{SB3}	Device deselected; V_{DD} = MAX; All inputs $\leq V_{IL}$ or V_{IH}; All inputs static; CLD frequency = 0	20	40	40	40	40	mA	2,3
Clock Running	I_{SB4}	Device deselected; V_{DD} = MAX; All inputs $\leq V_{SS}$ + 0.2 or V_{DD} -0.2; Cycle time 3 t_{KC} MIN	80	TBD	180	160	140	mA	2,3

** Advanced Information*

NOTES:
1. I_{DD} is specified with no output current and increases with faster cycle times. IDD increases with faster cycle times and greater output loading.
2. “Device deselected” means device is in power-down mode as defined in the truth table. “Device selected” means device is active (not in power-down mode).
3. Typical values are measured at 3.3V, 250°C and 10ns cycle time.

BGA CAPACITANCE

Description	Conditions	Symbol	Typ	Max	Units	Notes
Control Input Capacitance	T_A = 25°C; f = 1MHz	C_I	3	4	pF	1
Input/Output Capacitance (DQ)	T_A = 25°C; f = 1MHz	C_O	4	5	pF	1
Address Capacitance	T_A = 25°C; f = 1MHz	C_A	3	5	pF	1
Clock Capacitance	T_A = 25°C; f = 1MHz	C_{CK}	2.5	4	pF	1

NOTES:
1. This parameter is sampled.

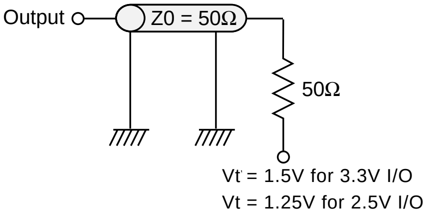
AC CHARACTERISTICS (WED2DL36513V)

Parameter	Symbol	200MHz Min	200MHz Max	166MHz Min	166MHz Max	150MHz Min	150MHz Max	133MHz Min	133MHz Max	Units
Clock										
Clock Cycle Time	t_{KC}	5.0		6.0		6.6		7.5		ns
Clock Frequency	t_{KF}		200		166		150		133	MHz
Clock HIGH Time	t_{KH}	2.0		2.4		2.6		2.6		ns
Clock LOW Time	t_{KL}	2.0		2.4		2.6		2.6		ns
Output Times										
Clock to output valid	t_{KQ}		2.5		3.5		3.8		4.0	ns
Clock to output invalid (2)	t_{KQX}	1.5		1.25		1.25		1.5		ns
Clock to output on Low-Z (2,3,4)	t_{KQLZ}	0		0		0		0		ns
Clock to output in High-Z (2,3,4)	t_{KQHZ}		3.0		3.5		3.8		4.0	ns
OE to output valid (5)	t_{OEQ}		2.5		3.5		3.8		4.0	ns
OE to output in Low-Z (2,3,4)	t_{OELZ}	0		0		0		0		ns
OE to output in High Z (2,3,4)	t_{OEHZ}		2.5		3.5		3.8		4.0	ns
Setup Times										
Address (6,7)	t_{AS}	1.5		1.5		1.5		1.5		ns
Address status (ADSC, ADSP) (6,7)	t_{ADSS}	1.5		1.5		1.5		1.5		ns
Address advance (ADV) (6,7)	t_{AAS}	1.5		1.5		1.5		1.5		ns
Write signals (BWa-BWd, BWE, GW) (6,7)	t_{WS}	1.5		1.5		1.5		1.5		ns
Data-in (6,7)	t_{DS}	1.5		1.5		1.5		1.5		ns
Chip enables (CE, CE2, CE2) (6,7)	t_{CES}	1.5		1.5		1.5		1.5		ns
Hold Times										
Address (6,7)	t_{AH}	0.5		0.5		0.5		0.5		ns
Address status (ADSC, ADSP) (6,7)	t_{ADSH}	0.5		0.5		0.5		0.5		ns
Address advance (ADV) (6,7)	t_{AAH}	0.5		0.5		0.5		0.5		ns
Write Signals (BWa-BWd, BWE, GW) (6,7)	t_{WH}	0.5		0.5		0.5		0.5		ns
Data-in (6,7)	t_{DH}	0.5		0.5		0.5		0.5		ns
Chip Enables (CE, CE2, CE2) (6,7)	t_{CEH}	0.5		0.5		0.5		0.5		ns

NOTES:

1. Test conditions as specified with the output loading as shown in Figure 1 for 3.3V 1/0 and Figure 3 for 2.5V 1/0 unless otherwise noted.
2. This parameter is measured with output load as shown in Figure 2 for 3.3V 1/0 and Figure 4 for 2.5V 1/0.
3. This parameter is sampled.
4. Transition is measured ±500mV from steady state voltage.
5. OE is a “Don’t Care” when a byte write enable is sampled LOW.
6. A WRITE cycle is defined by at least one byte write enable LOW and ADSP HIGH for the required setup and hold times. A READ cycle Is defined by all byte write enables HIGH and ADSC or ADV LOW or ADSP LOW for the required setup and hold times.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP or ADSC is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP or ADSC is LOW to remain enabled.

OUTPUT LOADS



AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	3.3V I/O	2.5V I/O	Unit
Input Pulse Levels	V_{SS} to 3.0	V_{SS} to 2.5	V
Input Rise and Fall Times	1	1	ns
Input Timing Reference Levels	1.5	1.25	V
Output Timing Reference Levels	1.5	1.25	V
Output Load	See figure, at left		

AC CHARACTERISTICS (WED2DL36513AV)

	Symbol	200MHz		166MHz		150MHz		133MHz		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock										
Clock Cycle Time	t_{KC}	5.0		6.0		6.6		7.5		ns
Clock Frequency	t_{KF}		200		166		150		133	MHz
Clock HIGH Time	t_{KH}	2.0		2.4		2.6		2.6		ns
Clock LOW Time	t_{KL}	2.0		2.4		2.6		2.6		ns
Output Times										
Clock to output valid	t_{KQ}		2.5		3.5		3.8		4.0	ns
Clock to output invalid (2)	t_{KQX}	1.25		1.25		1.25		1.5		ns
Clock to output on Low-Z (2,3,4)	t_{KQLZ}	0		0		0		0		ns
Clock to output in High-Z (2,3,4)	t_{KQHZ}		3.0		3.5		3.8		4.0	ns
$\overline{\text{OE}}$ to output valid (5)	t_{OEQ}		2.5		3.5		3.8		4.0	ns
$\overline{\text{OE}}$ to output in Low-Z (2,3,4)	t_{OELZ}	0		0		0		0		ns
$\overline{\text{OE}}$ to output in High Z (2,3,4)	t_{OEHZ}		2.5		3.5		3.8		4.0	ns
Setup Times										
Address (6,7)	t_{AS}	1.0		1.0		1.0		1.0		ns
Address status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$) (6,7)	t_{ADSS}	1.0		1.0		1.0		1.0		ns
Address advance ($\overline{\text{ADV}}$) (6,7)	t_{AAS}	1.0		1.0		1.0		1.0		ns
Write signals ($\overline{\text{BWa}}$-$\overline{\text{BWd}}$, $\overline{\text{BWE}}$, $\overline{\text{GW}}$) (6,7)	t_{WS}	1.0		1.0		1.0		1.0		ns
Data-in (6,7)	t_{DS}	1.0		1.0		1.0		1.0		ns
Chip enables ($\overline{\text{CE}}$, $\overline{\text{CE}}_2$, CE_2) (6,7)	t_{CES}	1.0		1.0		1.0		1.0		ns
Hold Times										
Address (6,7)	t_{AH}	1.0		1.0		1.0		1.0		ns
Address status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$) (6,7)	t_{ADSH}	1.0		1.0		1.0		1.0		ns
Address advance ($\overline{\text{ADV}}$) (6,7)	t_{AAH}	1.0		1.0		1.0		1.0		ns
Write Signals ($\overline{\text{BWa}}$-$\overline{\text{BWd}}$, $\overline{\text{BWE}}$, $\overline{\text{GW}}$) (6,7)	t_{WH}	1.0		1.0		1.0		1.0		ns
Data-in (6,7)	t_{DH}	1.0		1.0		1.0		1.0		ns
Chip Enables ($\overline{\text{CE}}$, $\overline{\text{CE}}_2$, CE_2) (6,7)	t_{CEH}	1.0		1.0		1.0		1.0		ns

NOTES:

1. Test conditions as specified with the output loading as shown in Figure 1 for 3.3V 1/0 and Figure 3 for 2.5V 1/0 unless otherwise noted.
2. This parameter is measured with output load as shown in Figure 2 for 3.3V 1/0 and Figure 4 for 2.5V 1/0.
3. This parameter is sampled.
4. Transition is measured ±500mV from steady state voltage.
5. $\overline{\text{OE}}$ is a "Don't Care" when a byte write enable is sampled LOW.
6. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{\text{ADSP}}$ HIGH for the required setup and hold times. A READ cycle Is defined by all byte write enables HIGH and $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ LOW or $\overline{\text{ADSP}}$ LOW for the required setup and hold times.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is LOW to remain enabled.

SNOOZE MODE

SNOOZE MODE is a low-current, “power-down “ mode In which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is notguaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		2(t_{KC})	ns	1
ZZ inactive to input sampled		t_{RZZ}	2(t_{KC})		ns	1
ZZ active to snooze current		t_{ZZI}		2(t_{KC})	ns	1
ZZ inactive to exit snooze current		t_{RZZI}			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

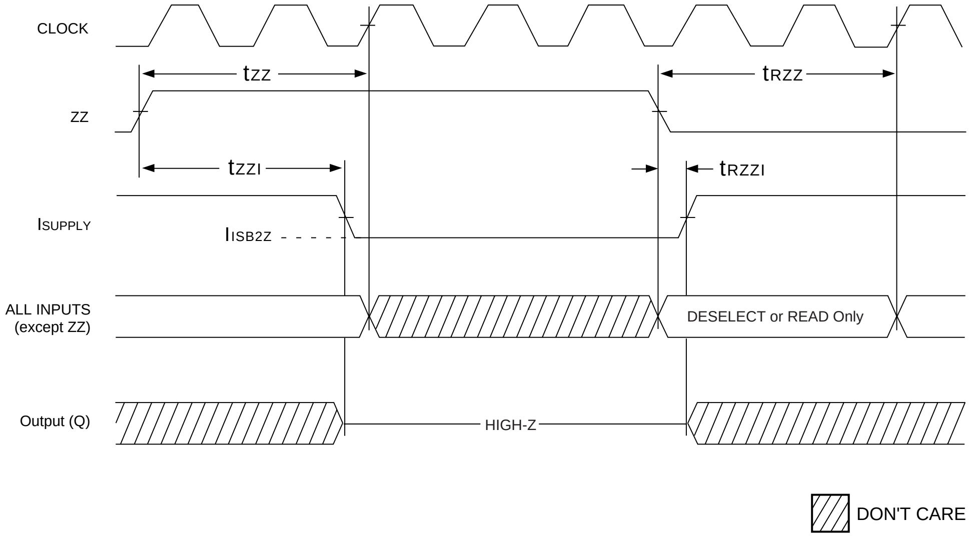
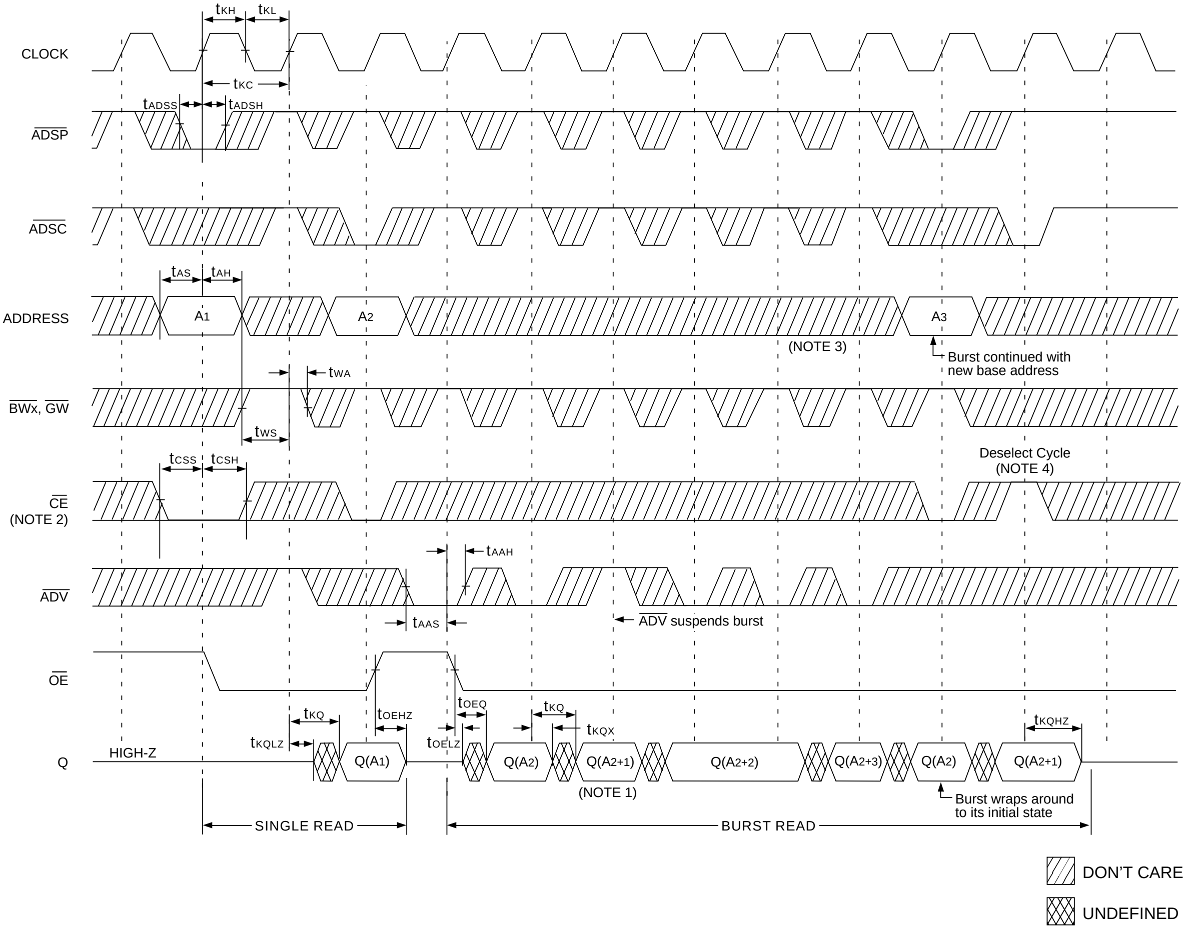


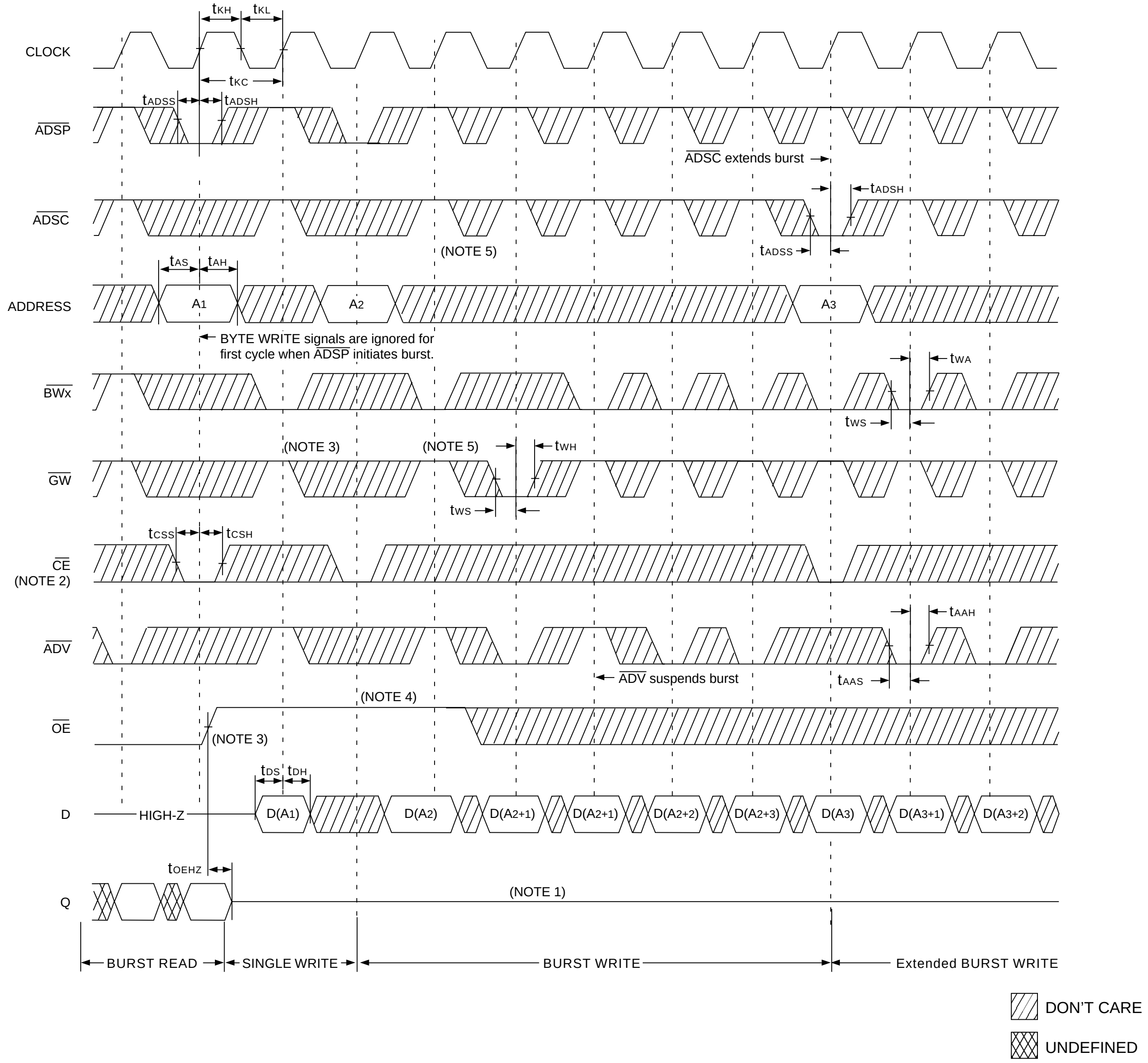
FIG. 3 READ TIMING DIAGRAM



NOTES:

1. Q (A2) refers to output from address A2. Q (A2+1) refers to output from the next internal burst address following A2.
2. $\overline{\text{CE}}$2 and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE}}$2 is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, CE2 is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within one clock cycle after deselect.

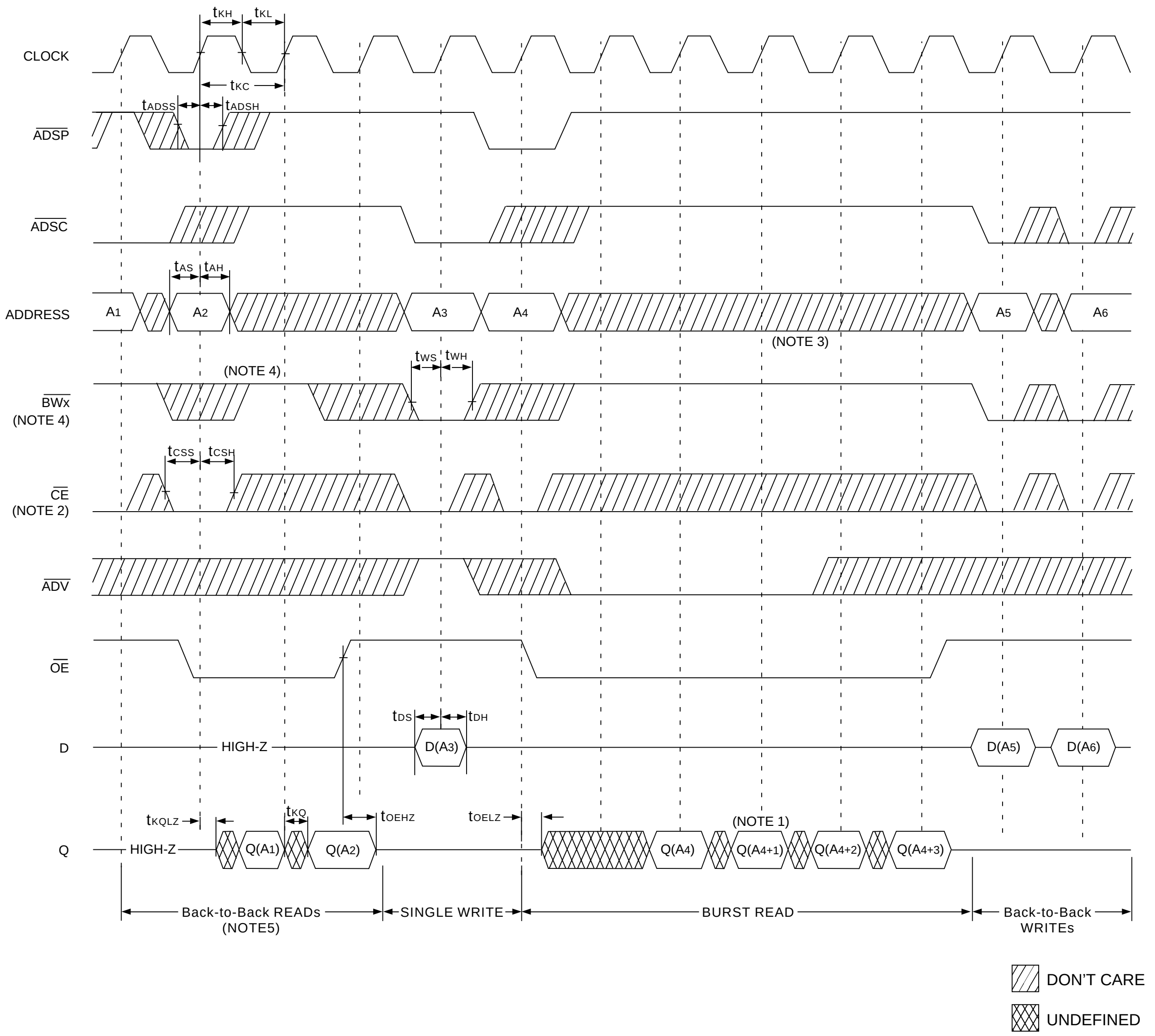
FIG. 4 WRITE TIMING DIAGRAM



NOTES:

1. D (A2) refers to output from address A2. D (A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}$2 and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}$2 is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}$2 is HIGH and $\overline{CE}$2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contentin for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the load address.
5. Full-width WRITE can be initiated by $\overline{GW}$ LOW, or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BWa}$, - $\overline{BWd}$ LOW. Timing is shown assuming that the device was not enabled before entering into its sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

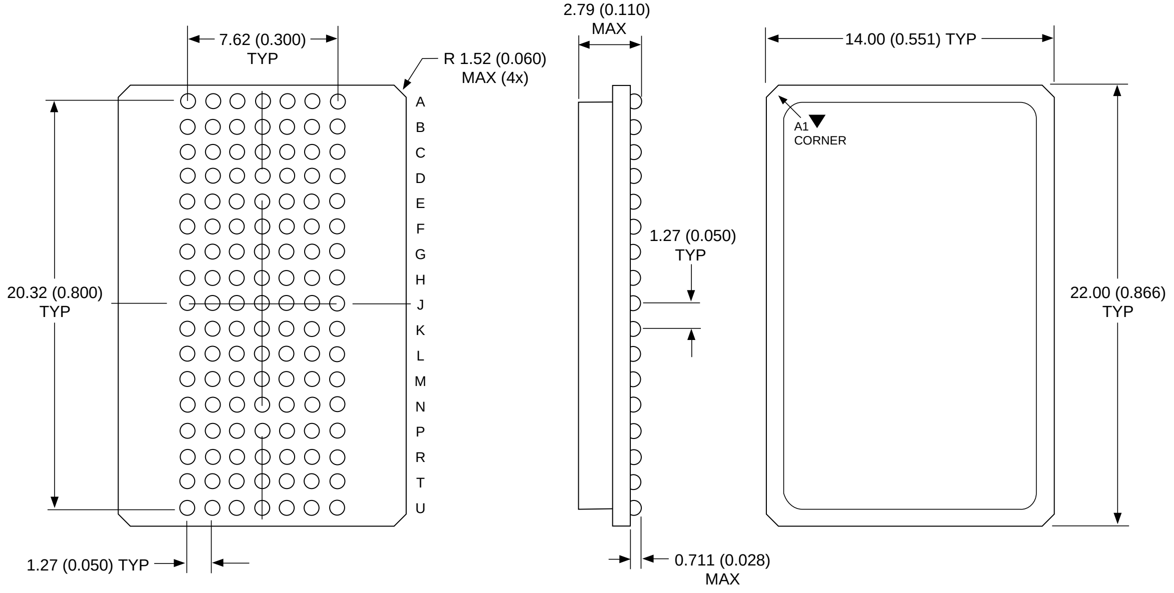
FIG. 5 READ/WRITE TIMING DIAGRAM



NOTES:

1. Q (A4) refers to output from address A4. Q (A4+1) refers to output from the next internal burst address following A4.
2. $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.
3. The data bus Q remains in High-Z following a WRITE cycle unless ADSP, ADSC or ADV cycle is performed.
4. $\overline{\text{GW}}$ is HIGH.
5. Back-to-back READs may be controlled by either ADSP or ADSC.

PACKAGE DIMENSION: 119 BUMP PBGA



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

512Kx36, Single CE

Part Number	Config.	tKQ (ns)	Clock (MHz)	Package No.
Commercial Temp Range (0°C to 70°C)				
WED2DL36513V25BC	512Kx36	2.5	200	435
WED2DL36513V35BC	512Kx36	3.5	166	435
WED2DL36513V38BC	512Kx36	3.8	150	435
WED2DL36513V40BC	512Kx36	4.0	133	435
Industrial Temp Range (-40°C to +85°C)*				
WED2DL36513V38BI	512Kx36	3.8	150	435
WED2DL36513V40BI	512Kx36	4.0	133	435

** Advanced Information*

512Kx36, Three CE

Part Number	Config.	tKQ (ns)	Clock (MHz)	Package No.
Commercial Temp Range (0°C to 70°C)				
WED2DL36514V25BC	512Kx36	2.5	200	435
WED2DL36514V35BC	512Kx36	3.5	166	435
WED2DL36514V38BC	512Kx36	3.8	150	435
WED2DL36514V40BC	512Kx36	4.0	133	435
Industrial Temp Range (-40°C to +85°C)				
WED2DL36514V38BI	512Kx36	3.8	150	435
WED2DL36514V40BI	512Kx36	4.0	133	435

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WED2DL36513AV38BC	512Kx36	3.8	150	435
WED2DL36513AV40BC	512Kx36	4.0	133	435
Industrial Temp Range (-40°C to +85°C)*				
WED2DL36513AV38BI	512Kx36	3.8	150	435
WED2DL36513AV40BI	512Kx36	4.0	133	435

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WED2DL36514AV38BC	512Kx36	3.8	150	435
WED2DL36514AV40BC	512Kx36	4.0	133	435
Industrial Temp Range (-40°C to +85°C)				
WED2DL36514AV38BI	512Kx36	3.8	150	435
WED2DL36514AV40BI	512Kx36	4.0	133	435

** Advanced Information*