General Description

The EDI7F324XDNSN and EDI7F2324XDNSN are organized as one and two banks of 4M x 32 respectively. The modules are based on Intel's E28F320J3, 4M x 8 / 2M x 16 device family. Both modules offer access times of 120-150ns

Features

- 4M x 32 and 2 x 4M x 32 Densities
- Based on Intel's Strataflash (J3) family of Flash Devices
  - E28F320J3
- (32) 128Kb Erase Blocks (Symetrical)
- High Performance Interface Async Page Mode Reads
  - 100/25 ns Read Access Time
- 2.7V - 3.6V Vcc Operation
- 128 bit Protection Register;
  - 64 bit Unique Device Identifier
  - 64 bit User Programmable OTP Cells
- Common Flash Interface (CFI)
- Scaleable Command Set (SCS)
- 32 byte Write Buffer, 32M Total Erase Cycles
  - 100,000 Erase Cycles per Block
- Package
  - 80 pin SIMM

Capacitance

		4M x 32	*2 x 4M x 32*	
Parameter	***Sym***	***Max***	***Max***	***Unit***
Address Lines	CA	35	70	pf
Data Lines	CDQ	15	30	pf
Chip & Write Enable Lines	CG	15	30	pf
Output Enable Lines	CG	35	70	pf

Pin Configurations

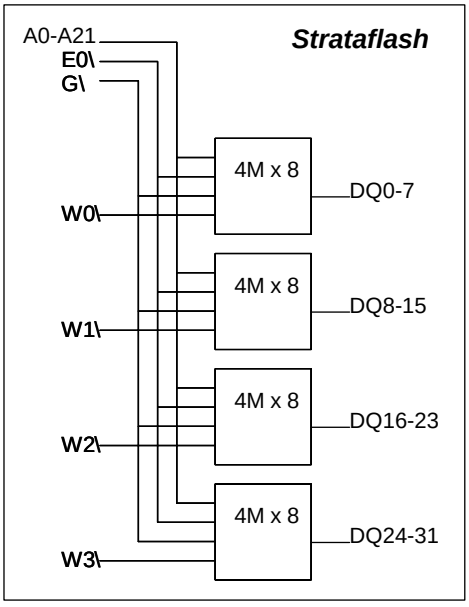
PIN#	P- NAME	PIN#	P- NAME	PIN#	P- NAME	PIN#	P- NAME
1	VSS	21	NC	41	A11	61	DQ9
2	VCC	22	NC	42	A10	62	DQ8
3	NC	23	*	43	A9	63	DQ7
4	G\	24	*	44	A8	64	DQ6
5	W0\	25	VSS	45	A7	65	DQ5
6	W1\	26	DQ29	46	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2\	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	A21	51	A1	71	NC
12	DQ20	32	A20	52	A0	72	VCC
13	DQ21	33	A19	53	W3\	73	PD1
14	DQ22	34	A18	54	VSS	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	VSS

*** SIMM DENSITY**

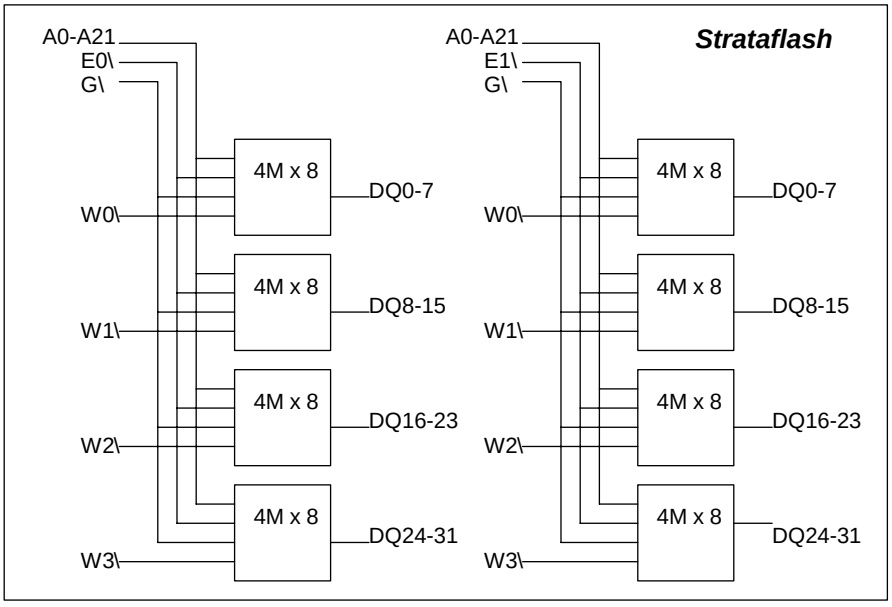
16MB PIN 24=E0\ PIN 23=NC
32MB PIN 24=E0\ PIN 23=E1\

Functional Block

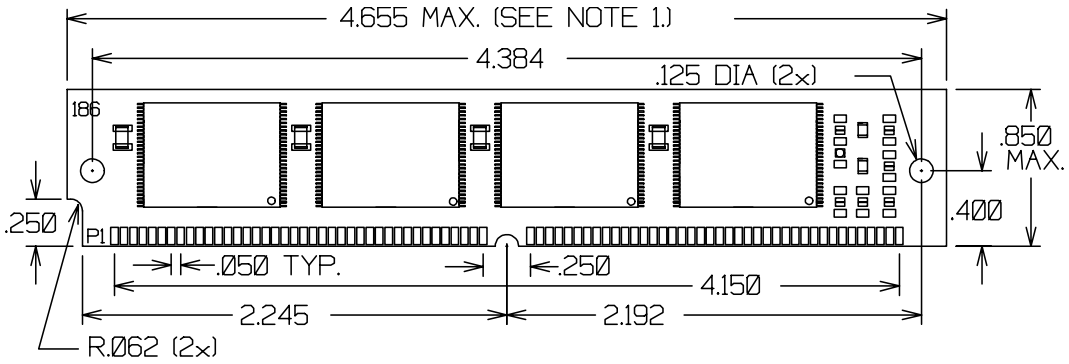
WED7F324DNSN; 4M x 32



WED7F2324XDNSN; 2 x 4M x 32



Mechanical



NOTE: 1.) THE MAXIMUM DIMENSION TO BE MEASURED WITHOUT INCLUDING THE BREAKAWAY AREA.

Module Configuration and Speed via Presence Detect

Module Speed Identification

Max Access Time	Presence Detect Pin Identification			*Order Config Standard / Options*
	PD5	PD6	PD7	
Underfined	*1*	*1*	*1*	***Standard***
45 ns	*0*	*1*	*1*	
55 ns	*1*	*0*	*1*	
70 ns	*0*	*0*	*1*	
90 ns	*1*	*1*	*0*	
120 ns	*0*	*1*	*0*	***Customer Option*** S-Spec
150 ns	*1*	*0*	*0*	***Customer Option*** S-Spec
200 ns	*0*	*0*	*0*	

unavailable

Module Configurator - Presence Detect Pins

Module Organization	*Device Density*	*# of Dev*	*Module Capacity*	*PD1*	*PD2*	*PD3*	*PD4*
4M x 32	32Mb	4	16MB	*0*	*1*	*1*	*1*
8M x 32	32Mb	8	32MB	*1*	*0*	*1*	*1*

Ordering Information

16Megabyte

WED7F324XDNSN10C	4M X 32 MODULE @100ns BASED ON Intel E28F320J3 (10%Vcc); 80 PAD SIMM
WED7F324XDNSN12C	4M X 32 MODULE @120ns BASED ON Intel E28F320J3 (10%Vcc). 80 PAD SIMM
WED7F324XDNSN15C	4M X 32 MODULE @150ns BASED ON Intel E28F320J3 (10%Vcc), 80 PAD SIMM

32Megabyte

WED7F2324XDNSN10C	2 X 4M X 32 MODULE @100ns, BASED ON Intel E28F320J3 (10%Vcc), 80 PAD SIMM
WED7F2324XDNSN12C	2 X 4M X 32 MODULE @120ns, BASED ON Intel E28F320J3 (10%Vcc), 80 PAD SIMM
WED7F2324XDNSN15C	2 X 4M X 32 MODULE @150ns, BASED ON Intel E28F320J3 (10%Vcc), 80 PAD SIMM