



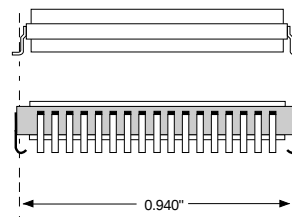
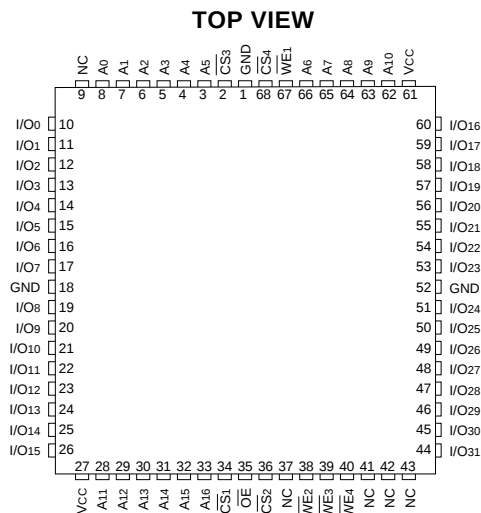
128Kx32 Radiation Hardened SRAM MODULE *ADVANCED**

FEATURES

- Access Time of 25ns
- Radiation Tolerant
 - Total Dose Hardness through 1×10^6 rad (SiO₂)
- Neutron Hardness through 1×10^{14} cm⁻²
- Dynamic and Static Transient Upset Hardness through 1×10^{11} rad (Si)/s
- Dose Rate Survivability through $< 1 \times 10^{12}$ rad (Si)/s
- Soft Error Rate of $< 1 \times 10^{-10}$ upsets/bit-day in Geosynchronous Orbit
- No Latchup
- Packaging:
 - 68 lead, Hermetic CQFP (G2S), 7.62mm (0.300") height (Package 515). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION FOR WS128K32-25G2SMX

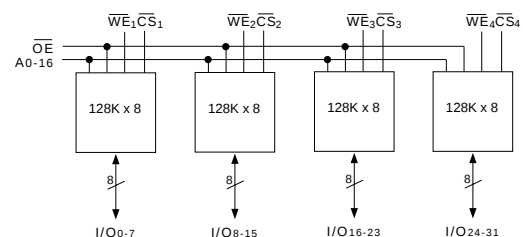


The White 68 lead G2S CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2S has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.3	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	6.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{\text{OE}}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	35	pF
$\overline{\text{WE}}$ ₁₋₄ capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{\text{CS}}$ ₁₋₄ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	35	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	$\overline{\text{CS}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		150	mA
Standby Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		30	mA
Output Low Voltage	V _{OL}	I _{OL} = 10mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -5.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions				Units
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{\text{CS}} = \text{V}_{\text{CC}} - 0.2\text{V}$	2.5		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 2.5V			4.0	mA



AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		Units
		Min	Max	
Read Cycle				
Read Cycle Time	t _{RC}	25		ns
Address Access Time	t _{AA}		25	ns
Output Hold from Address Change	t _{OH}	0		ns
Chip Select Access Time	t _{ACS}		25	ns
Output Enable to Output Valid	t _{OE}		9	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	2		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		9	ns

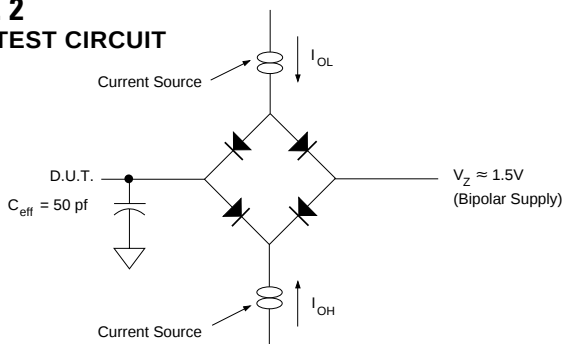
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		Units
		Min	Max	
Write Cycle				
Write Cycle Time	t _{WC}	25		ns
Chip Select to End of Write	t _{CW}	20		ns
Address Valid to End of Write	t _{AW}	20		ns
Data Valid to End of Write	t _{DW}	15		ns
Write Pulse Width	t _{WP}	20		ns
Address Setup Time	t _{AS}	0		ns
Address Hold Time	t _{AH}	0		ns
Output Active from End of Write	t _{OW} ¹	5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9	ns
Data Hold Time	t _{DH}	0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 3
TIMING WAVEFORM - READ CYCLE

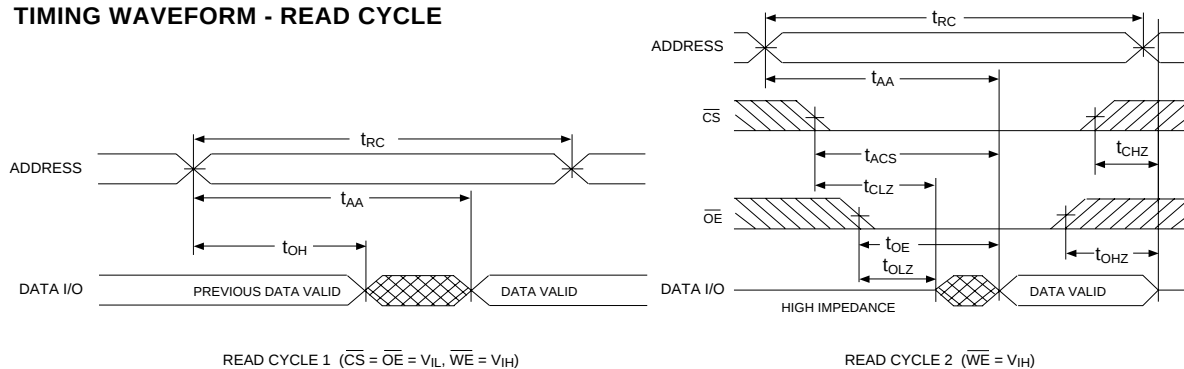


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

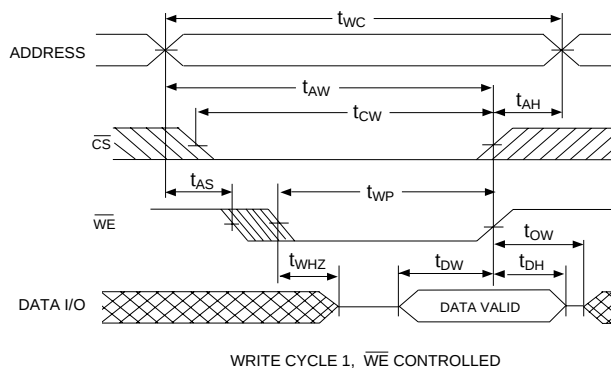
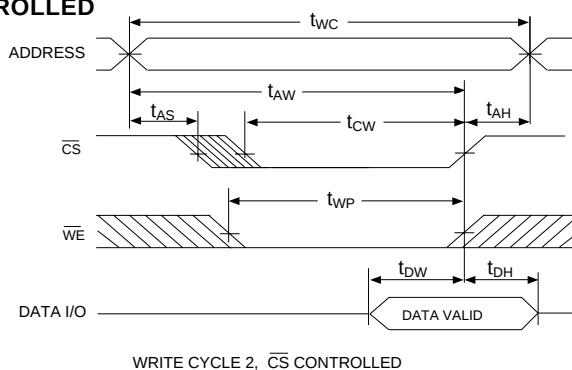
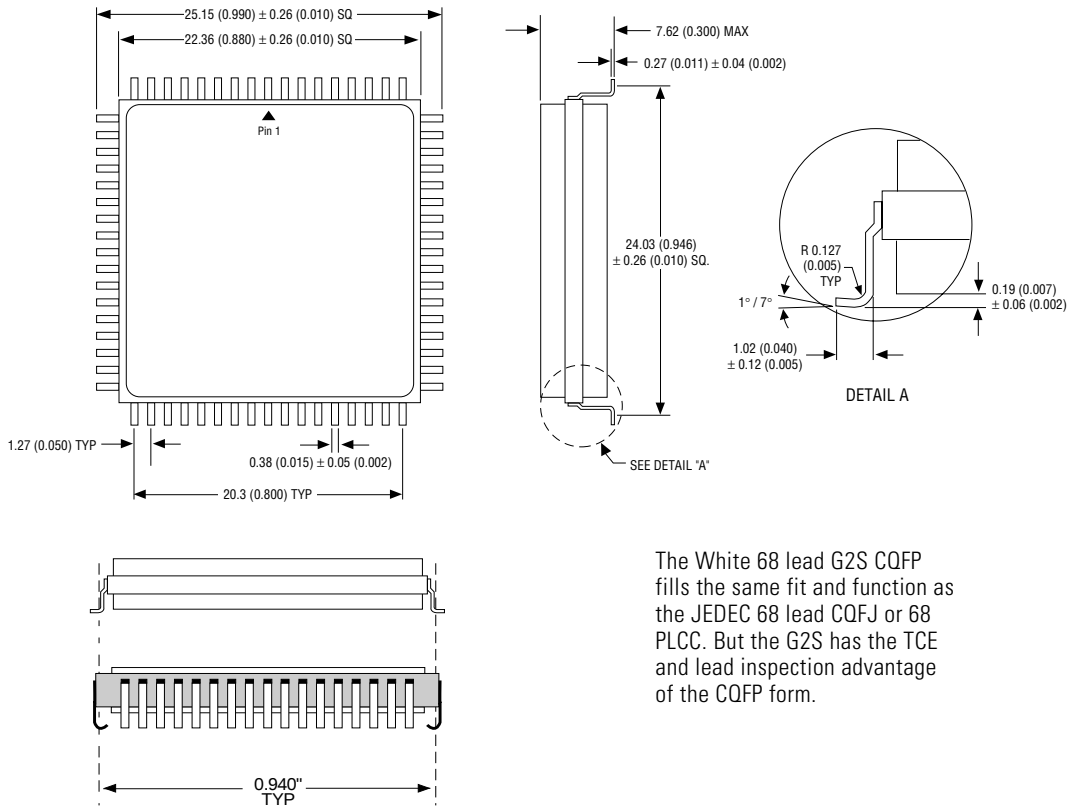


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



**PACKAGE 515: 68 LEAD CERAMIC QUAD FLAT PACK, CQFP (G2S)**

The White 68 lead G2S CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2S has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION****W S 128K 32 - 25 G2S M X X****LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

TOTAL DOSE HARDNESS:

N = No Radiation Screening

R = 1×10^5 rad (SiO₂)F = 3×10^5 rad (SiO₂)H = 1×10^6 rad (SiO₂)**DEVICE GRADE:**

M = Military Screened -55°C to +125°C

PACKAGE TYPE:

G2S = 0.300" high Ceramic Quad Flat Pack, CQFP (Package 515)

ACCESS TIME (ns)**ORGANIZATION, 128Kx32**

User configurable as 256Kx16 or 512Kx8

SRAM**WHITE MICROELECTRONICS**