Via Santa Maria Maddalena 12, 38100 Trento, Italy
tel. +39-0461-260 552 - fax + 39-0461-260 617
e-mail: info@neuricam.com; http: www.neuricam.com

VISTA 320 x 256 Digital Camera

PRELIMINARY DATA SHEET

Rel. 09/99

KEY FEATURES

- Full-frame CMOS active-pixel grey level image sensor with digital interface. It allows a complete digital camera to be assembled with only a few passive external components and does not require a frame grabber
- High dynamic range logarithmic response to light
- Non integrating continuos current reading pixels
- 320 x 256 -pixel resolution, 8-µm pitch square pixels, array size 2.560 x 2.048 mm^2, true random read operation
- Integrated video amplifier and analog-to-digital converter with 10-bit resolution
- Sensitivity adjustment circuit for operation under different illumination conditions
- Typical sensitivity: 2 lux with f=1.2
- Acquisition rate of 2 M pixels/s, corresponding to frame rates of up to 50 frames/s
- Implemented in CMOS technology for integration of functions which require several additional chips if conventional CCDs are employed
- Single 3.3-V operating voltage
- Low operating current: 50 mA typical
- Evaluation board of single-chip camera including interface to a personal computer and software drivers available.

APPLICATIONS

- Embedded cameras
- Industrial inspection and control
- Robotics
- 3D laser object reconstruction
- Automotive

GENERAL DESCRIPTION

VISTA is a monolithic full-frame active-pixel grey level image sensor with on-chip analog-to-digital converter and microprocessor interface. It uses conventional CMOS technology and integrates video amplifier, analog-to-digital converter and a bus interface. It permits the assembly of a compact and low-cost single-chip digital camera with the addition of only a few passive components. It can be connected directly to a microcomputer or a microcontroller and is easily adapted to user requirements. The digital camera VISTA can operate at a frame rate of up to 50 frame/s with a resolution of 10 bits.

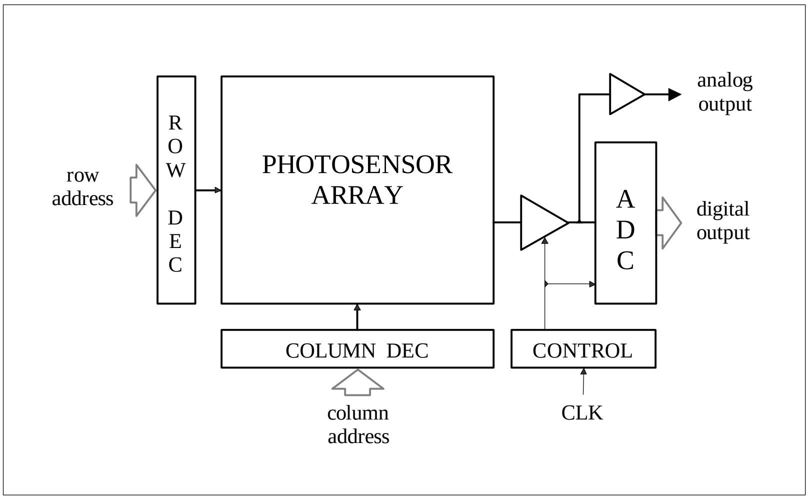


Fig. 1 Simplified camera block diagram.

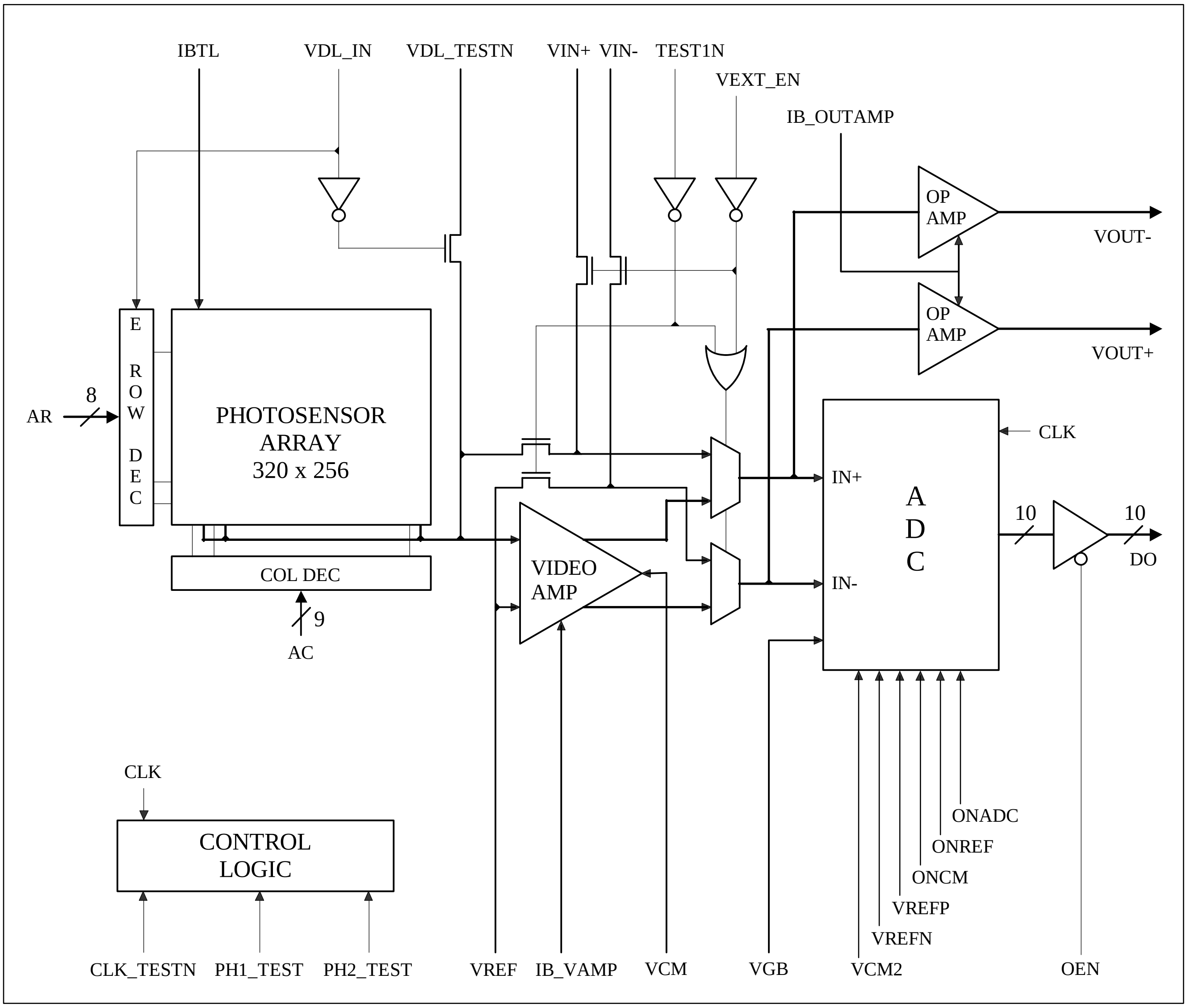
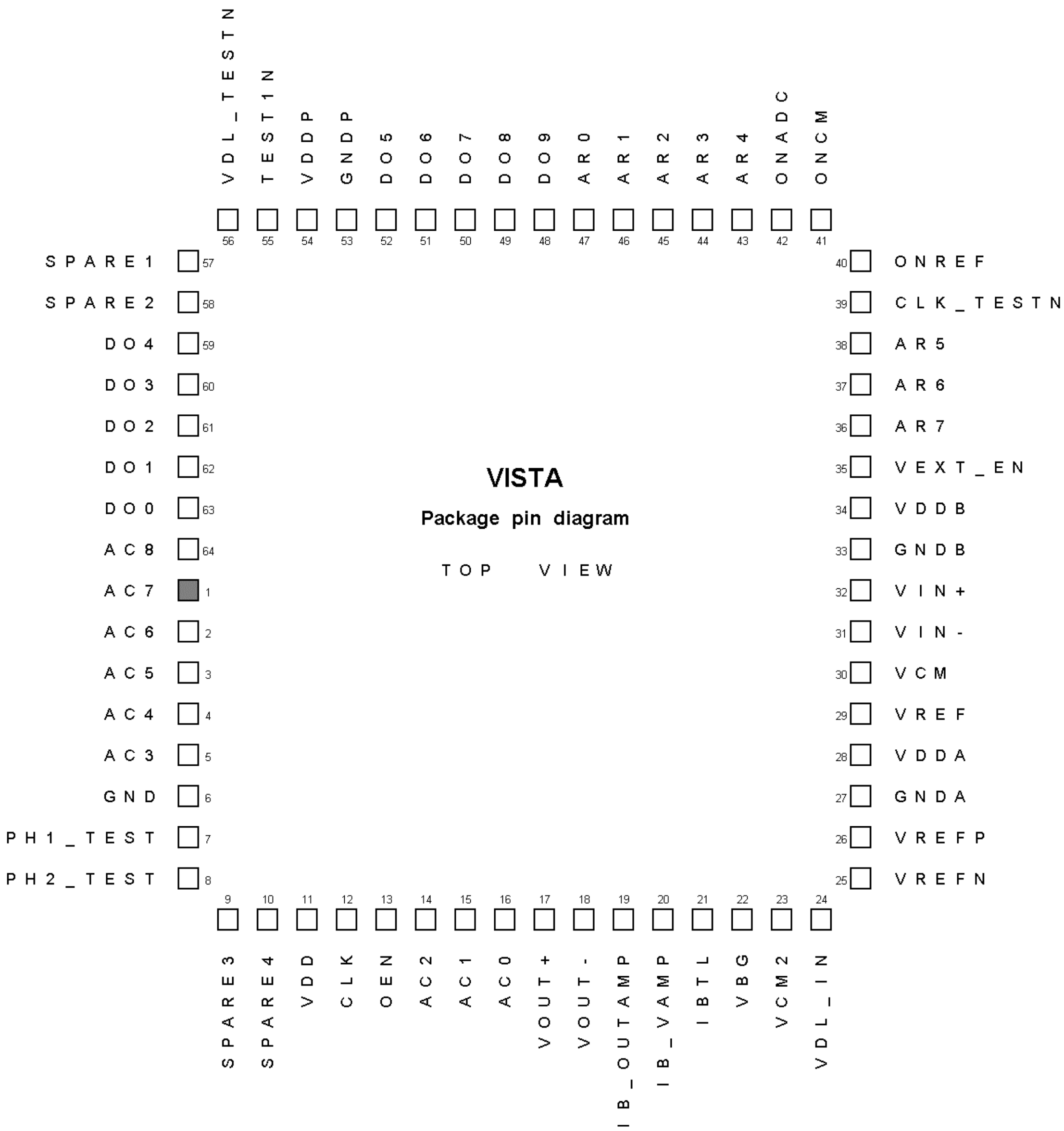


Fig. 2 Detailed camera block diagram.

PIN CONFIGURATION – 64 PIN LCC package with glass window



PIN DESCRIPTION

PIN NAME	TYPE	DESCRIPTION
DIGITAL		
CLK	DI	Clock - 20 MHz nominal - 50% duty cycle
AR[7:0]	DI	Row address bus. AR7 is the MSB
AC[8:0]	DI	Column address bus. AC8 is the MSB. Allowed range 0-319d
DO[9:0]	DO	Digital video data output. DO9 is the MSB. Bus can be trista-ted
OEN	DI	Output enable for DO output bus. Active low
VEXT_EN	DI	Enable VIN+, VIN- inputs. Active low
ANALOG		
IBTL	AI	Bitline bias current
IB_VAMP	AI	Video amplifier bias current
IB_OUTAMP	AI	Bias current for output amplifiers
VREF	AI	Video line reference voltage
VCM	AI	Common mode voltage for video amplifier and A/D converter
VBG	AI	Bandgap reference voltage or A/D converter
VIN+	AIO	External differential analog input, positive node (in mode 1). Video Line Output (in mode 3).
VIN-	AIO	External differential analog input, negative node (in mode 1). VREF Output (in mode 3).
VOUT+	AO	Differential analog output. Positive node
VOUT-	AO	Differential analog output. Negative node
TEST		
TEST1N	DI*	Bypass video amplifier. Active low
CLK_TESTN	DI*	Disconnect CLK input from PH1 PH2 generator and connect PH1_TEST, PH2_TEST. Active low
PH1_TEST	DI*	direct PH1 input
PH2_TEST	DI*	direct PH2 input
VDL_TESTN	DI*	Enable test of video line by enabling VDL_IN. Active low.
ONADC	DI*	Power down control for ADC. 1= normal operation
ONREF	DI*	Power down control for ADC reference generator. 1=normal operation
ONCM	DI*	Power down control for ADC common mode voltage generator. 1= normal operation
VDL_IN	AI*	Input to force video line with external voltage
VREFP	AIO*	Positive reference voltage of A/D converter
VREFN	AIO*	Negative reference voltage of A/D converter
VCM2	AIO*	Common mode voltage of A/D converter
SPARE1	DI*	Spare input pin
SPARE2	DI*	Spare input pin
SPARE3	DI*	Spare input pin
SPARE4	DI*	Spare input pin
SUPPLY		
GND	S	Digital ground
VDD	S	Digital supply voltage (3.3 V)
GNDA	S	Analog ground
VDDA	S	Analog supply voltage
GNDB	S	Ground for biasing of substrate
VDDB	S	Supply voltage for biasing of wells
GNDP	S	Ground for pad drivers
VDDP	S	Supply voltage for pad drivers

NOTES:

(1): D = digital line; A= analog line; I= input; O = output, S= supply
All digital inputs have TTL thresholds. All digital inputs have weak (70 Kohm) pull-ups. The pins marked with * can be connected only in CCC64 package.

Package:
64 CCC ceramic 40 mil pin pitch with glass window
Alternatively, 44 CC leadless ceramic 40 mil pitch with glass window

VISTA - Pin cross-reference list

ADDRESS		**OUTPUT**		**CONTROL**		**POWER**		**TEST**	
AC0	16	DOUT0	63	CLK	12	GND	6	TEST1N	55
AC1	15	DOUT1	62	OEN	13	VDD	11	CLK_TESTN	39
AC2	14	DOUT2	61	VEXT_EN	35			PH1_TEST	7
AC3	5	DOUT3	60			GNDA	27	PH2_TEST	8
AC4	4	DOUT4	59	IBTL	21	VDDA	28	VDL_TESTN	56
AC5	3	DOUT5	52	IBVAMP	20			ONADC	42
AC6	2	DOUT6	51	IBOUTAMP	19	GNDB	33	ONREF	40
AC7	1	DOUT7	50	VREF	29	VDDB	34	ONCM	41
AC8	64	DOUT8	49	VCM	30			VDL_IN	24
		DOUT9	48	VBG	22	GNDP	53	VREFP	26
AR0	47			VIN+	32	VDDP	54	VREFN	25
AR1	46			VIN-	31			VCM2	23
AR2	45			VOUT+	18				
AR3	44			VOUT-	17			SPARE1	57
AR4	43							SPARE2	58
AR5	38							SPARE3	9
AR6	37							SPARE4	10
AR7	36								

DETAILED DESCRIPTION

The architecture of the sensor is shown in figure 1. figure 2 shows detailed circuit diagram. The sensor operates in conjunction with a host microcomputer or microcontroller connected through a data bus carrying the video data to the processor, an address bus which defines the address of the pixel to be read and a set of control lines. As shown in Figure 1, the sensor comprises an array of 320 x 256 pixels, a video amplifier and 10-bit pipeline A/D converter. Single pixel selection is achieved by row and column decoders; the row decoder selects one row and the column decoder selects one of 320 pixels of this row and connects it to the video amplifier. The signal from the video amplifier is converted by the ADC to digital format. Control, timing and interface logic permits simple connection to a digital bus.

Photosensor array

The array of photodiodes converts the incoming light into a continuos current. No charge integration occurs in the sensor and therefore pixels can be read instantaneously at any time. The generated current of the photodiodes is linearly related to the intensity of the incident light. The biasing circuit of the photodiode posseses a logarithmic characteristic which results in an output voltage which is logarithmically correlated to the incident light. A voltage amplifier within the pixel connects the pixel to a vertical bit-line through a switch driven by the row decoder. Each bit-line is then connected to a global video-line through a set of switches driven by the column decoder. The pixels are square and have an area fill-factor of 0.85. Eight dummy rows and columns are placed on the four edges of the array for better photoresponse uniformity. The size of active portion of the photo-diode array is 2.560 mm x 2.048 mm. The 320 x 256 – pixel resolution can be used for ¼ VGA 320 x 240 resolution or for 256 x 256 resolution. Any other type of subsampling is achievable by simple addressing of the desired pixels.

Operation and timing of the camera

A control block provides all the internal timing signals. In a typical sequence of operation, row and column addresses AR AC are supplied by the user, so that a row of pixels is selected by the row decoder and the data from the selected column of pixels is put on the video amplifier via the video-line. The differential video amplifier amplifies the voltage signal of the video-line by a factor of 2. The resulting signal is then converted to digital by the analog-to-digital converter. The A/D conversion is performed by 10-bit pipeline A/D converter which supplies digital output data to the DO bus with a latency time of 5 clock cycles. The total latency from address valid to data output valid is 7 clock cycles.

In normal operation, one pixel is always selected by the binary value present on the two address busses and the camera continuously converts to digital the signal of this pixel. Both row and column address values should be changed on a rising clock edge only and remain stable for the rest of the cycle as they are not internally latched. A master clock CLK provides the timing for the whole circuit.

A set of voltage references and biasing currents are needed for the charge amplifiers and the analog-to-digital converters. These can be conveniently generated with external resistors from the supply voltage. A number of test lines are provided for production testing of the camera and can be ignored in normal operation.

ELECTRICAL CHARACTERISTICS

SENSITIVITY ADJUSTMENT

The following bias adjustment are adequate for typical operation:

IBTL(*)	100	uA
IB_VAMP(*)	200	uA
IB_OUTAMP(*)	1	mA
VREF	850	mV
VCM	1.50	V
VBG	1.25	V

VCM2(**)	VCM
VREFP(**)	VCM + 0.5 V
VREFN(**)	VCM – 0.5 V

(*) Currents are injected into the device.
(**) Necessary in test mode only. To be left floating during normal operating mode.

MODES DESCRIPTION

The modes of operation are summarised in the table below:

MODE	VEXT EN	TEST 1N	VDL TESTN	DESCRIPTION
0	1	1	1	Normal operating mode. Default, if test-pins are disconnected.
1	0	1	1	ADC differential inputs are connected to VIN+ and VIN- pins (used as inputs). The sensor array is disconnected.
2	1	0	x	Bypass Video Amplifier: the Video Line is connected directly to non-inverting input of ADC and VREF pin is connected to the inverting input.
3	0	0	x	Bypass Video Amplifier and Monitoring: besides being connected to the ADC, the Video Line is also connected to VIN+ pin and VREF is also connected to VIN- pin (used as outputs).
	x	x	0	Disable Sensor Array: the sensor array is turned off and the Video Line is connected to the VDL_IN pin. This function operates in modes 2 and 3.

Absolute maximum ratings

Operating temperature	-15 ºC to 110 ºC
Storage temperature	- 55 ºC to 150 ºC
Voltage on any pin to V_{SS}	- 0.5 to 4.5 V
Power dissipation	450 mW @ 20 MHz, 3.3V

Operating conditions

Symbol	Parameter	Min	Nom	Max	Units
T_A	Ambient temperature under bias	-15		110	ºC
V_{DD}	Digital supply voltage	3.0	3.3	3.6	V

F_{CLK}	Master clock frequency	0.01		20	MHz

DC characteristics (over specified operating conditions**)**

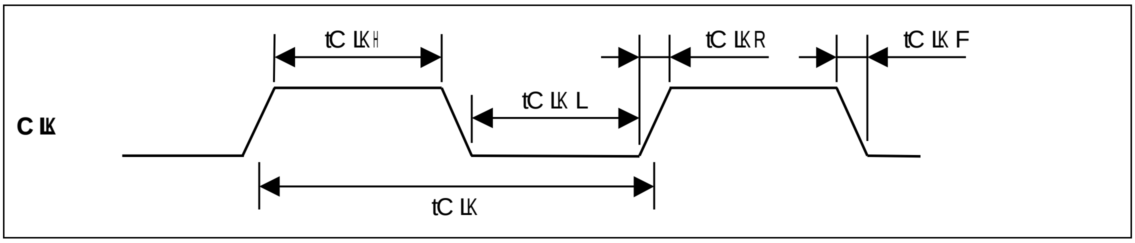
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input "high" voltage	TTL inputs	2.0		V_{DD} +0.5	V
V_{IL}	Input "low" voltage	TTL inputs	-0.5		0.8	V
I_{IH}	Input "high" current	TTL inputs			±10	µA
I_{IL}	Input "low" current	TTL inputs			±200	µA
I_{OT}	Output three-state leakage				±10	µA
V_{OH}	Output "high" voltage	IOH=-4 mA	V_{DD} - 0.4			V
V_{OL}	Output "low" voltage	I_{OL}=4 mA			0.4	V
FSLH	Output slew factor (low-to-high transition)				0.08	ns/pF
FSLL	Output slew factor (high-to-low transition)				0.05	ns/pF
R_{PU}	Weak pullup on TTL input			70		Kohm
CPIN	Pin capacitance (any pin to V_{SS})			5.0		pF
I_{DD}	Supply current (active mode)	f_{CLK}=20 MHz		50		mA

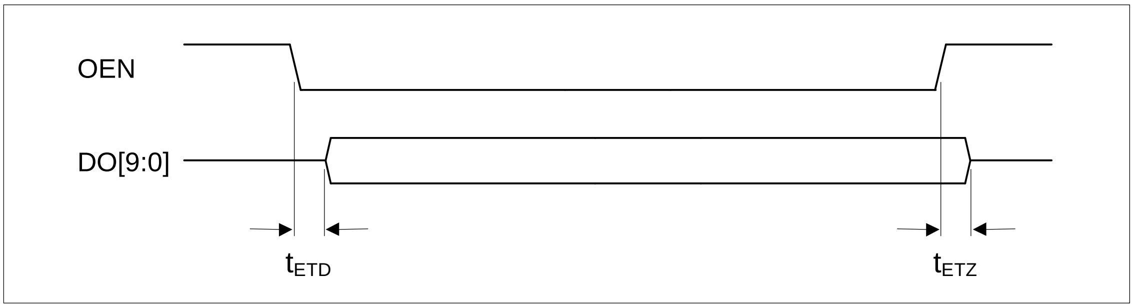
AC PARAMETERS (over specified operating conditions)

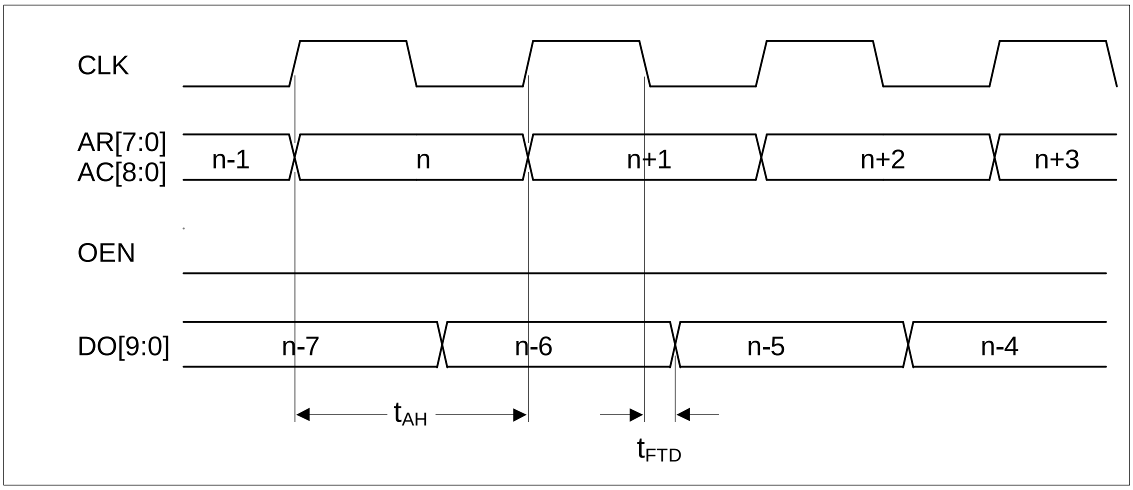
External clock drive

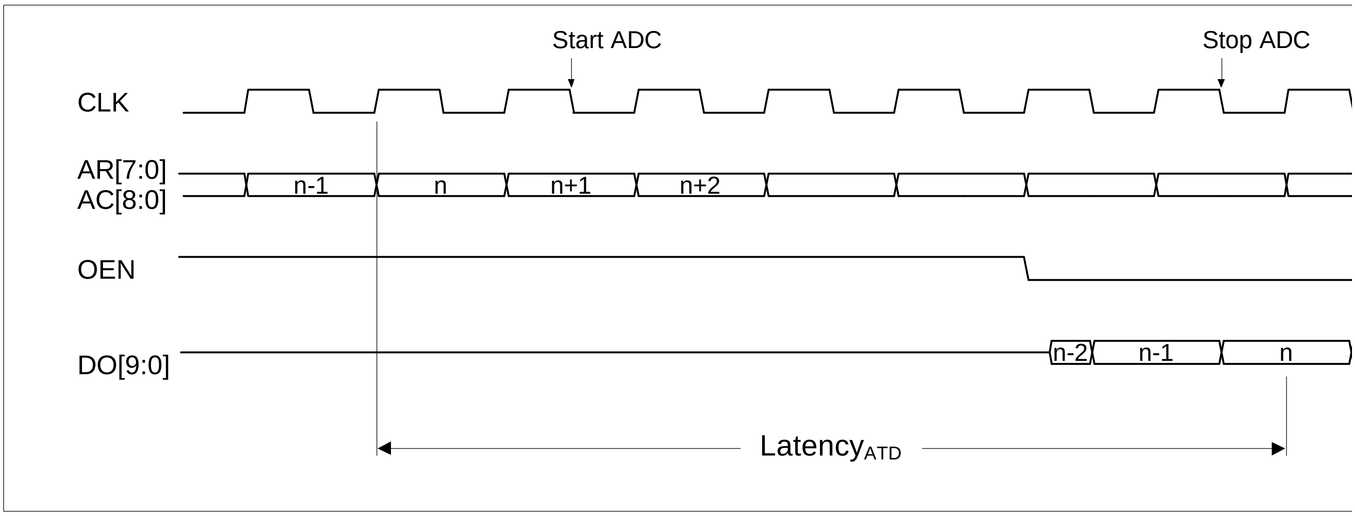
Symbol	Parameter	Min	Max	Units
$1/t_{CLK}$	Clock frequency	0.1	16	MHz
T_{CLK}	Clock period	62.5	10000	ns
T_{CLKH}	Clock high time	20		ns
T_{CLKL}	Clock low time	20		ns
T_{CLKR}	Clock rise time		20	ns
T_{CLKF}	Clock fall time		20	ns

External clock drive waveforms








Start ADC
Stop ADC
CLK
AR[7:0]
AC[8:0]
n-1
n
n+1
n+2
OEN
DO[9:0]
n-2
n-1
n
Latency ATD

ELECTRO-OPTICAL CHARACTERISTICS

Array resolution	320 x 256
Pixel pitch	8 µm x 8 µm
Fill factor	0.85
Array size	2.560 mm x 2.048 mm
ADC resolution	10 bit
Differential non-linearity	1/2 LSB
Integral non-linearity	1 LSB
Dark Current	t.b.d. nA/cm^2 @ 25 C
Peak Responsivity	0.2 A/W @ 600 nm
Sensitivity	2 lux (with f=1.2)
Fixed-pattern noise	t.b.d.
Dynamic Range	120 dB
Input referred noise	t.b.d. e^- @ 50 % saturation exposure, @ 650 nm

APPLICATIONS

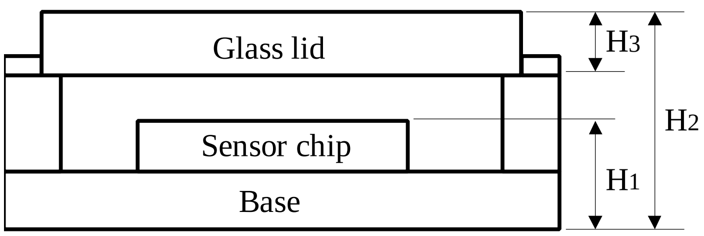
The complete digital camera only requires the sensor chip and a minimal number of external passive components for the generation of bias voltages and currents for the sensor, a simple power supply and a clock oscillator. Several of these functions are available in the host system and therefore do not require extra components in a typical system.
A possible connection to a microprocessor requiring only an external decoder is the following:

VISTA		**MICROPROCESSOR**
D[7:0]	<>	DATA[7:0]
A[1:0]	<	ADDRESS[1:0]
RDN	<	READN
WRN	<	WRITEN
CSN	<	DECODED HIGH ADDRESSES
EOF	>	INTERRUPT
LE	>	INTERRUPT
RESETN	<	RESETN

A typical programming sequence of the processor is the following:

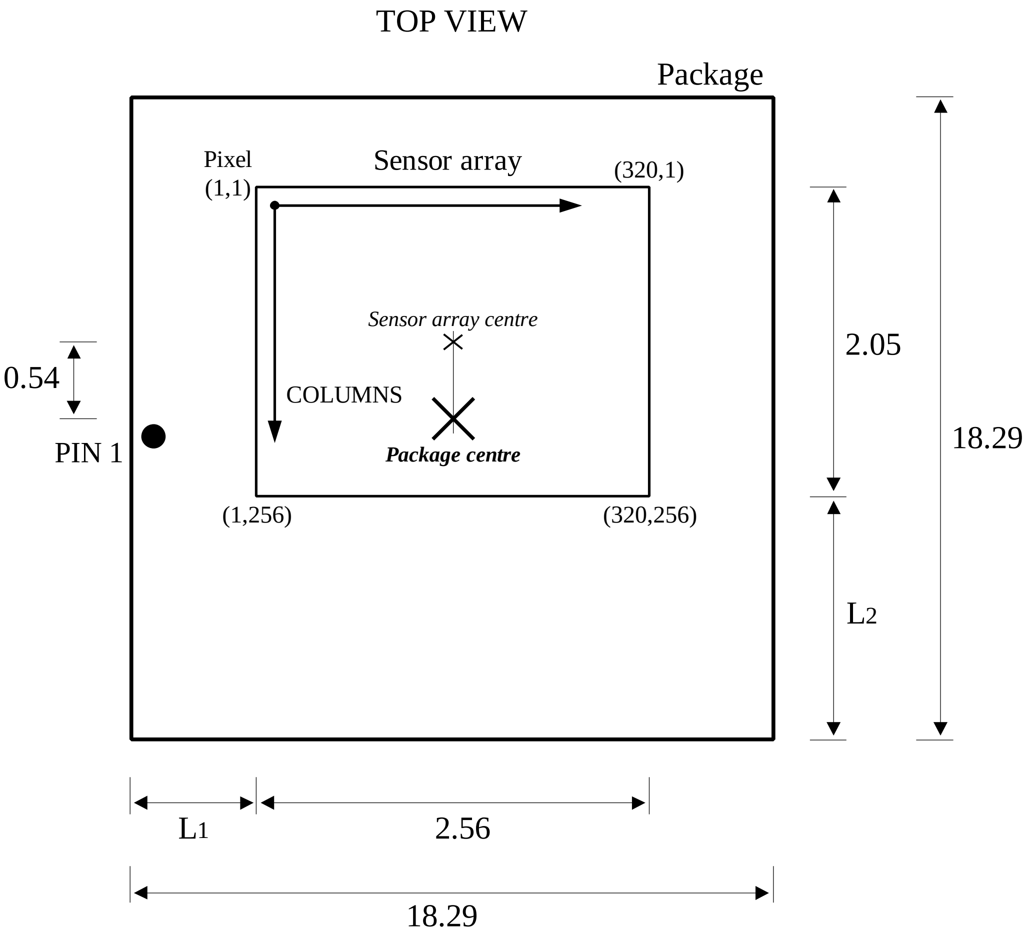
PACKAGE DETAILS

64-pin leadless LCC package with 40 mil pin pitch



Height of photosensor plane from seating plane of package H1 = 1.1 ± 0.1 mm
Total height of package including glass lid H2 = 2.0 mm
Thickness of glass lid H3 = 0.5 mm
Lid charactristics: optical glass; n=t.b.d .

SENSOR POSITION



Photosensor array position and orientation within package.
All dimensions are in mm.

L1 = 7.87 ± 0.1 mm
L2 = 8.66 ± 0.1 mm