

Description

The device is CMOS Synchronous Dynamic RAM organized as 524,288 words x 32 bits x 4 banks. It is fabricated with an advanced submicron CMOS technology and designed to operate from a singly 3.3V only power supply. It is packaged in 86-pin TSOPII package.

Features

- Single 3.3V ($\pm 0.3V$) power supply
- High speed clock cycle time : 5/6/7/8ns
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable $\overline{\text{CAS}}$ latency (2 & 3)
- Programmable burst length (1, 2, 4, 8 & Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Quad Internal banks controlled by BA0 & BA1 (Bank Select)
- Each Bank can operate simultaneously and independently
- LVTTTL compatible I/O interface
- Random column access in every cycle
- X32 organization
- Input/Output controlled by DQM
- 4,096 refresh cycles/64ms
- Burst termination by burst stop and precharge command
- Burst read/single write option

Pin Configuration

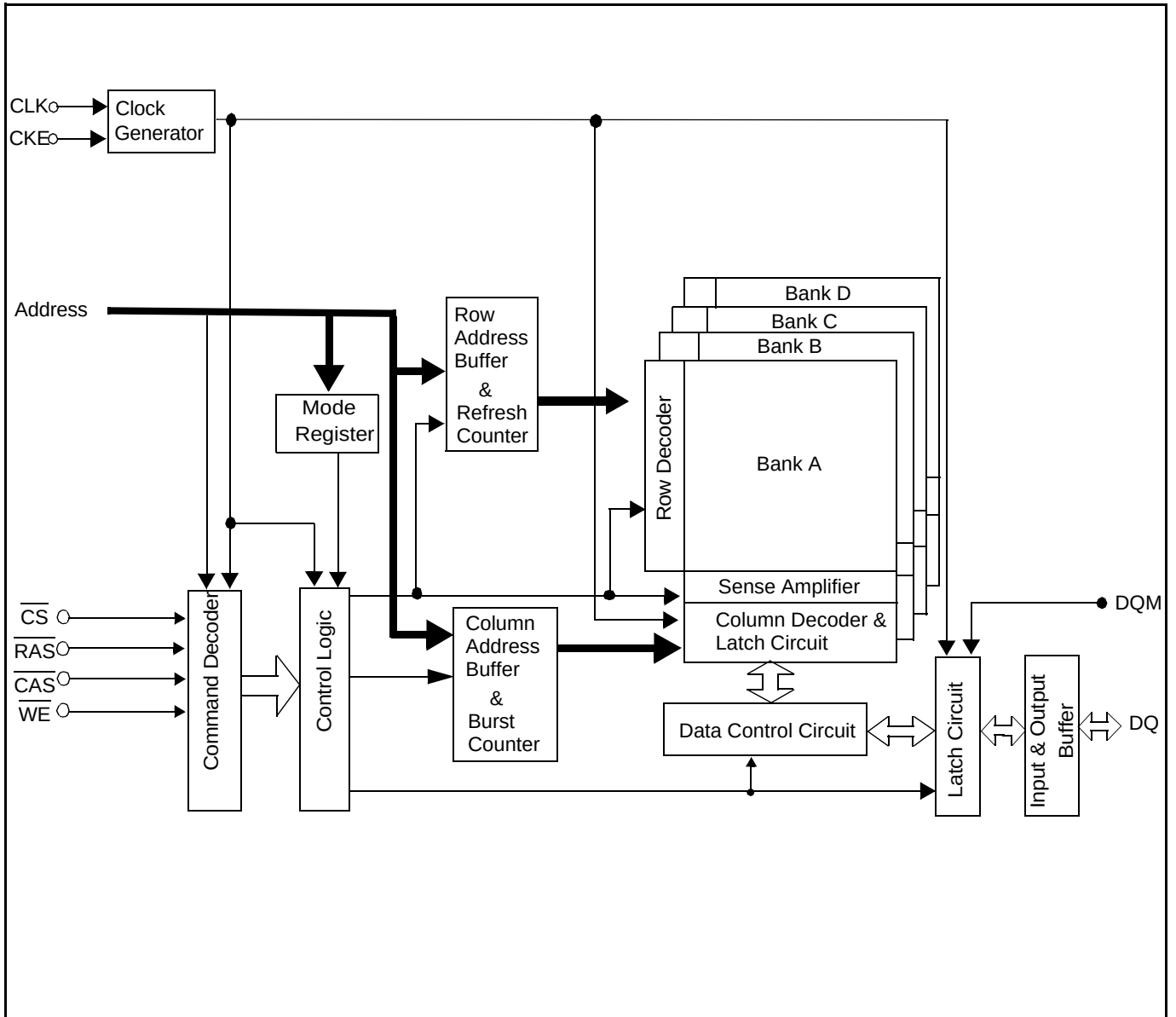
V _{DD}	1	86	V _{SS}
DQ0	2	85	DQ15
V _{DDQ}	3	84	V _{SSQ}
DQ1	4	83	DQ14
DQ2	5	82	DQ13
V _{SSQ}	6	81	V _{DDQ}
DQ3	7	80	DQ12
DQ4	8	79	DQ11
V _{DDQ}	9	78	V _{SSQ}
DQ5	10	77	DQ10
DQ6	11	76	DQ9
V _{SSQ}	12	75	V _{DDQ}
DQ7	13	74	DQ8
NC	14	73	NC
V _{DD}	15	72	V _{SS}
DQM0	16	71	DQM1
$\overline{\text{WE}}$	17	70	NC
$\overline{\text{CAS}}$	18	69	NC
$\overline{\text{RAS}}$	19	68	CLK
$\overline{\text{CS}}$	20	67	CKE
NC	21	66	A ₉
BA0	22	65	A ₈
BA1	23	64	A ₇
A10/AP	24	63	A ₆
A ₀	25	62	A ₅
A ₁	26	61	A ₄
A ₂	27	60	A ₃
DQM2	28	59	DQM3
V _{DD}	29	58	V _{SS}
NC	30	57	NC
DQ16	31	56	DQ31
V _{SSQ}	32	55	V _{DDQ}
DQ17	33	54	DQ30
DQ18	34	53	DQ29
V _{DDQ}	35	52	V _{SSQ}
DQ19	36	51	DQ28
DQ20	37	50	DQ27
V _{SSQ}	38	49	V _{DDQ}
DQ21	39	48	DQ26
DQ22	40	47	DQ25
V _{DDQ}	41	46	V _{SSQ}
DQ23	42	45	DQ24
V _{DD}	43	44	V _{SS}

86Pin TSOP (II)
(400mil x 875mil)
(0.5mm pin pitch)

Pin Description

Pin Name	Function	Pin Name	Function
A0 - A10	Address inputs Row address: RA0~RA10 Column address: CA0~CA7	BA0, BA1	Bank select
DQ0 ~ DQ31	Data input/output	DQM0-DQM3	DQs Mask enable
$\overline{\text{RAS}}$	Row address strobe	CLK	Clock input
$\overline{\text{CAS}}$	Column address strobe	CKE	Clock enable
$\overline{\text{WE}}$	Write enable	$\overline{\text{CS}}$	Chip select
V _{SS}	Ground	V _{DDQ}	Power for DQs (+3.3V)
V _{DD}	Power (+3.3V)	V _{SSQ}	Ground for DQs

Block Diagram



Absolute Maximum D.C. Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Supply voltage relative to Vss	V_{DD}, V_{DDQ}	-0.5 to +4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to +70	°C
Storage temperature	T_{STG}	-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause peumanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Maximum A.C. Operating Requirements for LVTTL Compatible

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	V_{IH}	2.0	$V_{DDQ} + 2.0$	V	2
Input Low Voltage	V_{IL}	$V_{SSQ} - 2.0$	0.8	V	2

Recommended DC Operating Conditions for LVTTL Compatible

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.0	-	$V_{DD} + 0.3$	V
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V

Capacitance

(Ta = 25°C, f = 1MHZ)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (all input pins except CLK pin)	C_{in}	2.5	3.50	4.5	pF	1
Input capacitance (CLK pin)	C_{CLK}	2.5	3.25	4.0	pF	1
Data input/output capacitance	$C_{I/O}$	4.0	5.25	6.5	pF	1

Notes : 1. Capacitance measured with effective capacitance measuring method.

2. The overshoot and undershoot voltage duration is $\leq 3ns$ with no input clamp diodes.

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	VG36643241A									
			-5		-6		-7		-8		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Operating current	I _{CC1}	Burst length = 1 One bank active t _{RC} ≤ t _{RC(MIN)} , I _{OL} = 0mA		150		140		130		120		
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL(MAX)} t _{CK} = 10ns		2		2		2		2	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX)} t _{CK} = ∞		2		2		2		2		
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH(MIN)} t _{CK} = 10ns. CS ≥ V _{IH(MIN)} Input signals are changed one time during 2 CLK cycles.		20		20		20		20	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN)} , t _{CK} = ∞ CLK ≤ V _{IL(MAX)} Input signals are stable.		10		10		10		10		
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL(MAX)} , t _{CK} = 10ns		5		5		5		5	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX)} , t _{CK} = ∞		5		5		5		5		
Active standby current in non power-down mode	I _{CC3N}	CKE ≥ V _{IH(MIN)} , t _{CK} = 10ns CS ≥ V _{IH(MIN)} Input signals are changed one time during 2CLKs.		40		40		40		40	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN)} t _{CK} = ∞ CLK ≤ V _{IL(MAX)} Input signals are stable.		30		30		30		30		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN)} , I _O = 0mA All banks Active		220		200		180		160	mA	2
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN)}		230		210		190		170	mA	3
Self refresh current	I _{CC6}	CKE ≤ 0.2V		1		1		1		1	mA	
Input leakage current (Inputs)	I _{IL}	0 ≤ V _{IN} ≤ V _{DD(MAX)} Pins not under test = 0V	- 1	1	-1	1	-1	1	-1	1	μA	
Input leakage current (I/O pins)	I _{IL}	0 ≤ V _{OUT} ≤ V _{DD(MAX)} DQ# in H - Z., Dout disabled	- 1.5	1.5	-1.5	1.5	-1.5	1.5	-1.5	1.5	μA	
Output Low Voltage	V _{OL}	I _{OL} = 2mA		0.4		0.4		0.4		0.4	V	4
Output High Voltage	V _{OH}	I _{OH} = -2mA	2.4		2.4		2.4		2.4		V	4

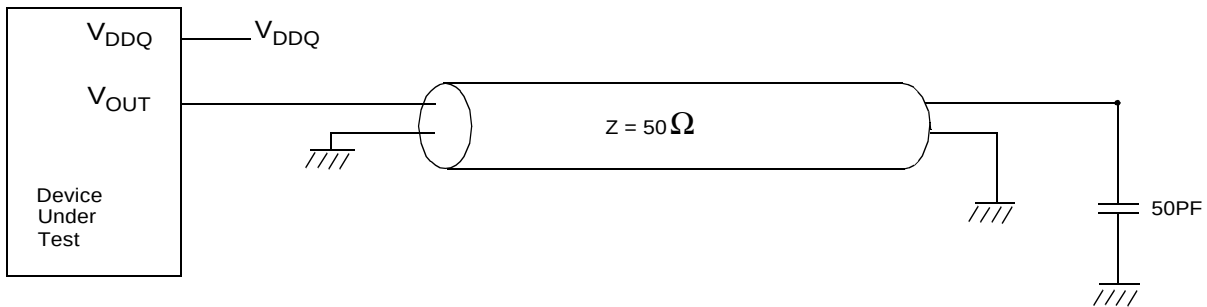
- Notes:
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN)}$.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN)}$.
 - I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN)}$.
 - For LVTTTL compatible.

AC Characteristics : ($T_a = 0$ to 70°C , $V_{DD} = 3.3\text{V} \pm 0.3$, $V_{SS} = 0\text{V}$)

Test Conditions for LVTTL Compatible :

AC input Levels (V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference level	1.4V
Input rise and fall time	1ns	Output load condition	50pF

AC Test Load Circuits (for LVTTL interface) :

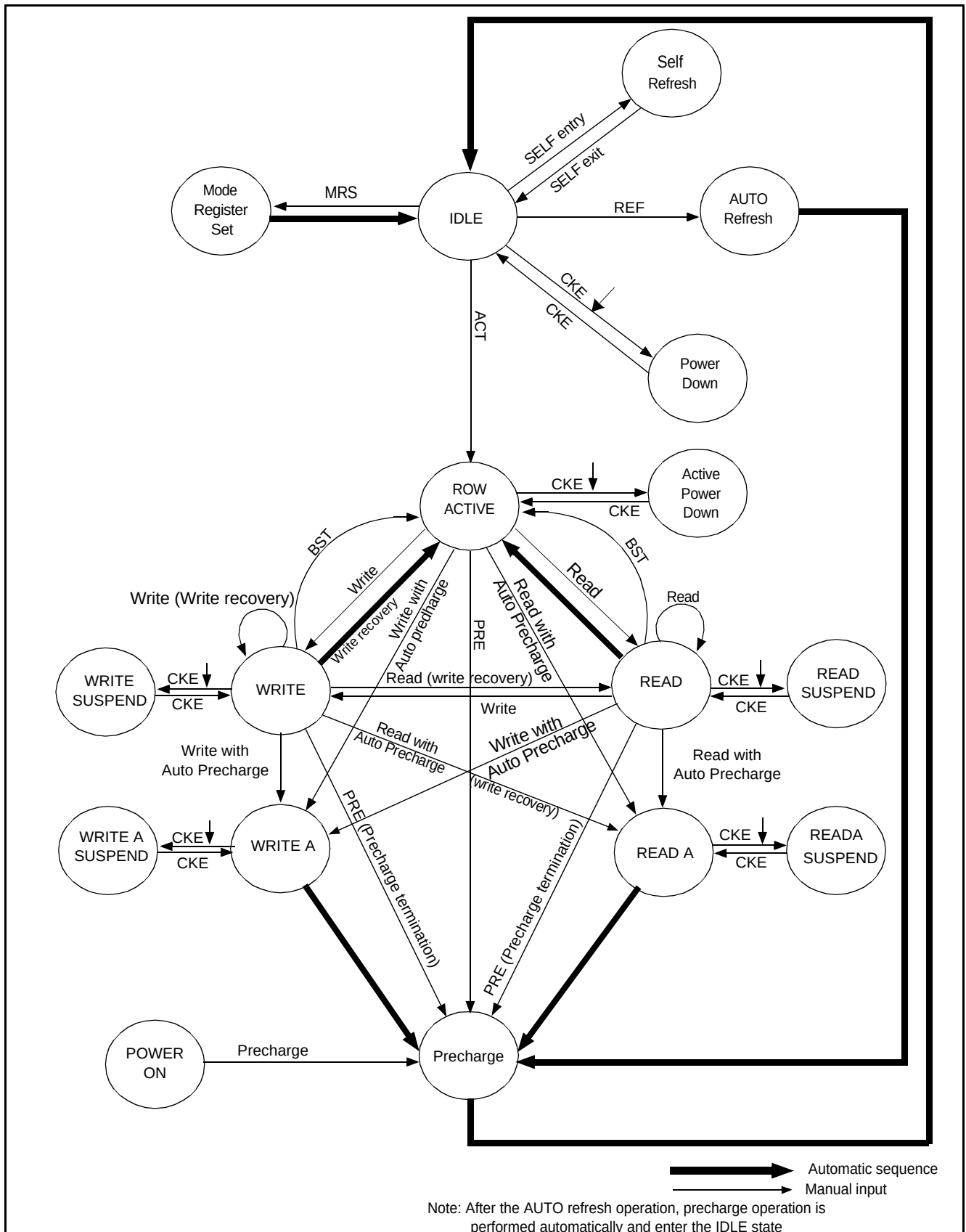


A.C. Characteristics:(Ta=0 to 70°C,VDD=3.3V ±0.3V , VSS =0V)

Parameter	CAS Latency	symbol	VG36643241A								Unit
			-5		-6		-7		-8		
			Min	Max	Min	Max	Min	Max	Min	Max	
CLK cycle time	3	t _{CK3}	5		6		7		8		ns
	2	t _{CK2}	-		8		10		12		ns
Access time form CLK	3	t _{AC3}	4.5		5.5		5.5		6		ns
	2	t _{AC2}	-		6		6		7		ns
CLK high level width		t _{CH}	2		2.5		2.5		3		ns
CLK low level width		t _{CL}	2		2.5		2.5		3		ns
CKE setup time		t _{CKS}	1.5		1.5		1.75		2		ns
CKE hold time		t _{CKH}	0.8		1		1		1		ns
Address setup time		t _{AS}	1.5		1.5		1.75		2		ns
Address hold time		t _{AH}	0.8		1		1		1		ns
Command setup time		t _{CMS}	1.5		1.5		1.75		2		ns
Command hold time		t _{CMH}	0.8		1		1		1		ns
Data input setup time		t _{DS}	1.5		1.5		1.75		2		ns
Data input hold time		t _{DH}	0.8		1		1		1		ns
Output data hold time		t _{OH}	2		2.5		2.5		3		ns
CLK to output in low -		t _{LZ}	1		1		1		1		ns
CLK to output in H - Z	3	t _{HZ}	4.5		5.5		5.5		6		ns
	2		-		6		6		6		
Row active to active		t _{RRD}	10		12		14		16		ns
RAS to CAS delay		t _{RCD}	15		18		20		20		ns
Row precharge time		t _{RP}	15		18		20		20		ns
ROW active time		t _{RAS}	40	100K	42	100K	42	100K	48	100K	ns
ROW cycle time		t _{RC}	55		60		63		68		ns
CAS to CAS dela		t _{CCD}	1		1		1		1		clk
Data in to active com-mand		t _{DAL}	1clk+t _{RP}		1clk+t _{RP}		1clk+t _{RP}		1clk+t _{RP}		clk
Data in to prechrge		t _{DPL}	7		7		7		7		ns
Transition time		t _T	0.5	10	0.5	10	0.5	10	0.5	10	ns
Mode reg. set cycle		t _{RSC}	2		2		2		2		clk
Power down exit		t _{PDE}	2		2		2		2		ns
Self refresh exit time		t _{SRX}	1		1		1		1		clk
Refresh time		t _{REF}		64		64		64		64	ms

Basic Features and Function Description

1.Simplified State Diagram



2.Truth Table

2.1 Command Truth Table

FUNCTION	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	A10	A11 A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
CBR (Auto) refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh	SELF	H	L	L	L	L	H	X	X	X

2.2 DQM Truth Table

FUNCTION	Symbol	CKE		DQM
		n - 1	n - 1	
Data write/output enable	ENB	H	X	L
Data mask/output disable	MASK	H	X	H

2.3 CKE Truth Table

Current State	Function	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Add - ress
			n - 1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

H : High level, L : Low level

X : High or Low level (Don't care), V : Valid Data input

2.4 Operative Command Table (note 1)

(1/3)

HCurrent state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or Power down	2
	L	H	H	X	X	NOP or BST	Nop or Power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BR, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self refresh	4
	L	L	L	L	Op-Code	MPS	Mode register access	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read : Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write : Determine AP	7,8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → write recovering	
	L	H	H	H	X	NOP	Continue burst to end → write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read : Determine AP	7,8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CA}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → write recovering with auto precharge	
	L	H	H	H	X	NOP	Continue burst to end → write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,9
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3,8,11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3,11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Auto Refreshing	H	X	X	X	X	DESL	Nop Enter idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Nop Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode register setting	H	X	X	X	X	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	X	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/REF/SELF/MRS	ILLEGAL	

- Note: 1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power downmode.
All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by BankAddress(BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode.
All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy t_{DPL} .
10. Illegal if t_{RRD} is not satisfied.
11. Illegal for single bank, but legal for other banks in multi-bank devices.

2.5 Command Truth Table for CKE (Note 1)

Current state	CKE _{n-1}	CKE _n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	X	X	X	X	X	X	INVALID, CLK (n - 1) would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain S.R.	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t _{RC}	
	H	H	L	H	H	X	X	Idle after t _{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin clock suspend next cycle	5
	H	L	L	H	H	X	X	Begin clock suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
	L	L	X	X	X	X	X	Maintain clock suspend	
Power down (P.D.)	H	X	X	X	X	X		INVALID, CLK (n - 1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D. → Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operation in Operative Command Table	
	H	H	L	L	L	H	X	Auto Refresh	
	H	H	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	3
	H	L	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	3
Any state other than listed above	H	H	X	X	X	X	X	Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Note: 1. H : High level, L : low level, X : High or low level (Don't care).

2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

3. Power down and Self refresh can be entered only from the both banks idle state.

4. Must be legal command as defined in Operative Command Table.

5. Illegal if t_{SREX} is not satisfied.

3.Initiallization

The synchronous DRAM is initialized in the power on sequence. Once power has been applied, a 100us minimum delay is needed in which stable power and input signals are maintained. During this delay, CKE and DQM recommend to be held high.

After the 100us delay, all banks must be precharged using the precharge command. Once precharge is completed and the minimum t_{RP} is satisfied, mode register can be programmed.

Minimum two CBR refresh commands must be performed before or after the mode register set command.

4.Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A13 through A0 as data inputs. The register retains data until it is reprogrammed or until the device loses power.

Following mode register programming, no command can be asserted before at least two clock cycles have elapsed.

CAS Latency

CAS latency is the most critical parameter to be set. It tells the device how many clocks must elapse before the data will be available. The SDRAM is capable of reconfiguring its internal architecture based on the value of CAS latency.

The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.

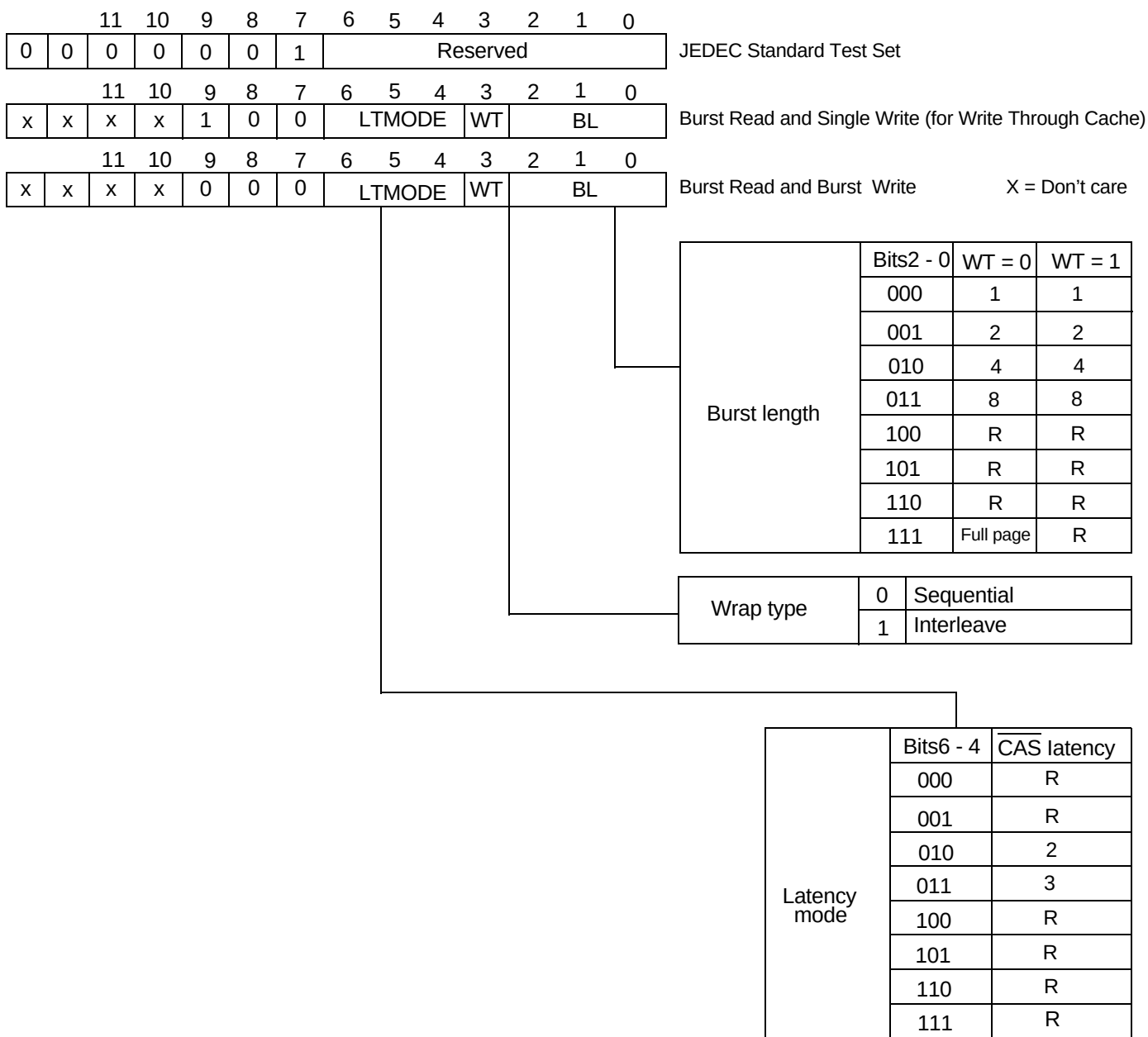
The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. Both sequences support bursts of 1,2,4 and 8. Only the sequential burst. supports the full-page length.

5.Mode Register (Address Input for Mode Set)



Remark R : Reserved

5.1 Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

(Burst of Four)

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

(Burst of Eight)

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence(decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 for 8M x 8 devices.

6.Address Bits of Bank-Select and Precharge

6.1 Quad banks controlled by A12 & A13 (for VG36648041/VG36648042)

Row	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A12	A13	Result
(Activate command)															0	0	Select Bank A "Activate" command
															0	1	Select Bank B "Activate" command
															1	0	Select Bank C "Activate" command
															1	1	Select Bank D "Activate" command

Row	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A10	A12	A13	Result
(Precharge command)															0	0	0	Precharge Bank A
															0	0	1	Precharge Bank B
															0	1	0	Precharge Bank C
															0	1	1	Precharge Bank D
															1	X	X	Precharge All Banks

X: Don't care

															0	Disables Auto - Precharge (End of Burst)
															1	Enables Auto - Precharge (End of Burst)

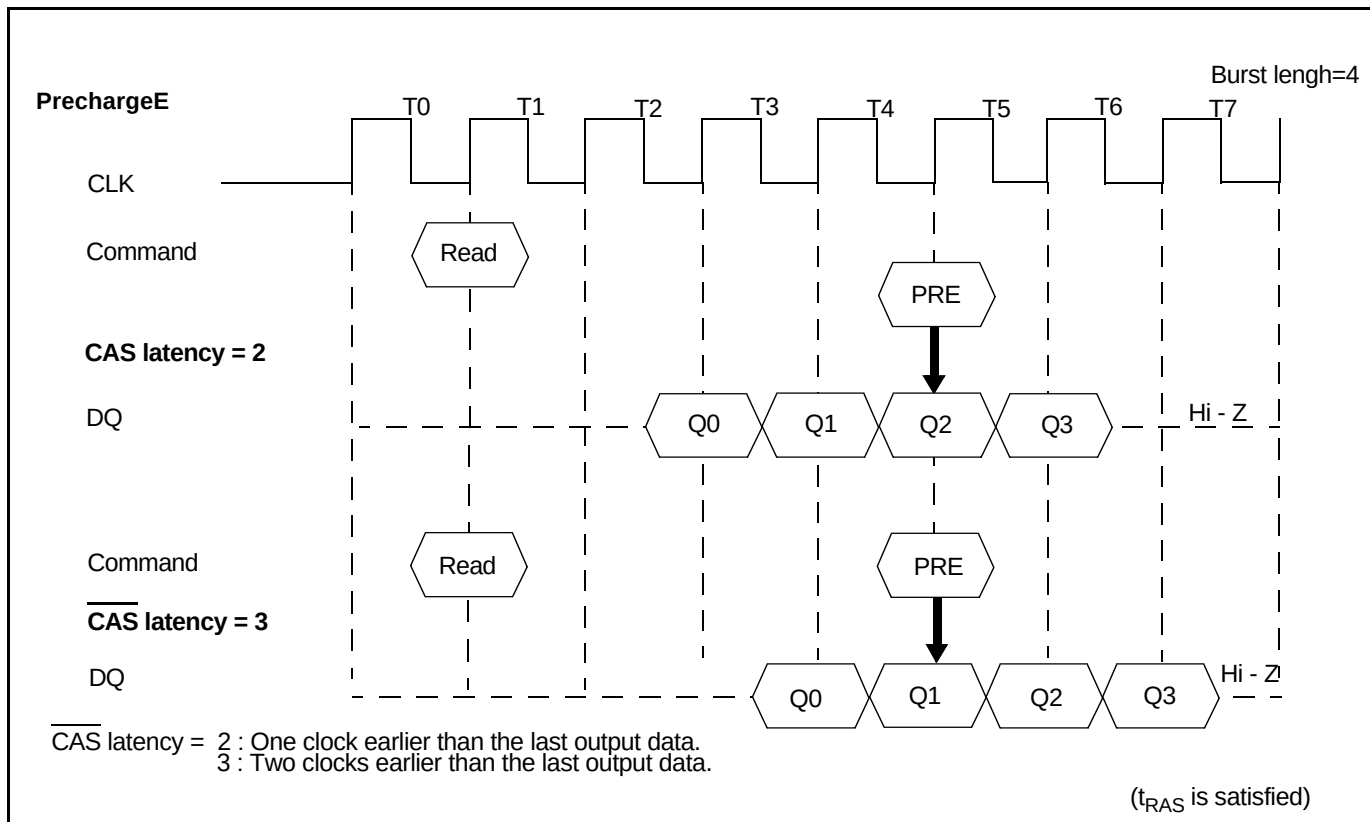
Co1.	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A12	A13	Result
(CAS strobes)															0	0	Enables Read/Write commands for Bank A
															0	1	Enables Read/Write commands for Bank B
															1	0	Enables Read/Write commands for Bank C
															1	1	Enables Read/Write commands for Bank D

7.Precharge

The precharge command can be asserted anytime after $t_{RAS(min)}$ is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after $t_{RP(min)}$ is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.



In order to write all data to the memory cell correctly, the asynchronous parameter " t_{DPL} " must be satisfied. The $t_{DPL(min)}$ specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks can be calculated by dividing $t_{DPL(min)}$ by the clock cycle time.

In summary, the precharge command can be asserted relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

CAS latency	Read	Write
2	-1	+ $t_{DPL(min)}$
3	-2	+ $t_{DPL(min)}$

8.Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically after the burst access.

In the write cycle, $t_{DAL(min.)}$ must be satisfied before asserting the next activate command to the bank being precharged.

When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

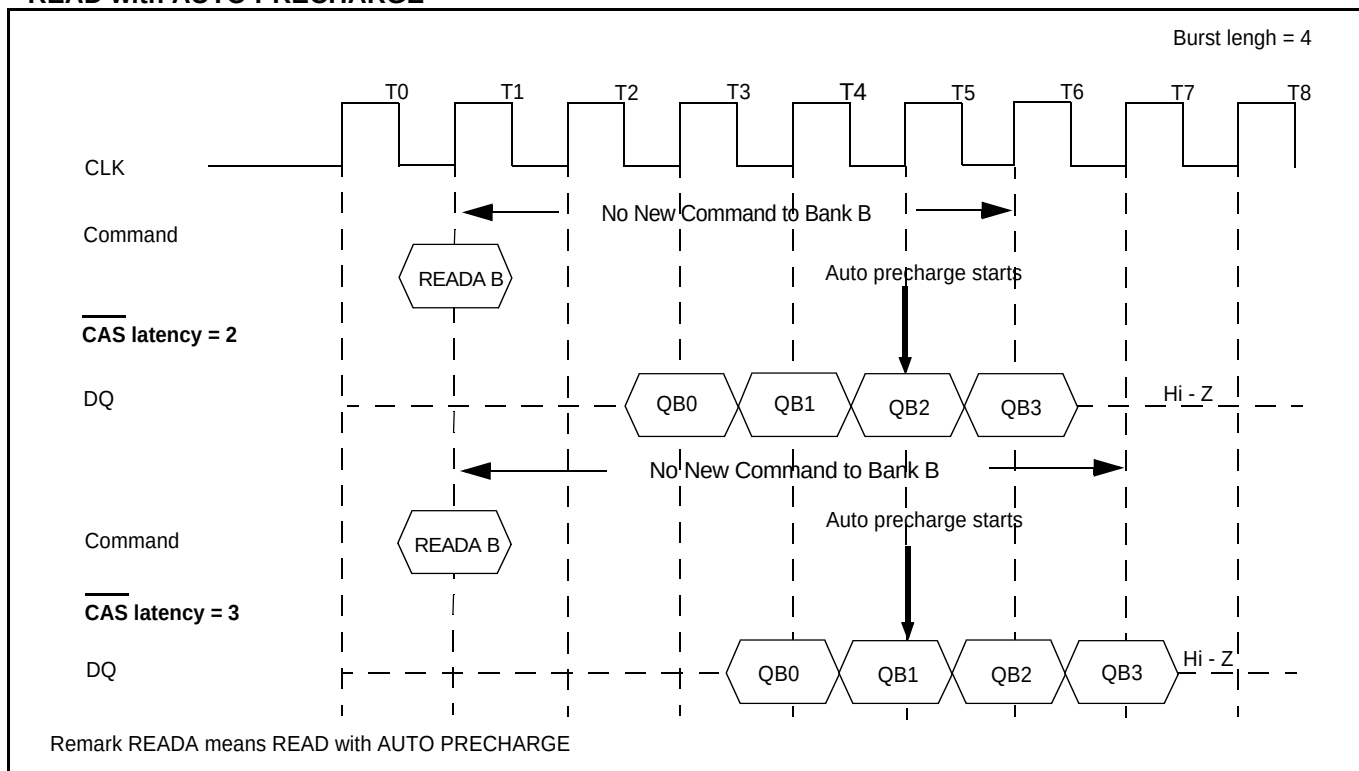
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Pre-charge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the $\overline{CAS}$ latency programmed into the mode register and whether the cycle is read or write.

8.1 Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier ($CL = 2$) or two clocks earlier ($CL = 3$) than the last word output.

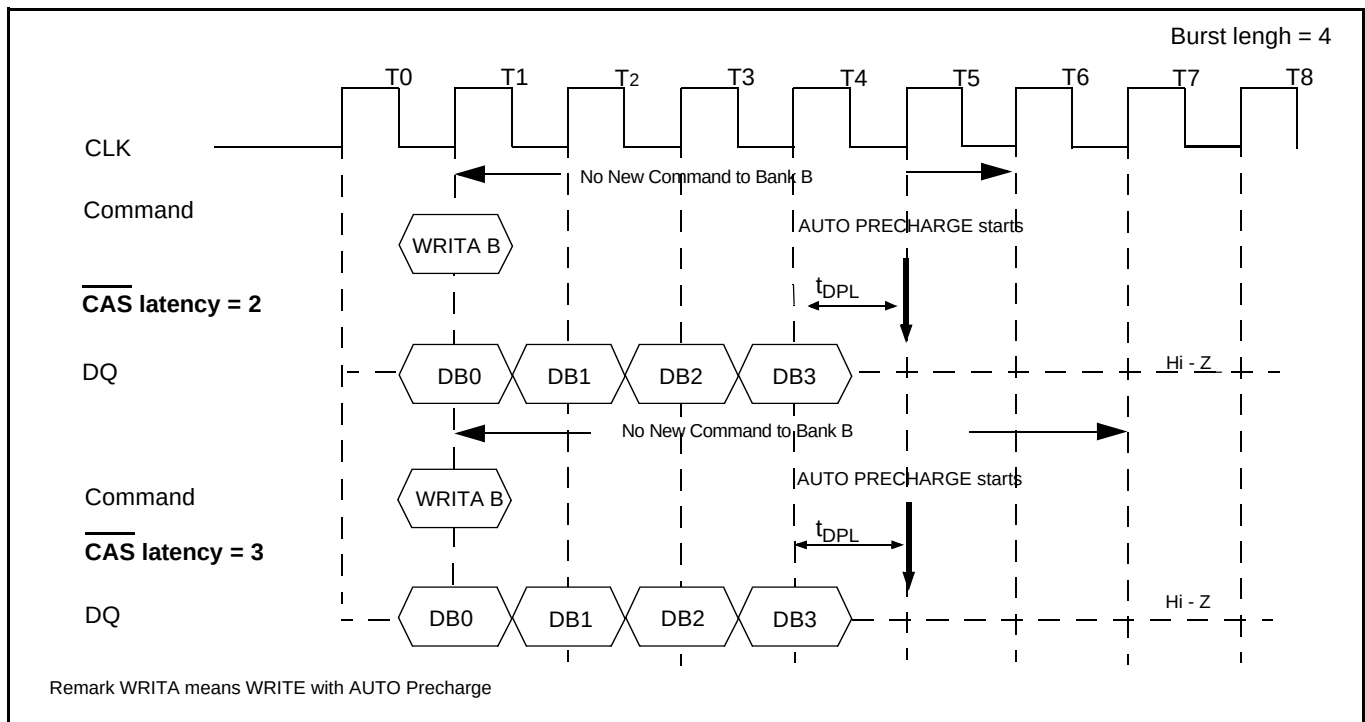
READ with AUTO PRECHARGE



8.2 Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of $t_{DPL(min.)}$ after the last data word input to the device.

WRITE with AUTO PRECHARGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

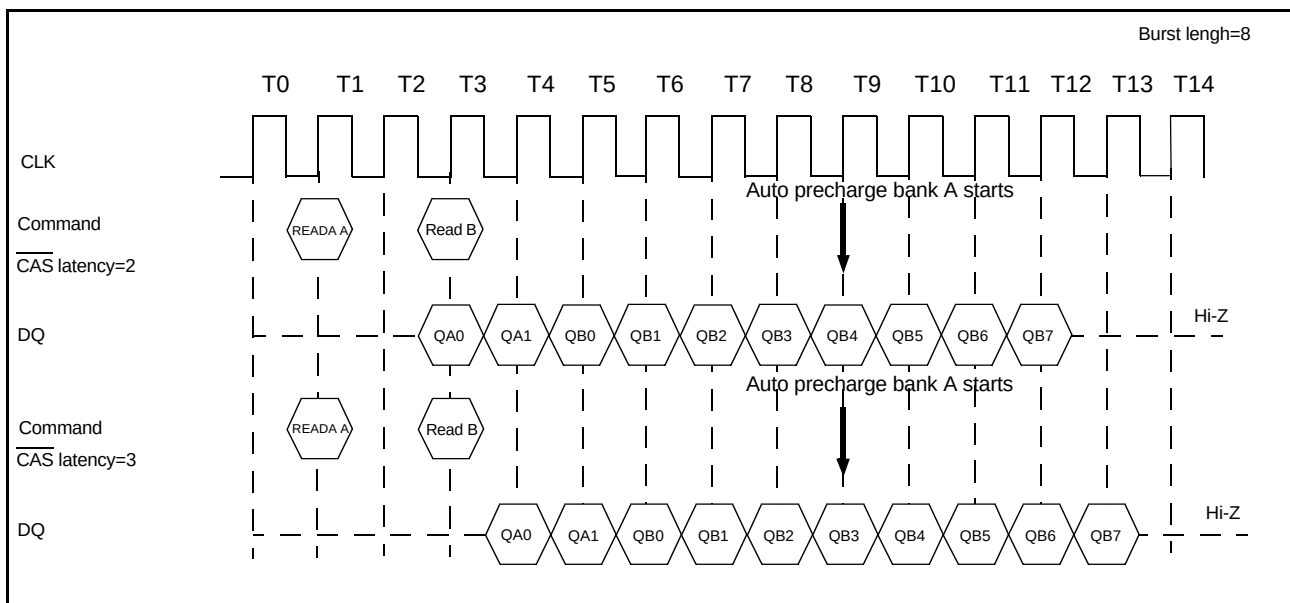
CAS latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

9. Read/Write Command Interval

8.3 Multibank Operation- Read with Auto Precharge

During a READA cycle interrupted by a Read, Write command of another banks, the auto-pre-charge scheduled time would not be changed.

Multibank Operation

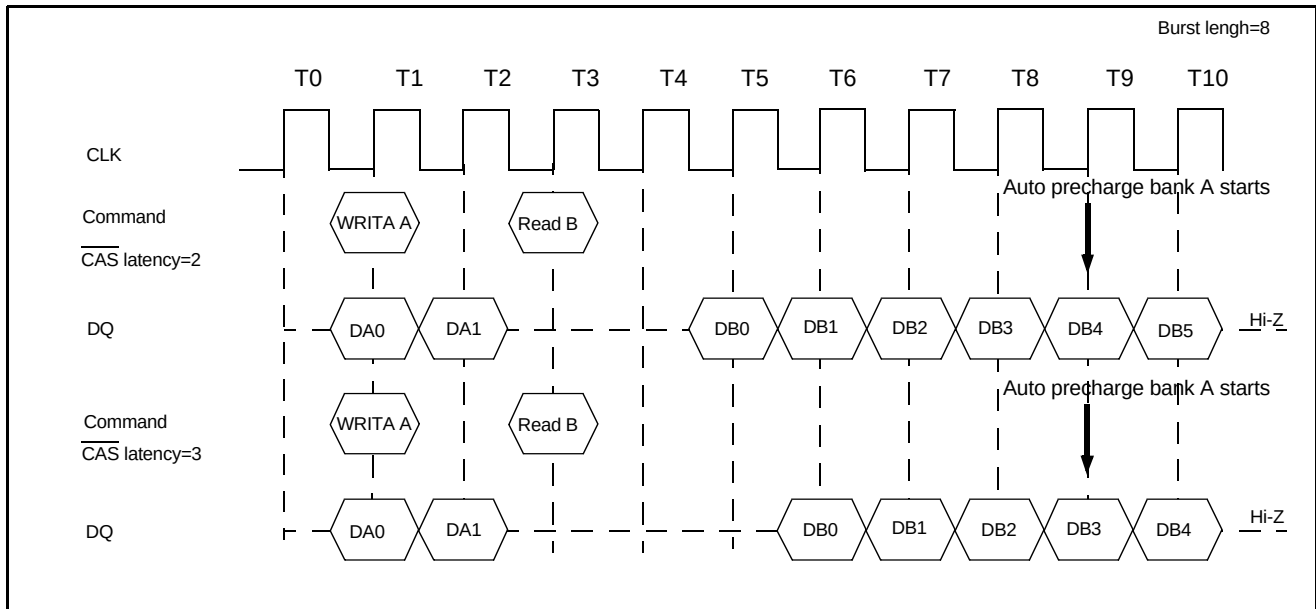


Similar top.21

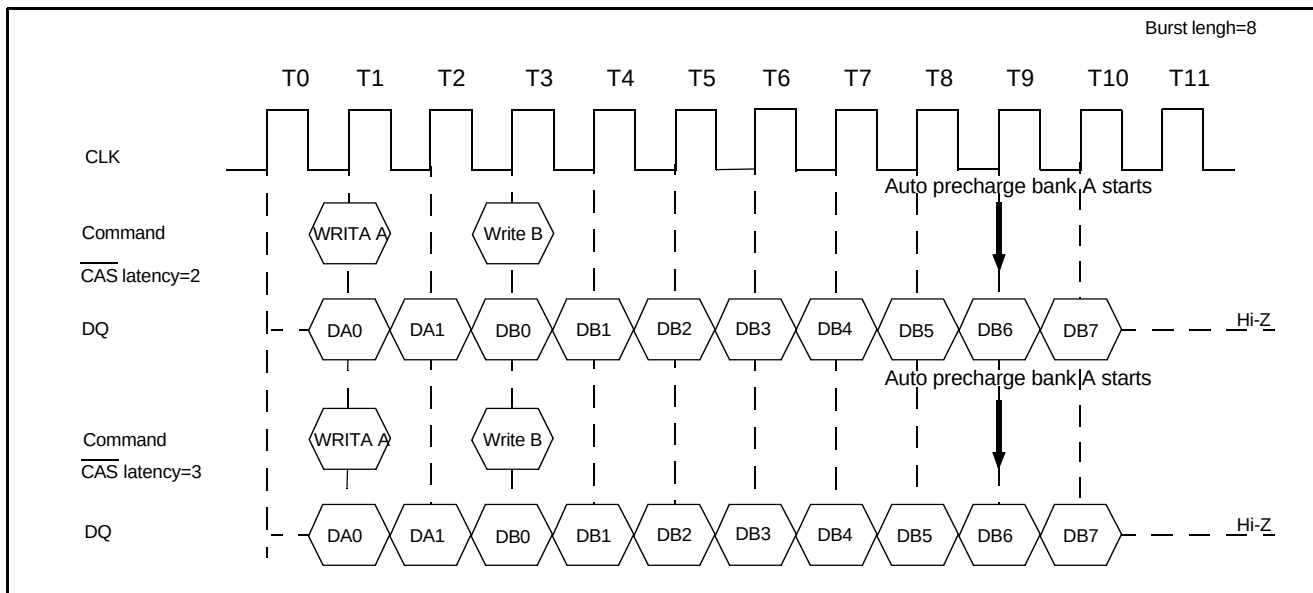
8.4 Multibank Operation- Write with Auto Precharge

During a WRITEA cycle interrupted by a Read, Write command of another banks, the auto-pre-charge scheduled time would not be changed.

Multibank Operation



Multibank Operation

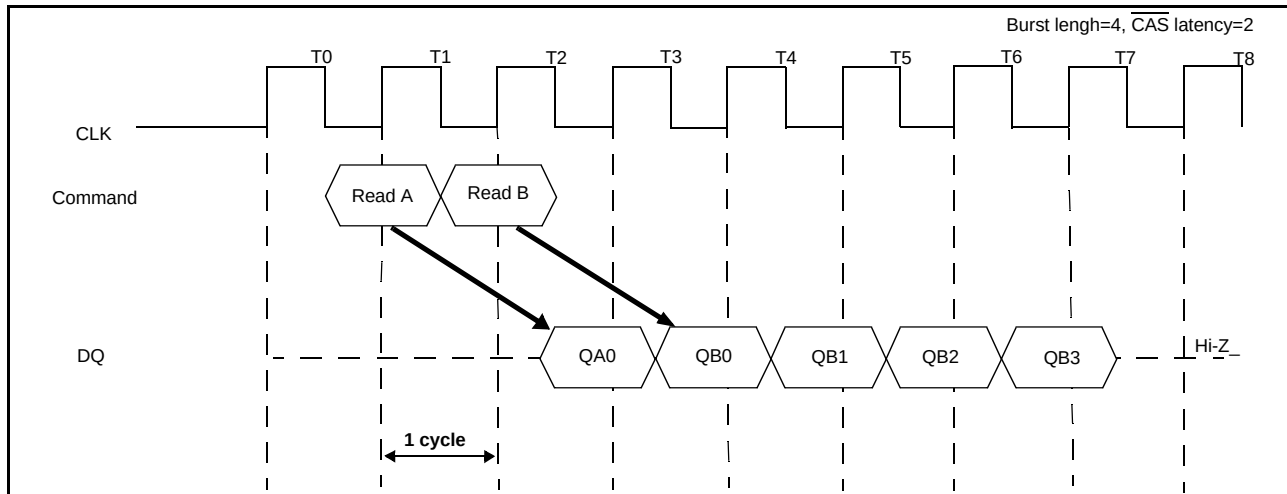


9.1 Read to Read command interval

During a read cycle when a new read command is asserted, it will be effective after the $\overline{\text{CAS}}$ latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval

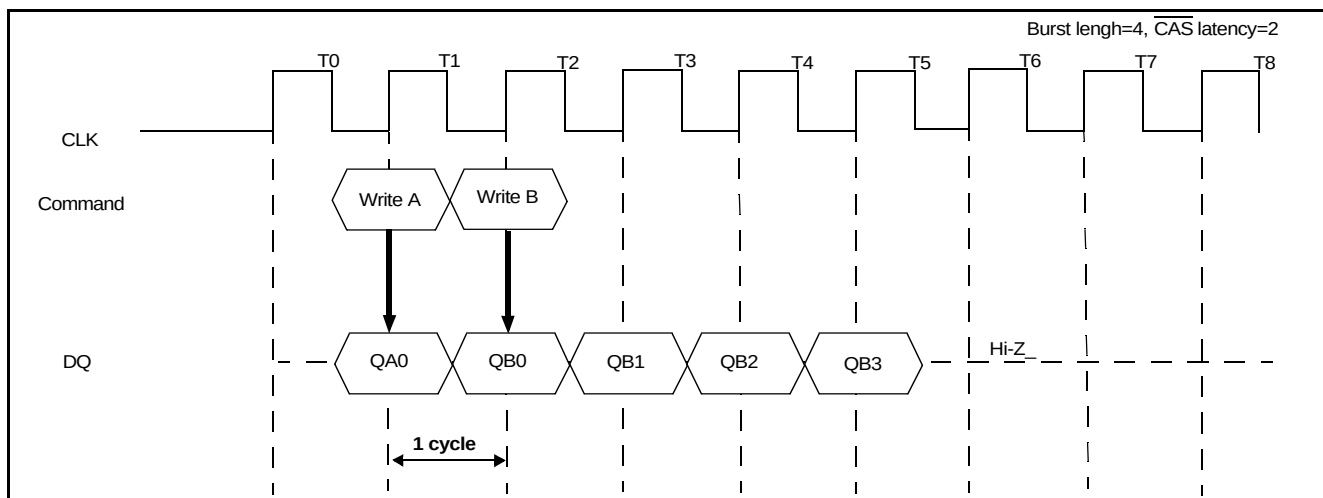


9.2 Write to Write Command Interval

During a write cycle, when a new Write command is asserted, the previous burst will be terminated and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.

Each write command can be asserted in every clock without any restriction.

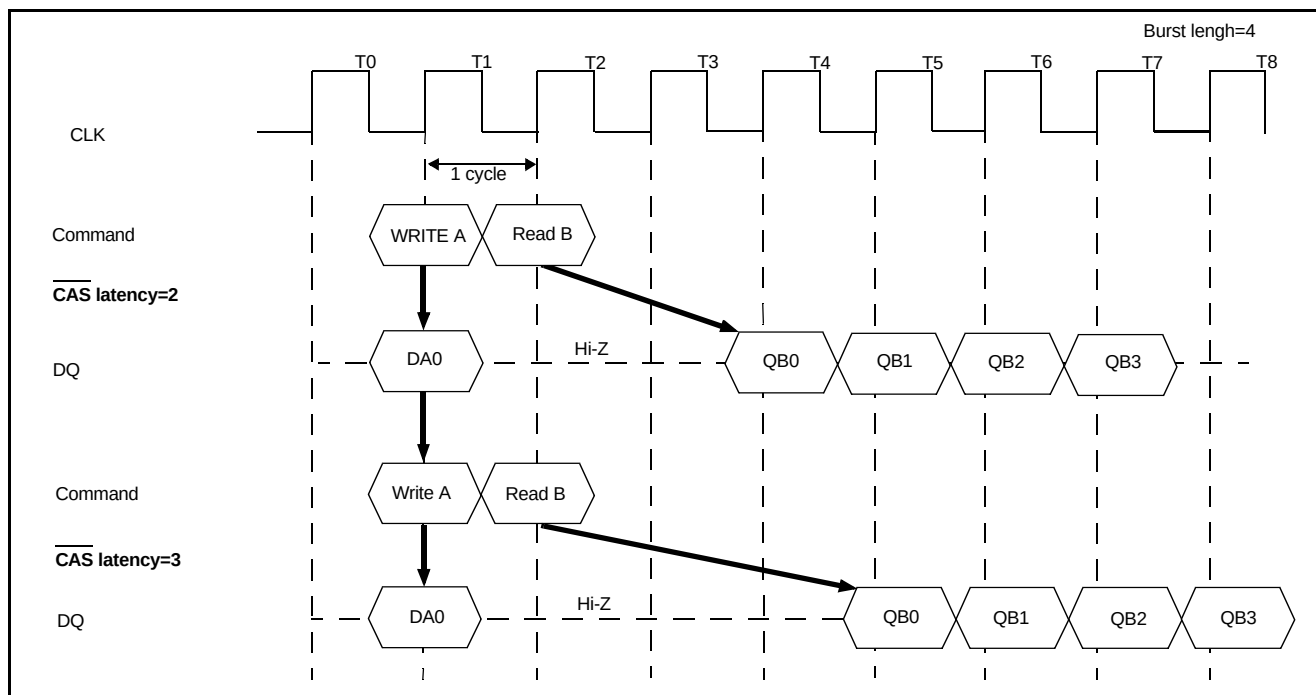
WRITE to WRITE Command Interval



9.3 Write to Read Command Interval

The write command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi-Z at least one cycle prior to the first D_{OUT}.

WRITE to READ Command Interval

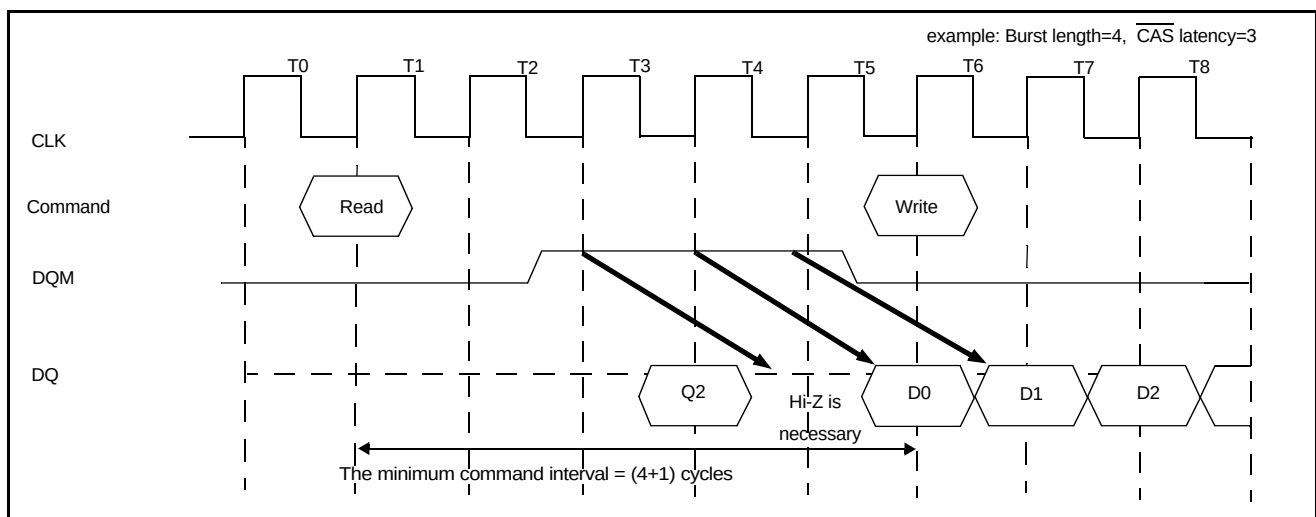
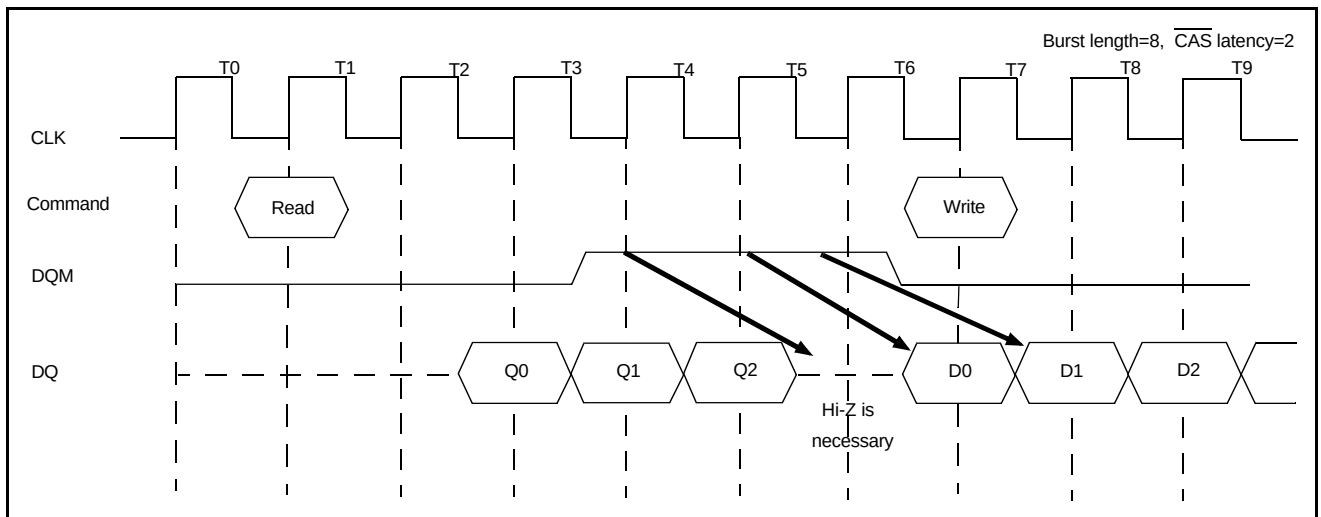
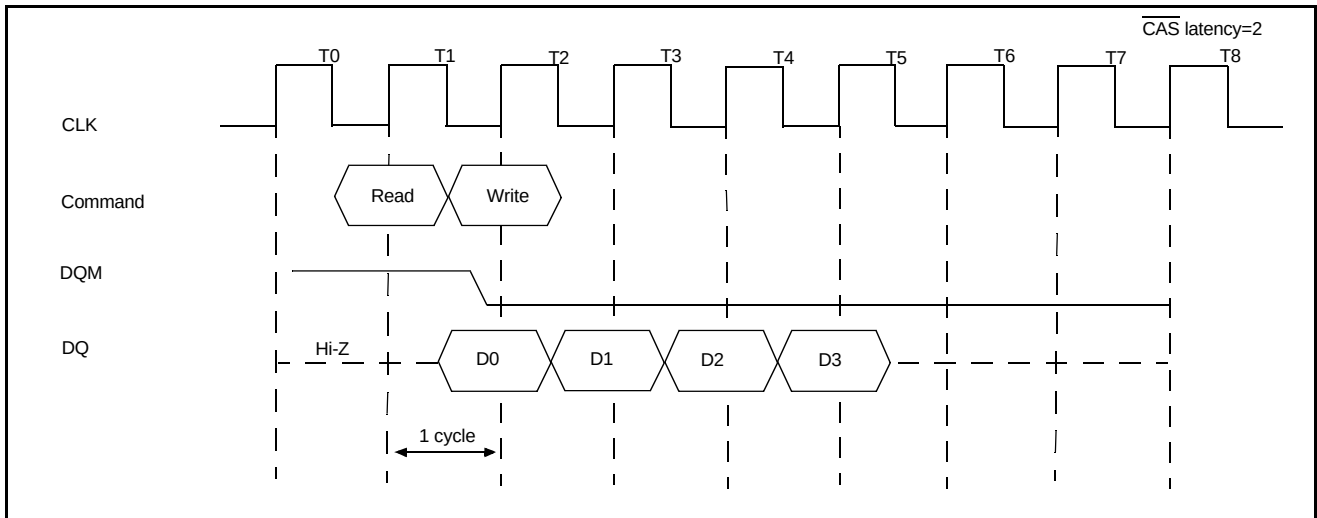


9.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

DQM must be in High at least 3 clocks prior to the write command. There is a restriction to avoid a data conflict. The data bus must be Hi-Z using DQM before Write.

READ to WRITE Command Interval



10.BURST Termination

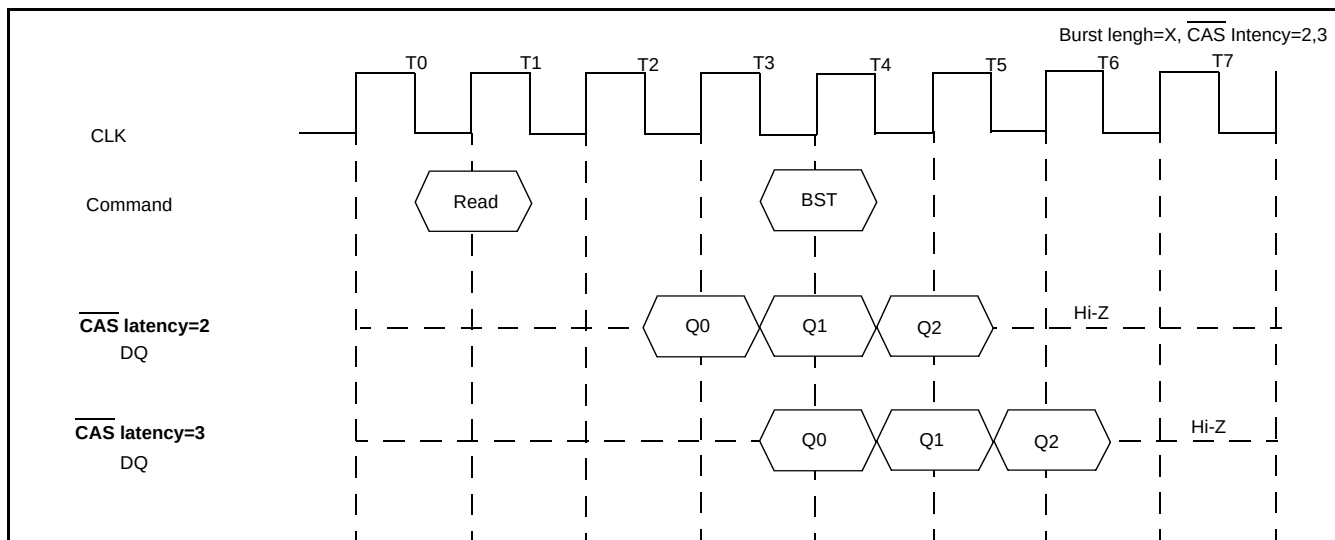
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

10.1 BURST Stop Command

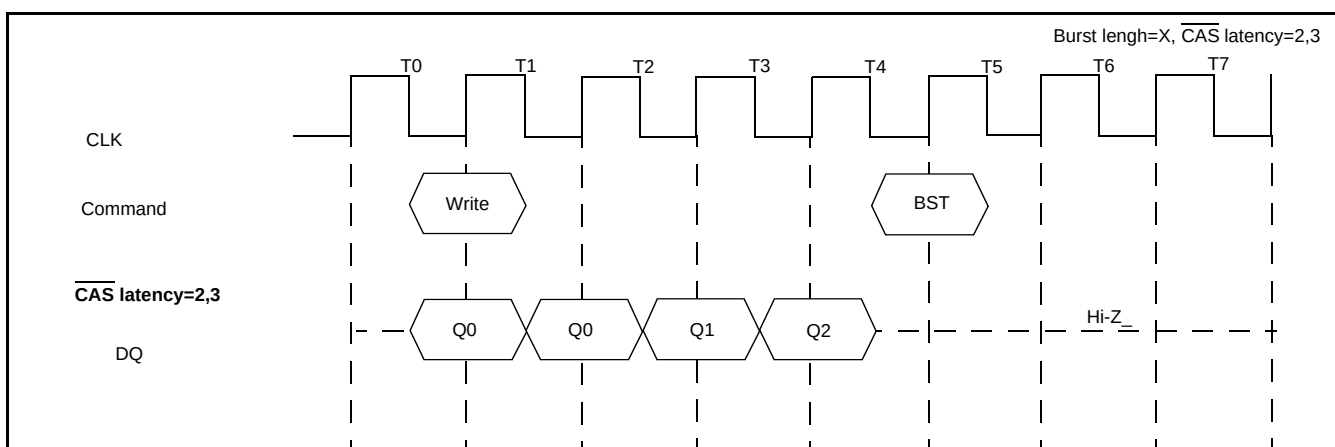
During a read burst, when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high-impedance after the $\overline{\text{CAS}}$ latency from the burst stop command.

During a write burst, when the burst stop command is asserted, any data provided at that cycle will not be written. The burst write is effectively terminated and no further data can be written until a new write command is asserted.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst command

10.2 PRECHARGE TERMINATION

10.2.1 PRECHARGE TERMINATION in READ Cycle

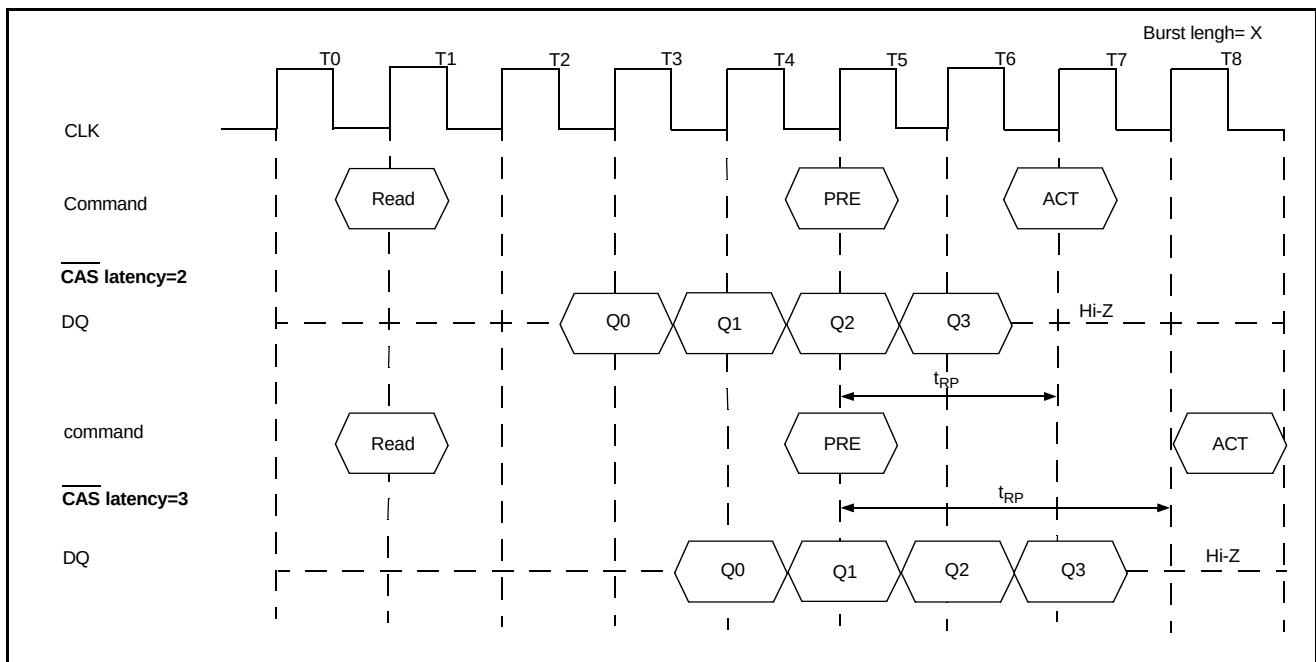
During READ cycle, the burst read operation is terminated by a precharge command. When the precharge command is asserted, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When CAS latency is 2, the read data will remain valid until one clock after the precharge command.

When CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



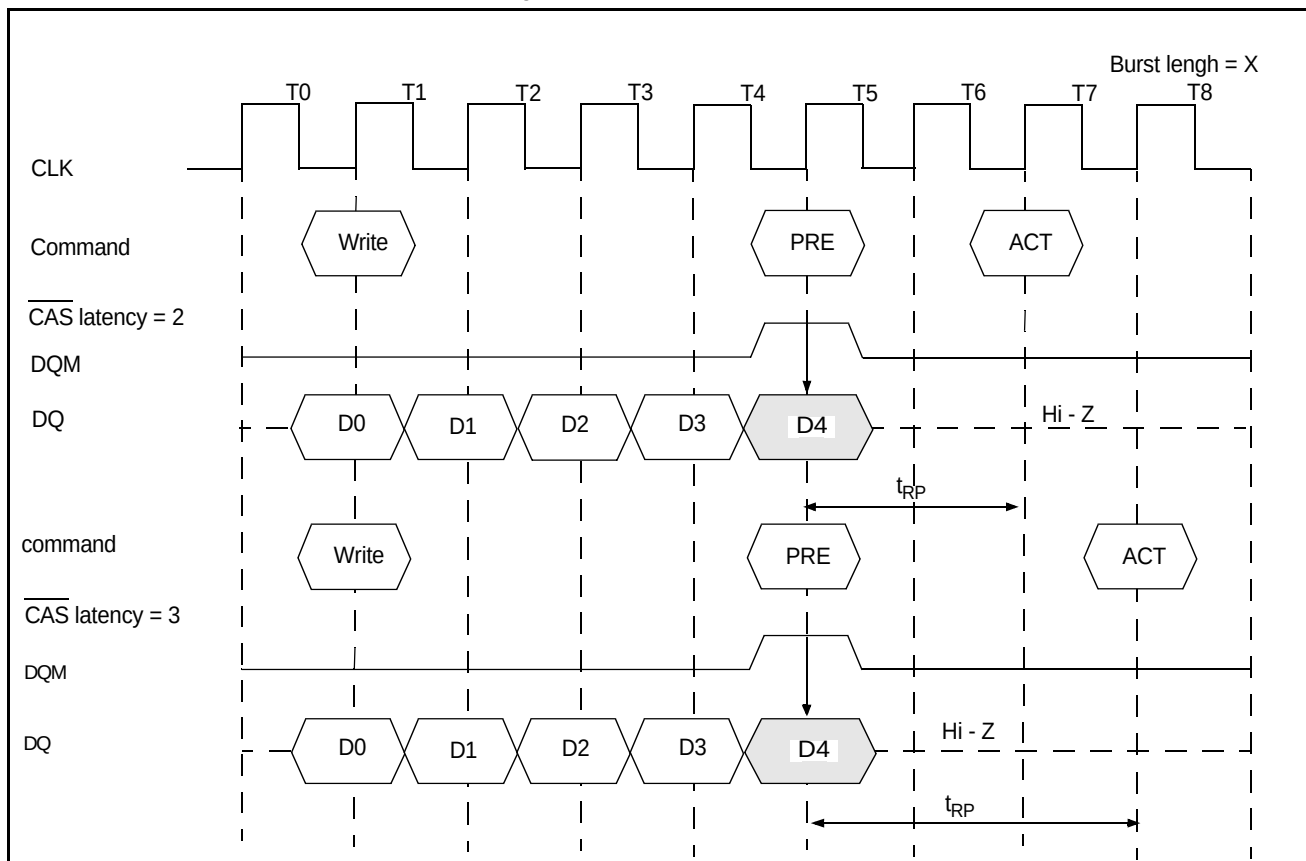
10.2.2 Precharge Termination in WRITE Cycle

During WRITE cycle, the burst write operation is terminated by a precharge command. When the precharge command is asserted, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

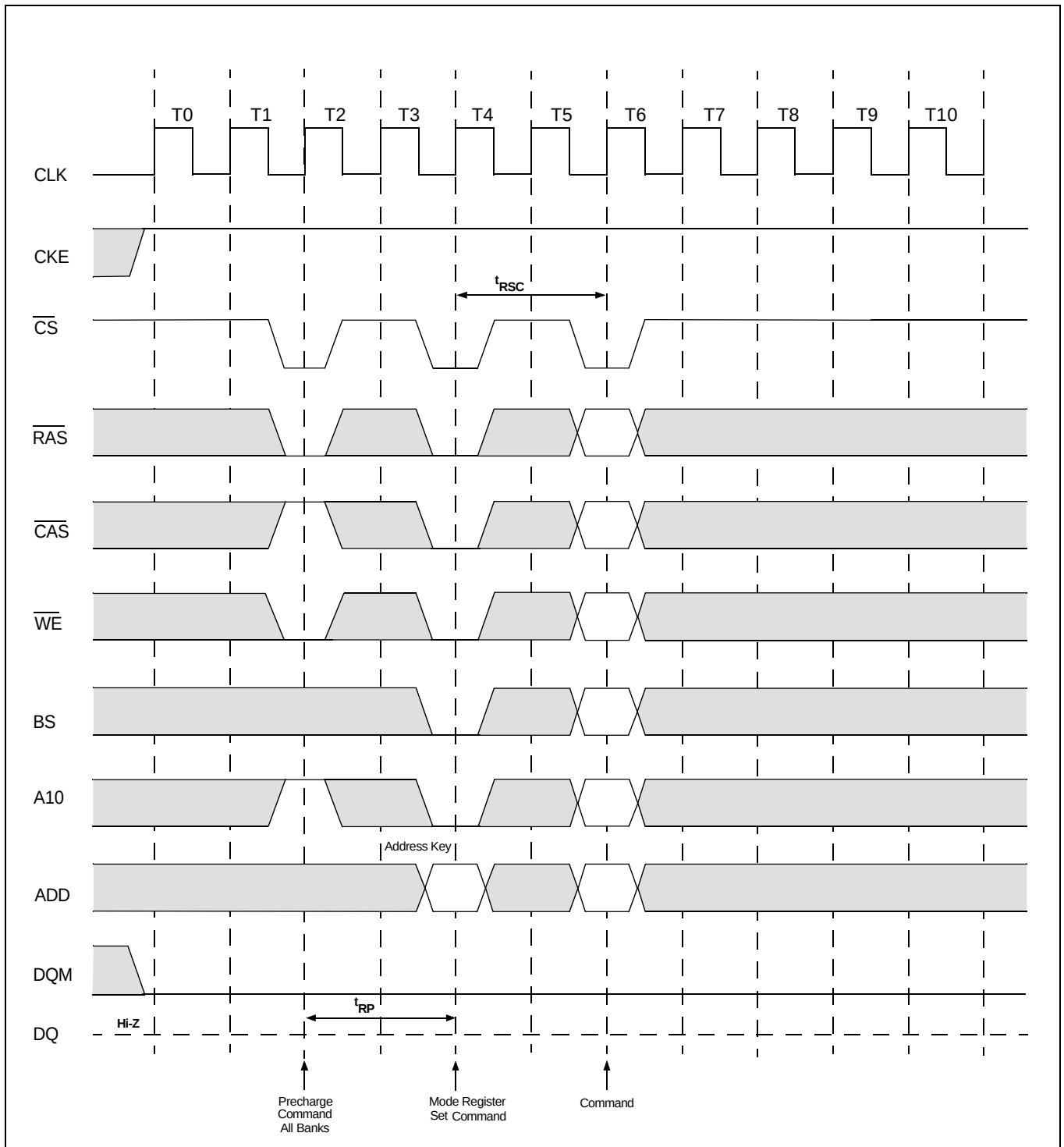
During WRITE cycle, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

PRECHARGE TERMINATION in WRITE Cycle

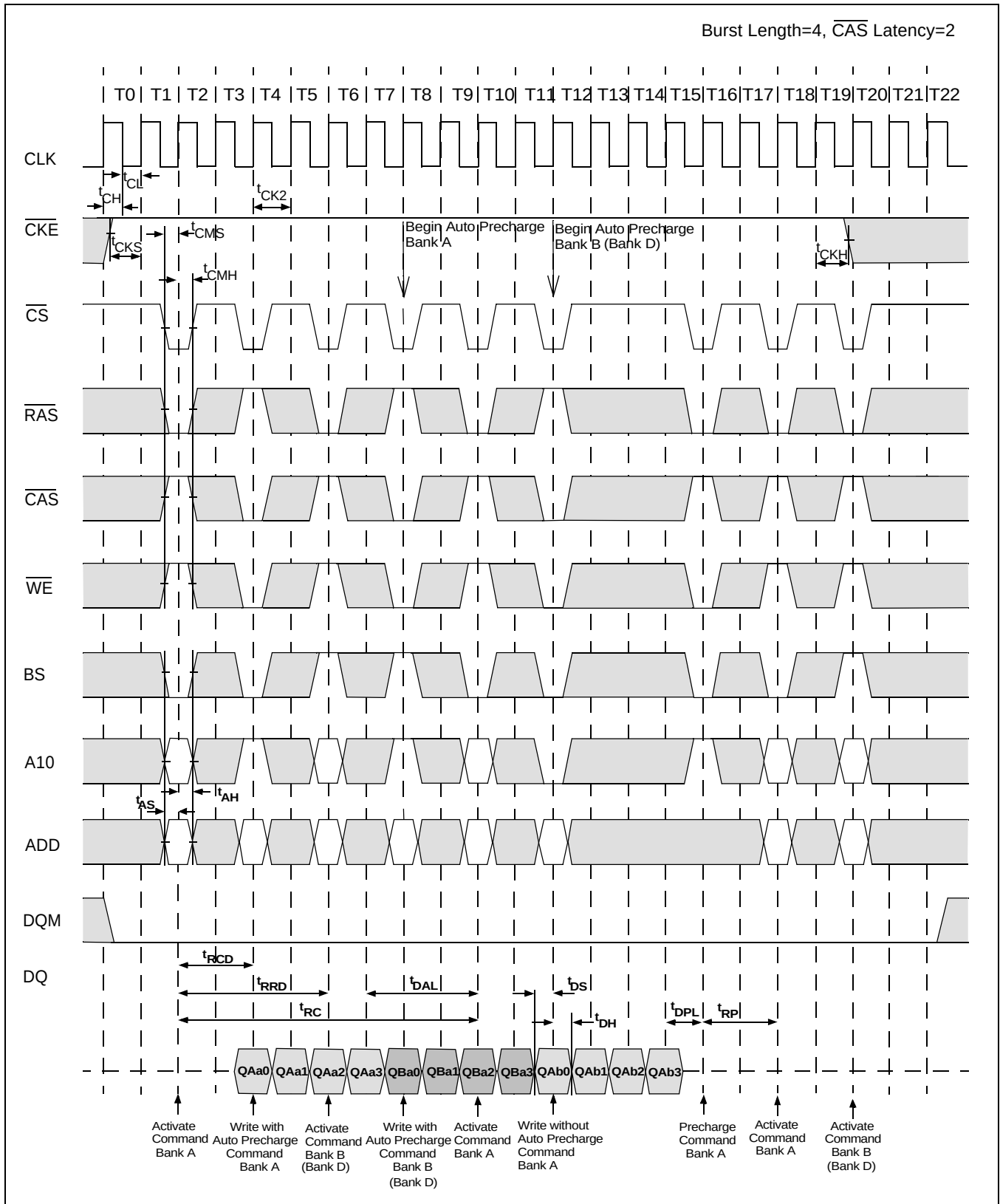


Timing Diagram

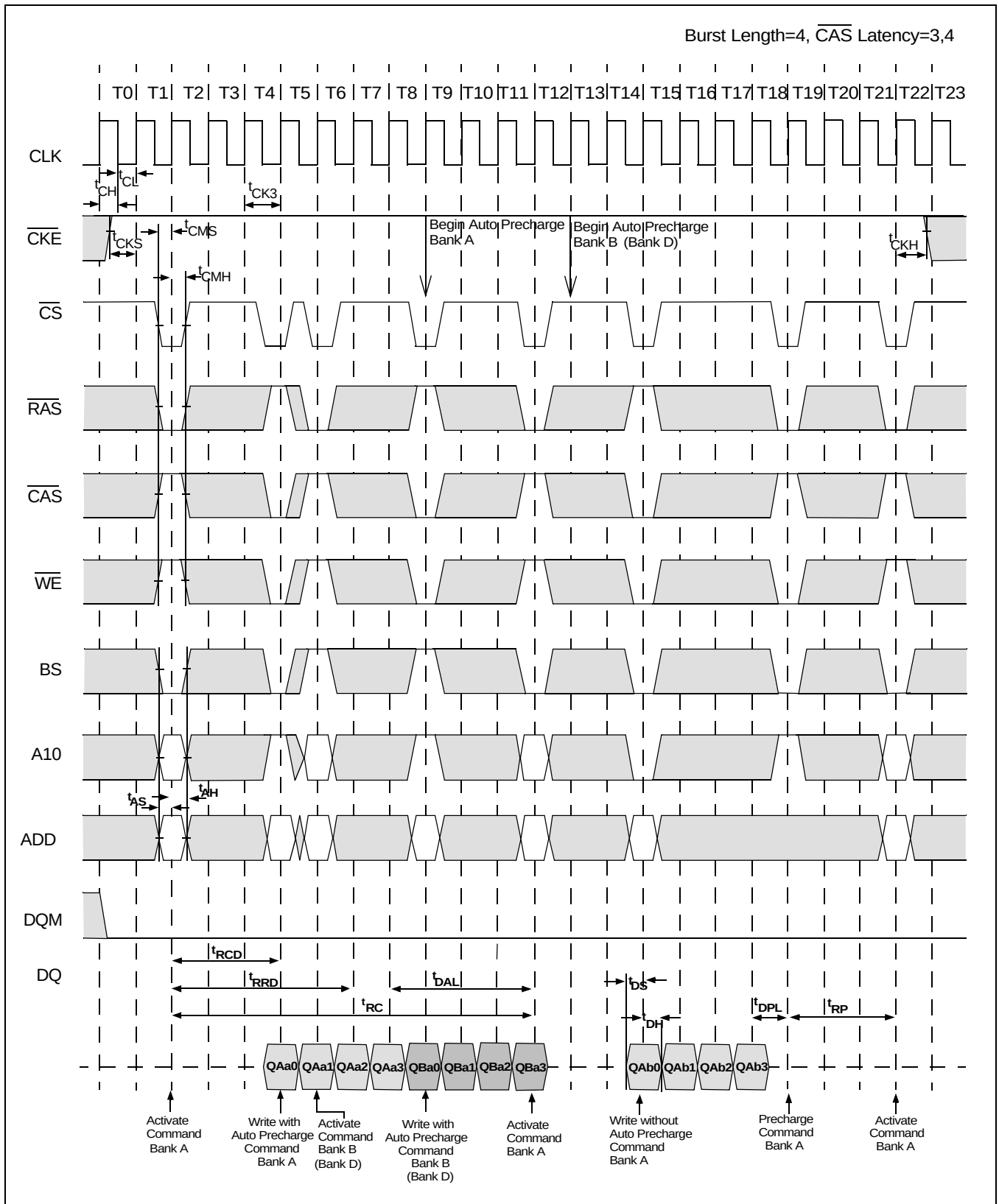
Mode Register Set



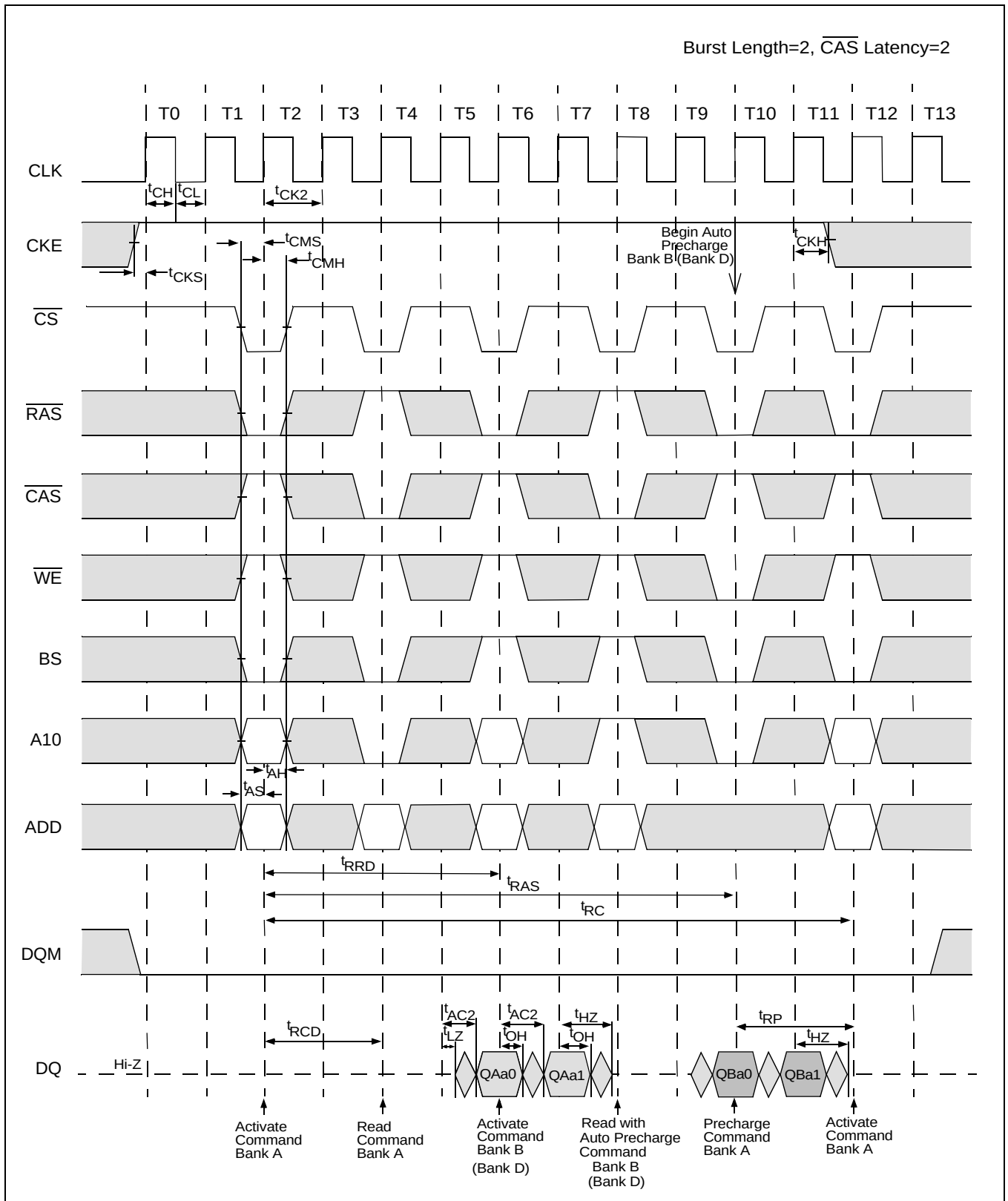
AC Parameters for Write Timing (1 of 2)



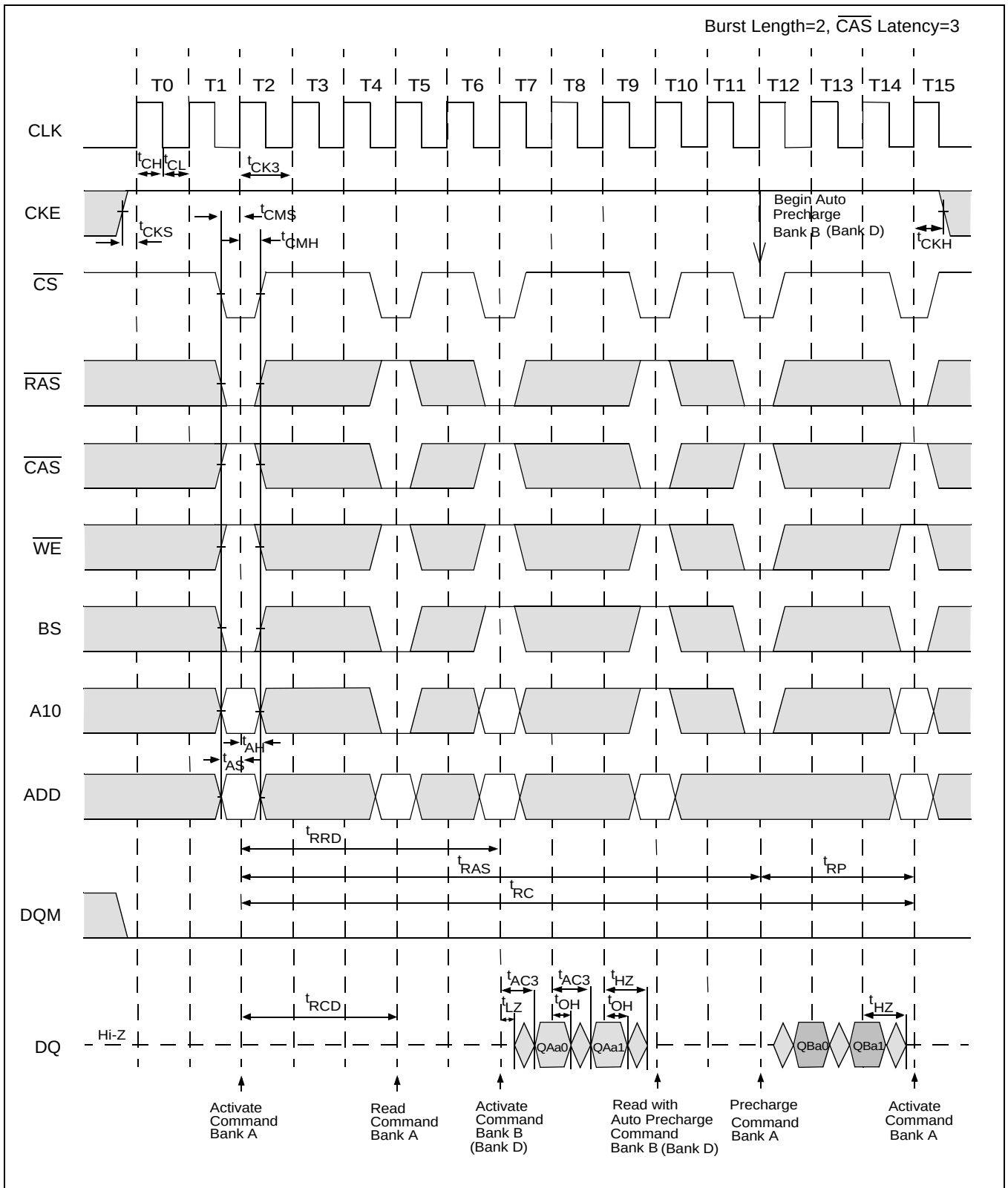
AC Parameters for Write Timing (2 of 2)



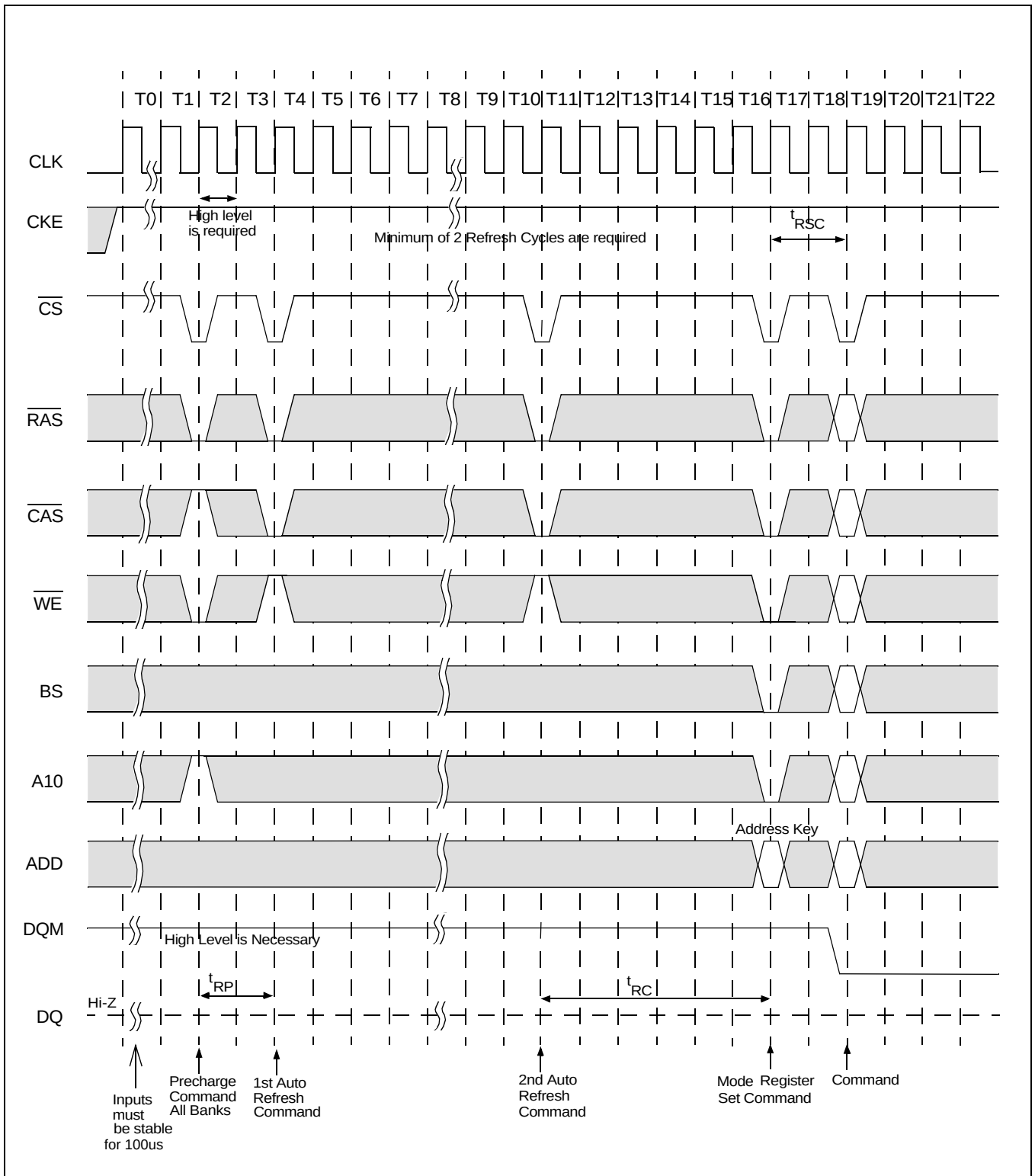
AC Parameters for Read Timing (1 of 2)



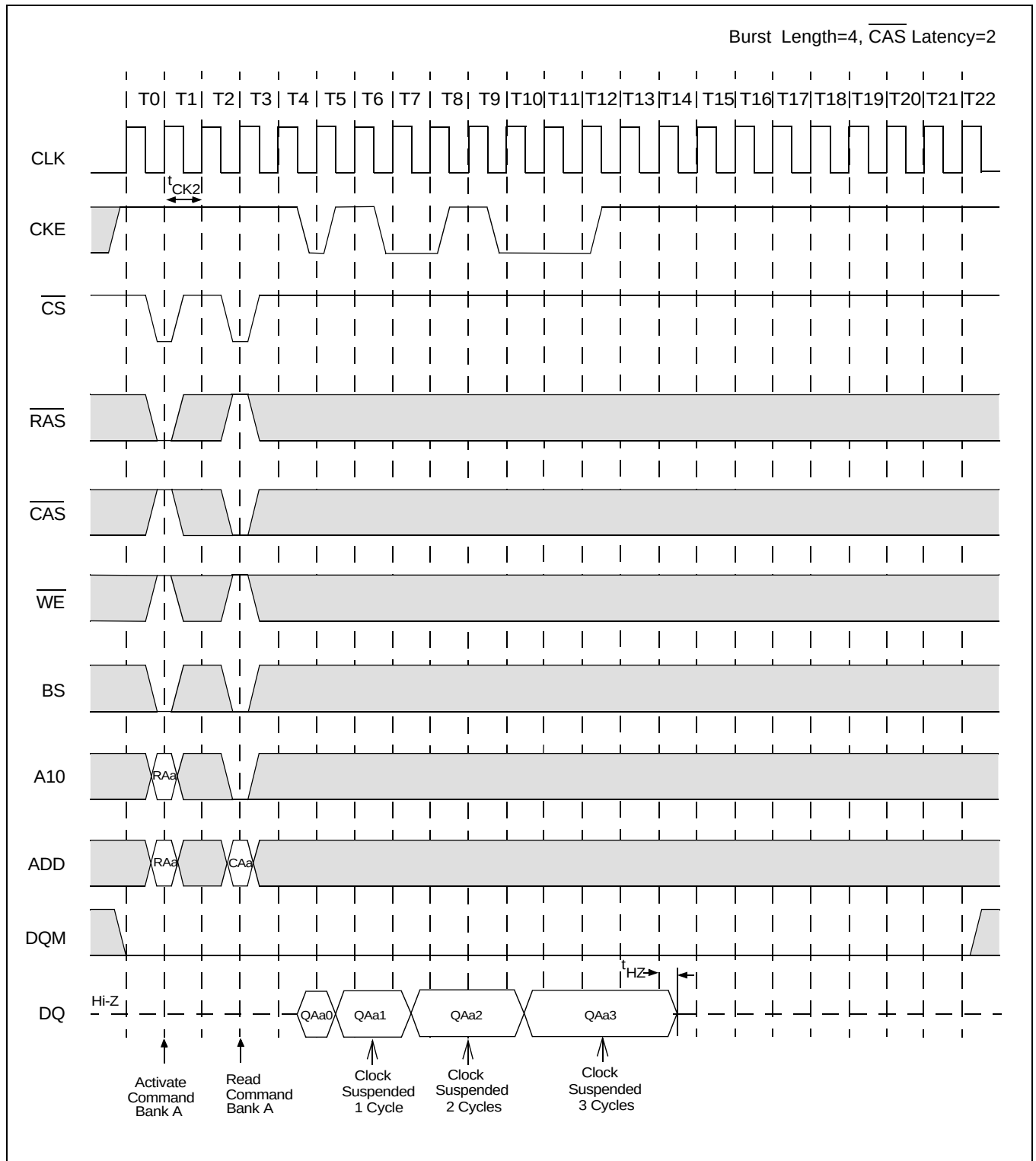
AC Parameters for Read Timing (2 of 2)



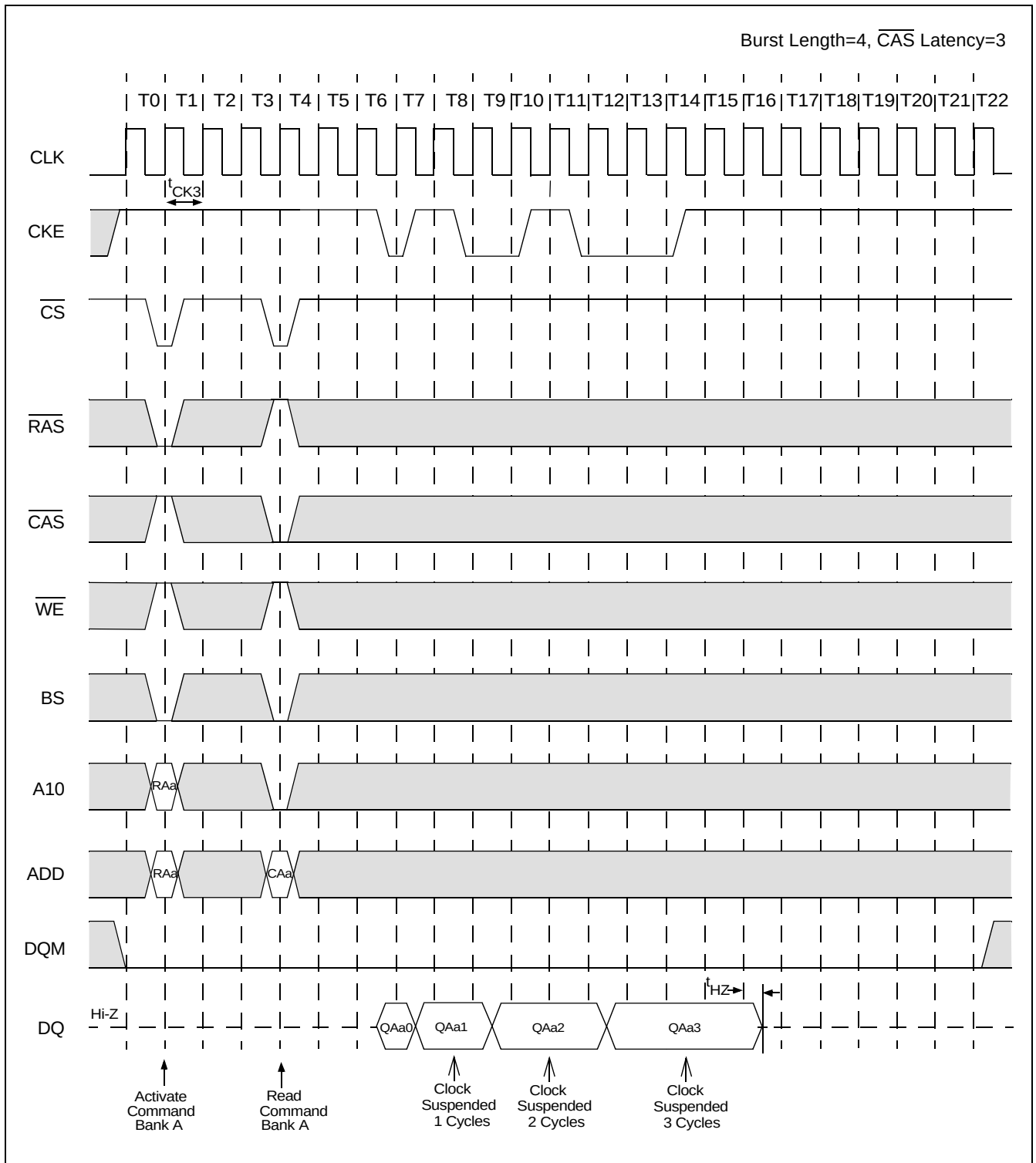
Power on Sequence and Auto Refresh (CBR)



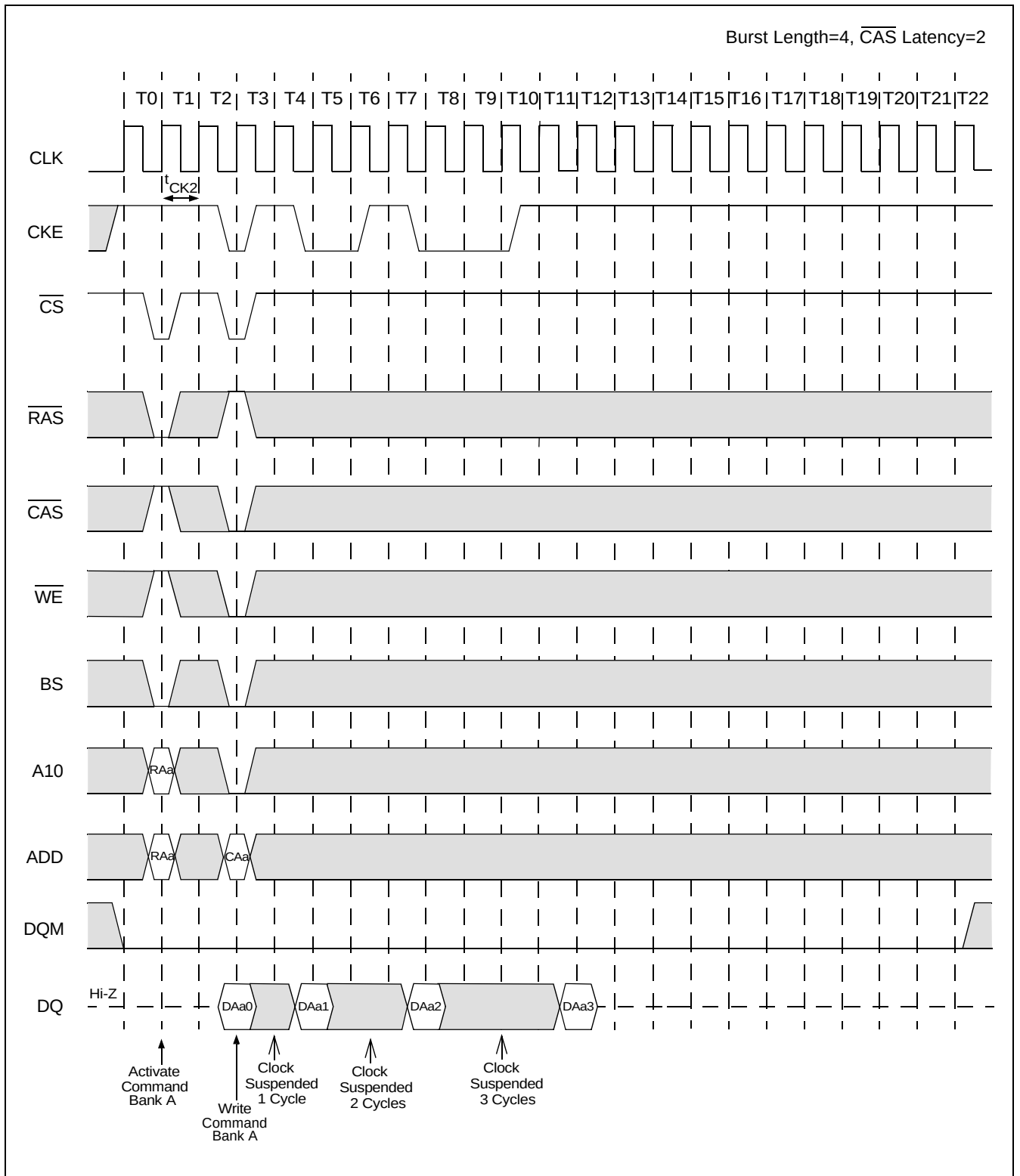
Clock Suspension During Burst Read (Using CKE) (1 of 2)



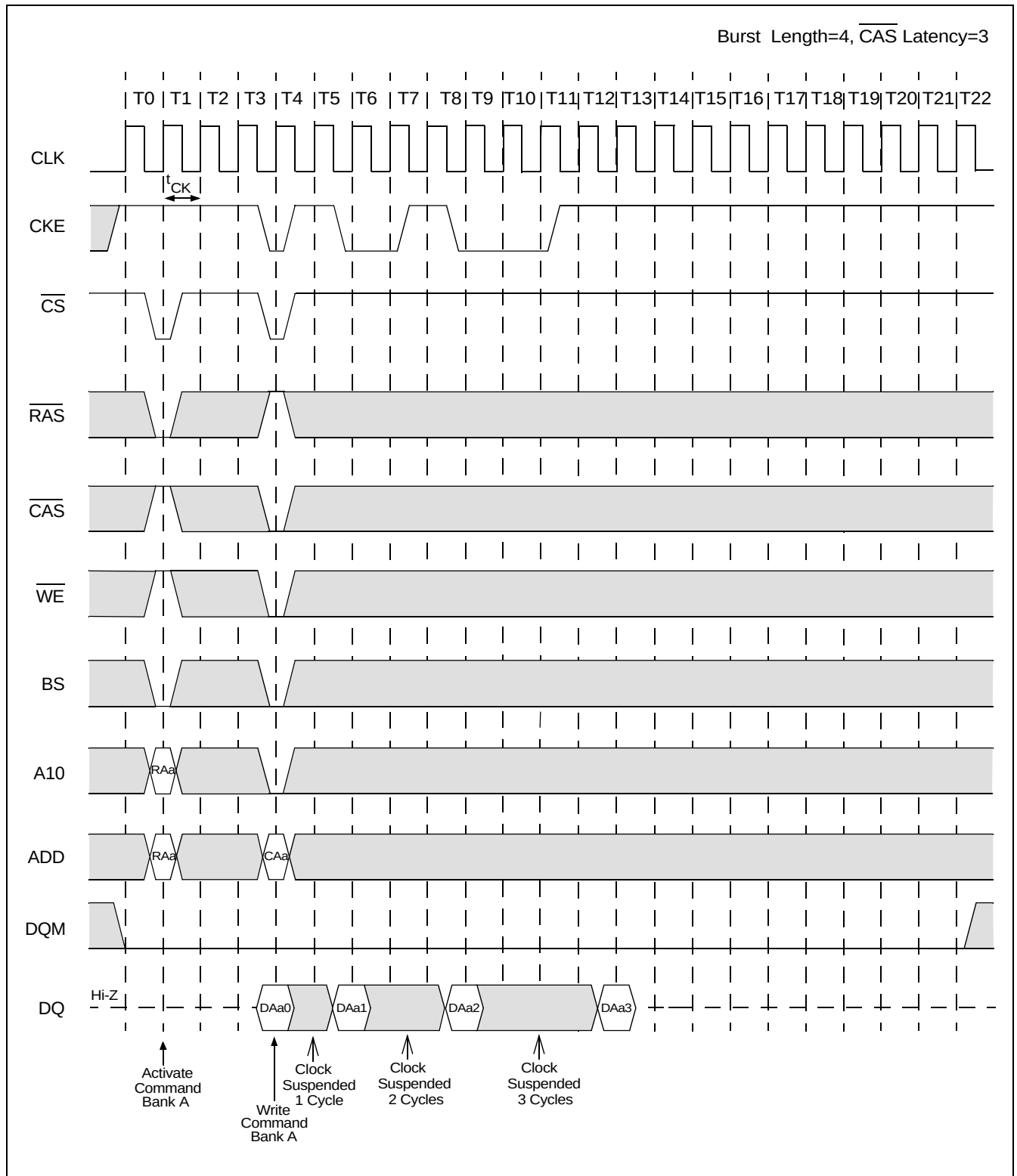
Clock Suspension During Burst Read (Using CKE) (2 of 2)



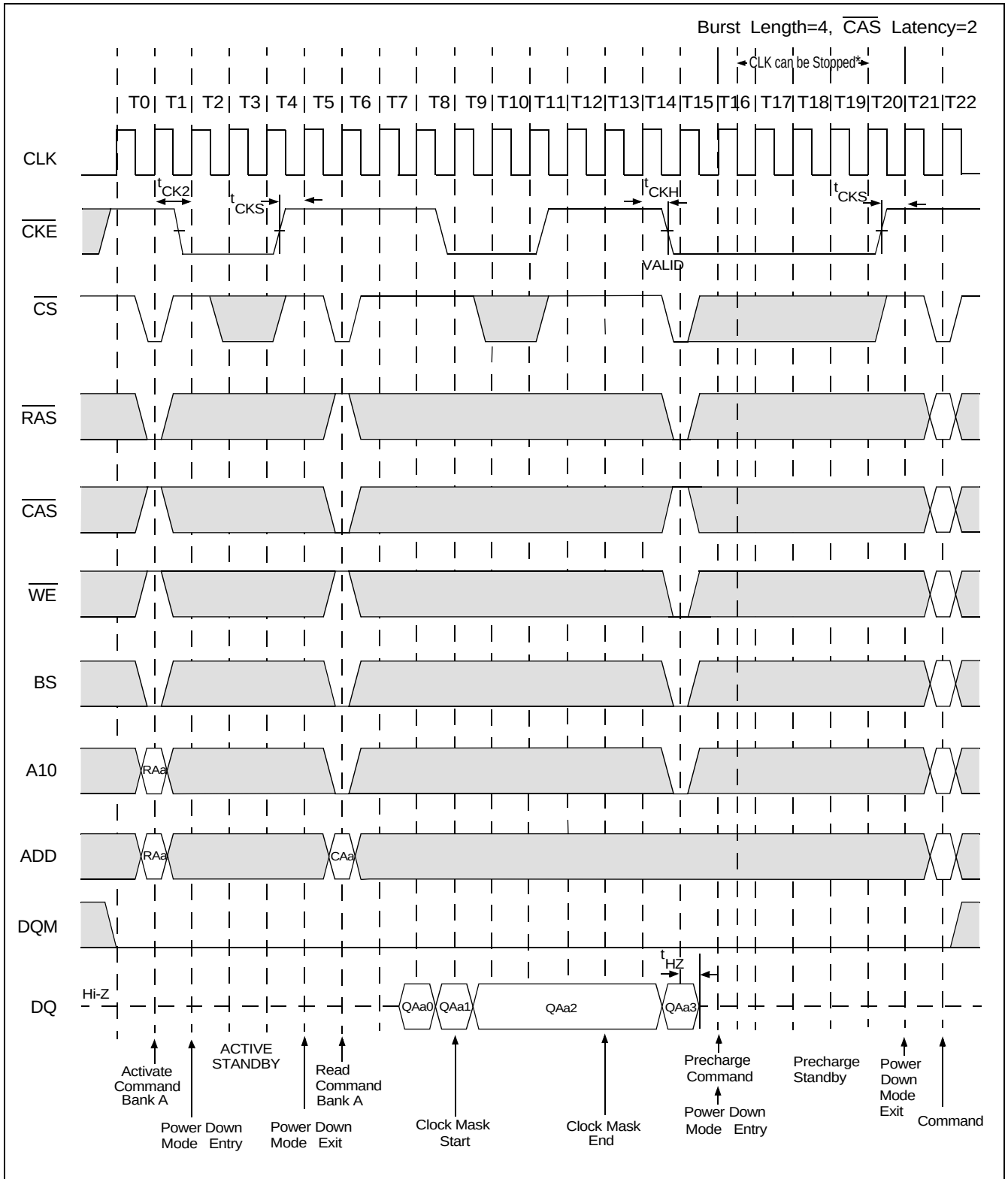
Clock Suspension During Burst Write (Using CKE) (1 of 2)



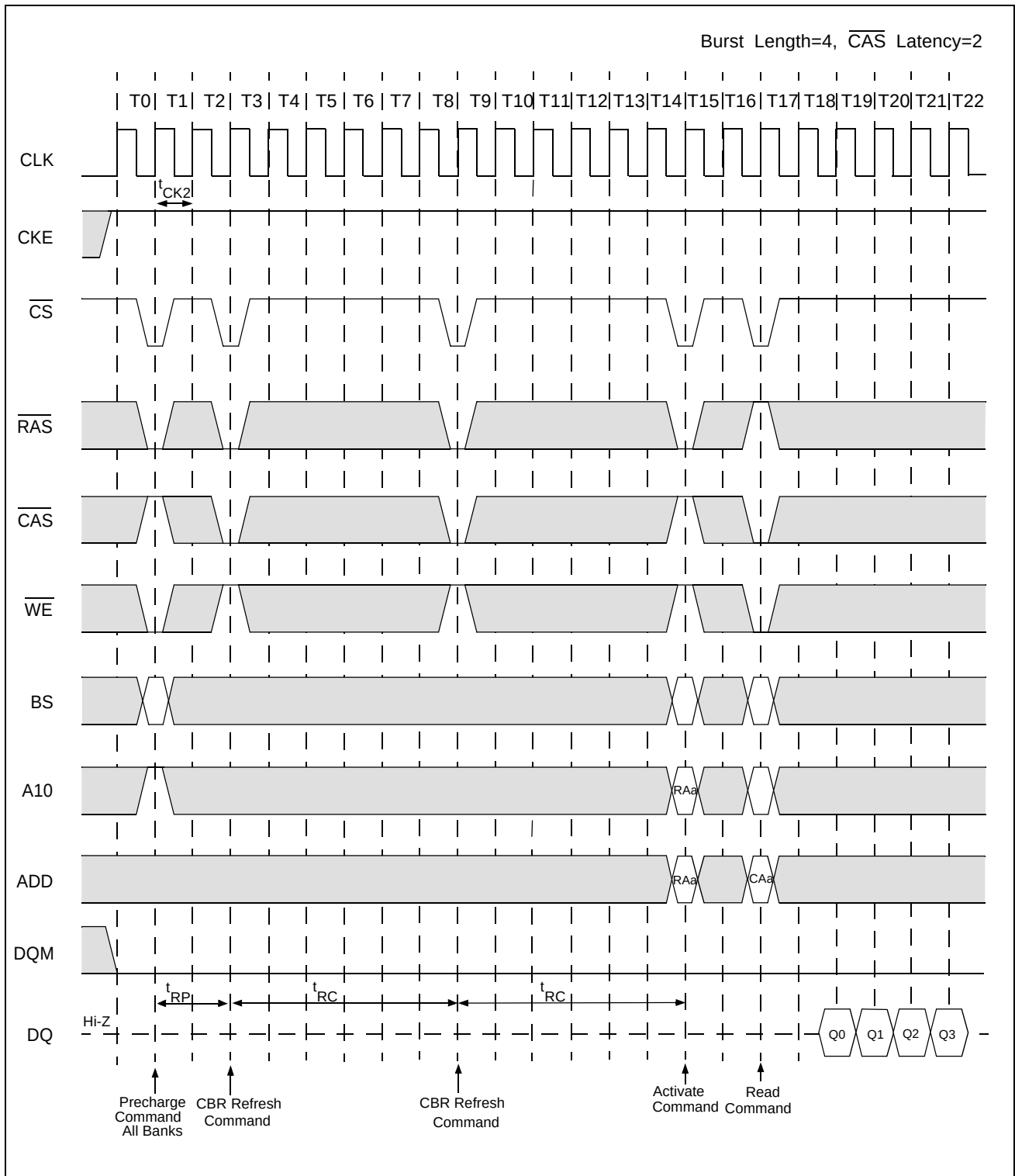
Clock Suspension During Burst Write (Using CKE) (2 of 2)



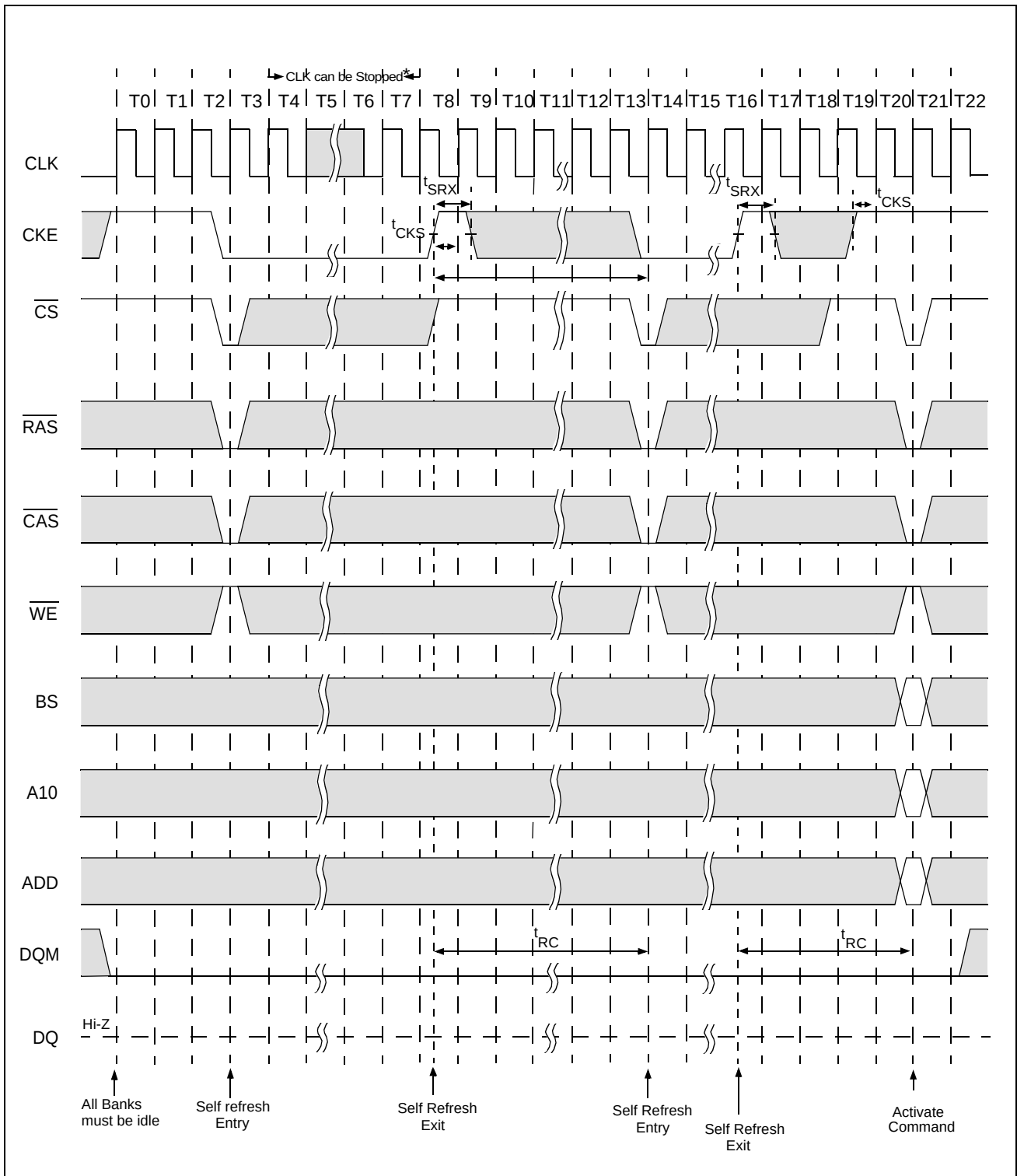
Power Down Mode and Clock Mask



Auto Refresh (CBR)

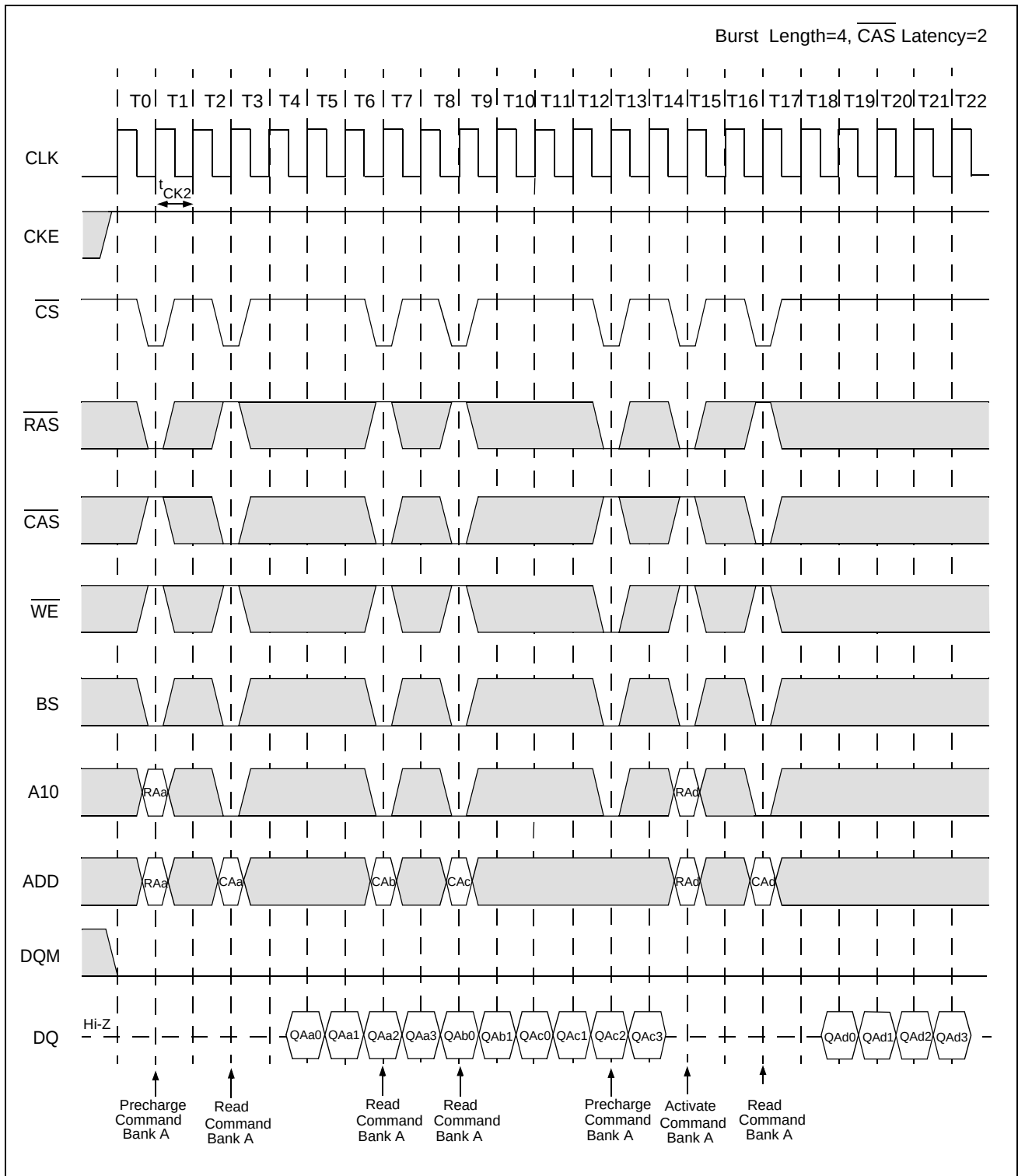


Self Refresh (Entry and Exit)

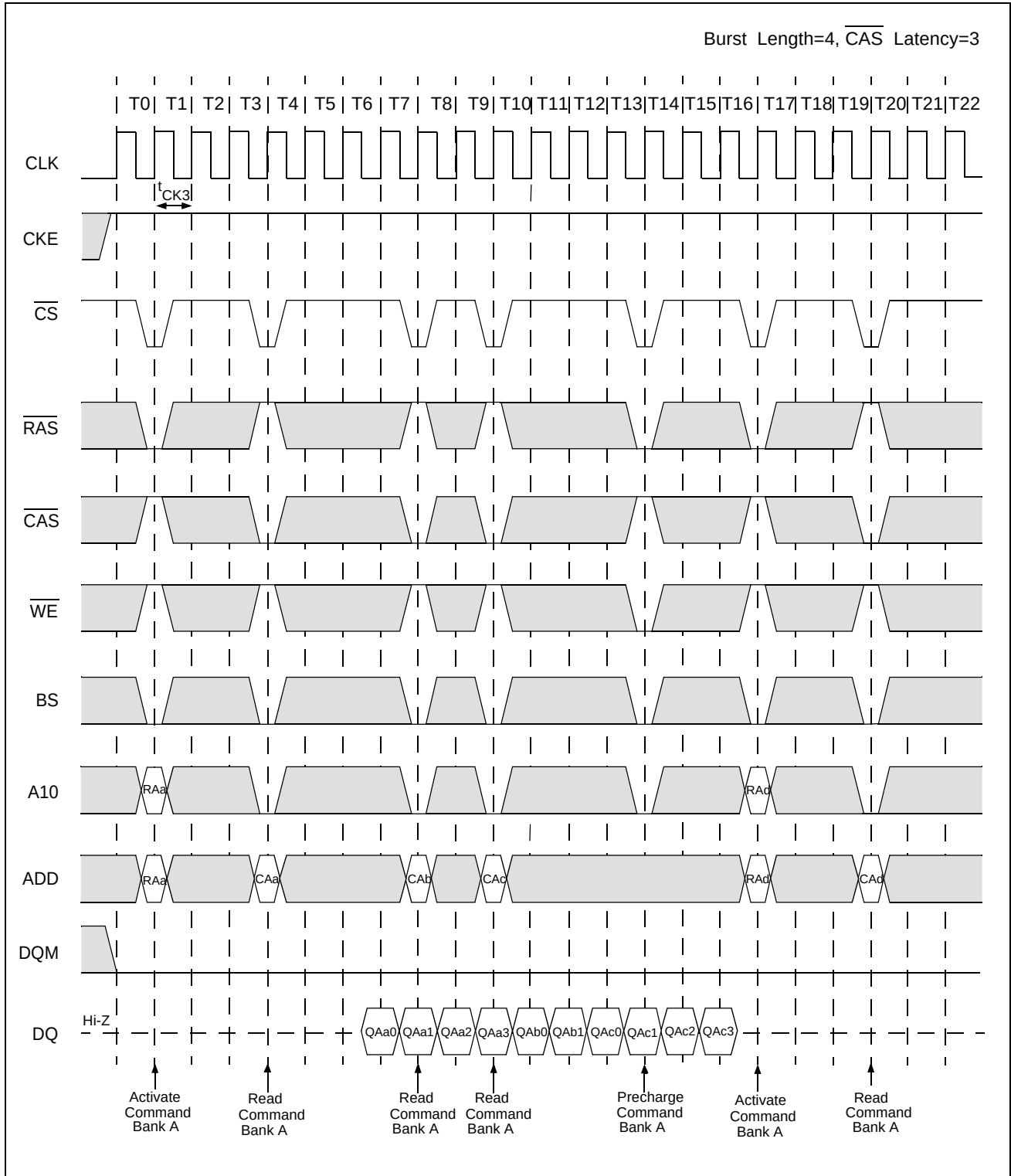


* Clock can be stopped at CKE=Low. If clock is stopped, it must be restarted/stable for 4 clock cycles before CKE=High

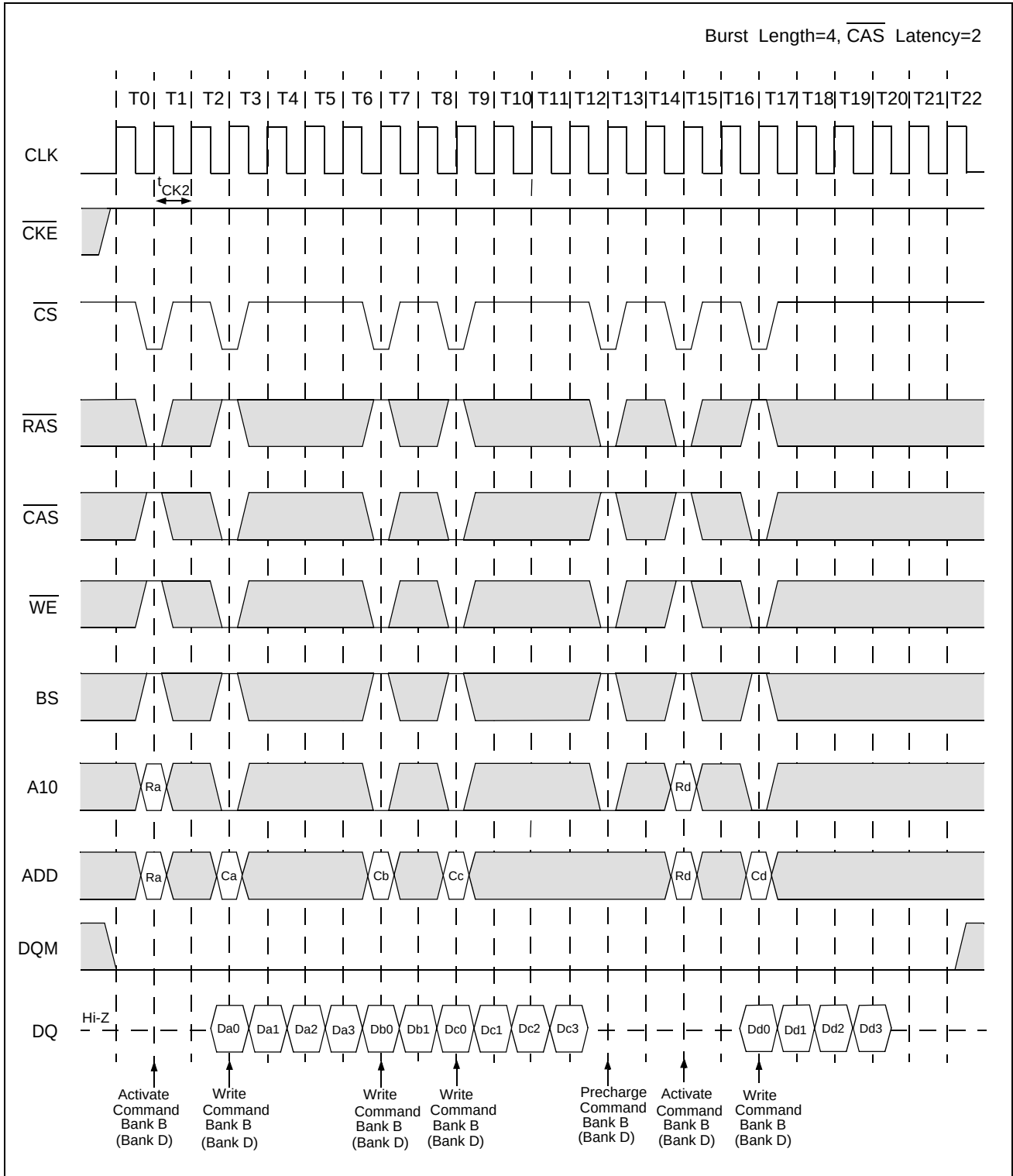
Random Column Read (Page Within same Bank)(1 of 2)



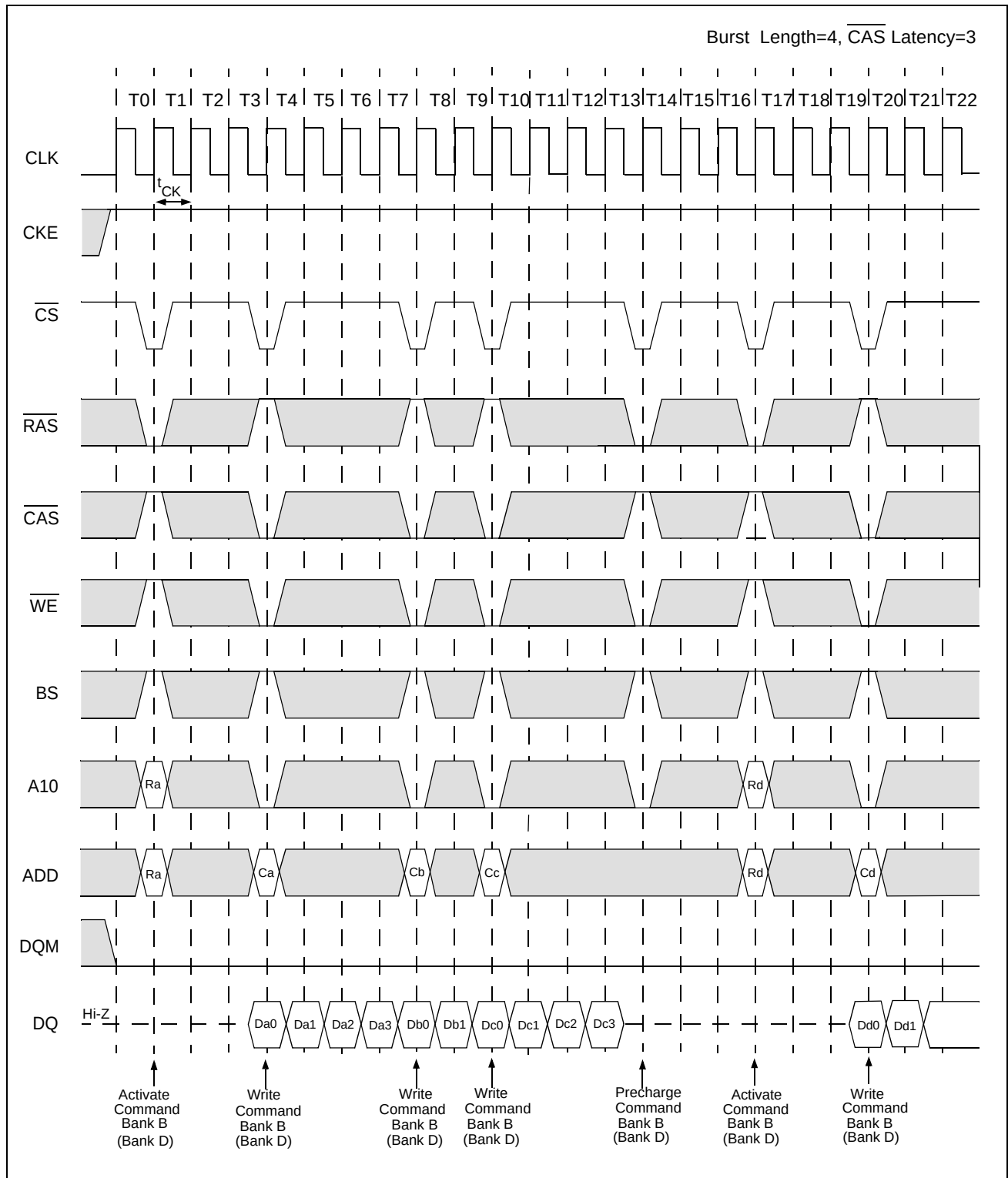
Random Column Read (Page Within same Bank)(2 of 2)



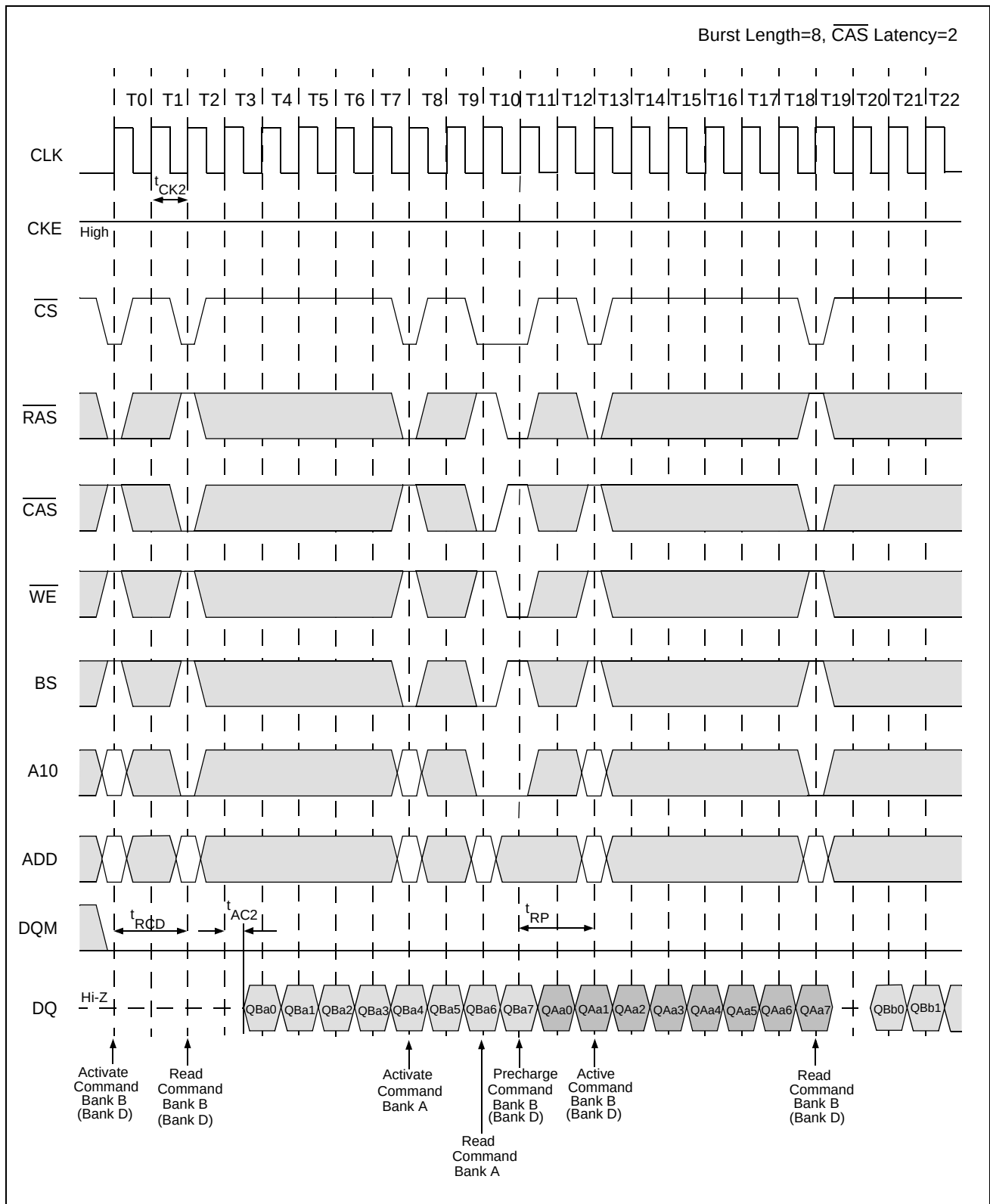
Random Column Write (Page Within same Bank) (1 of 2)



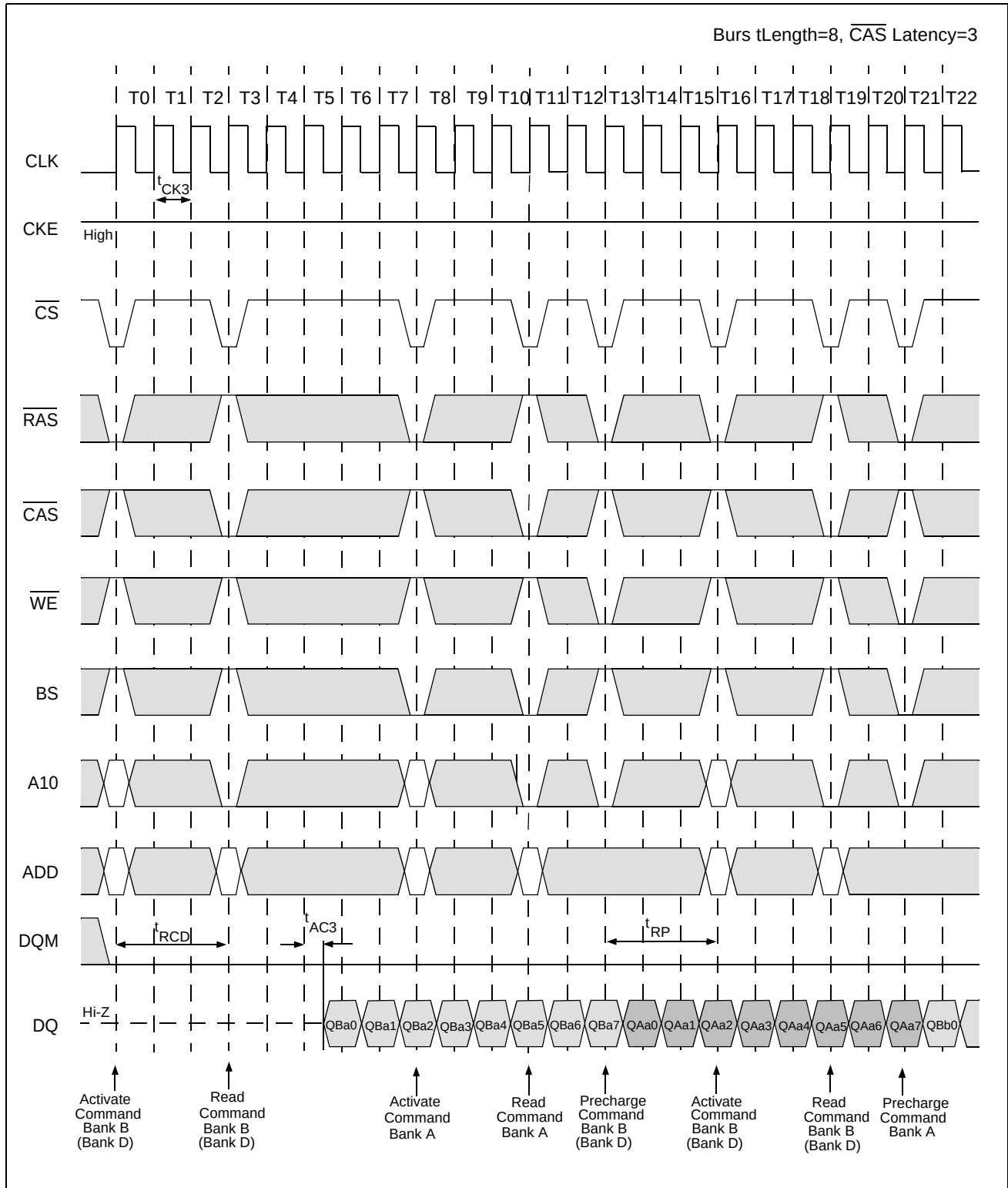
Random Column Write (Page Within same Bank) (1 of 2)



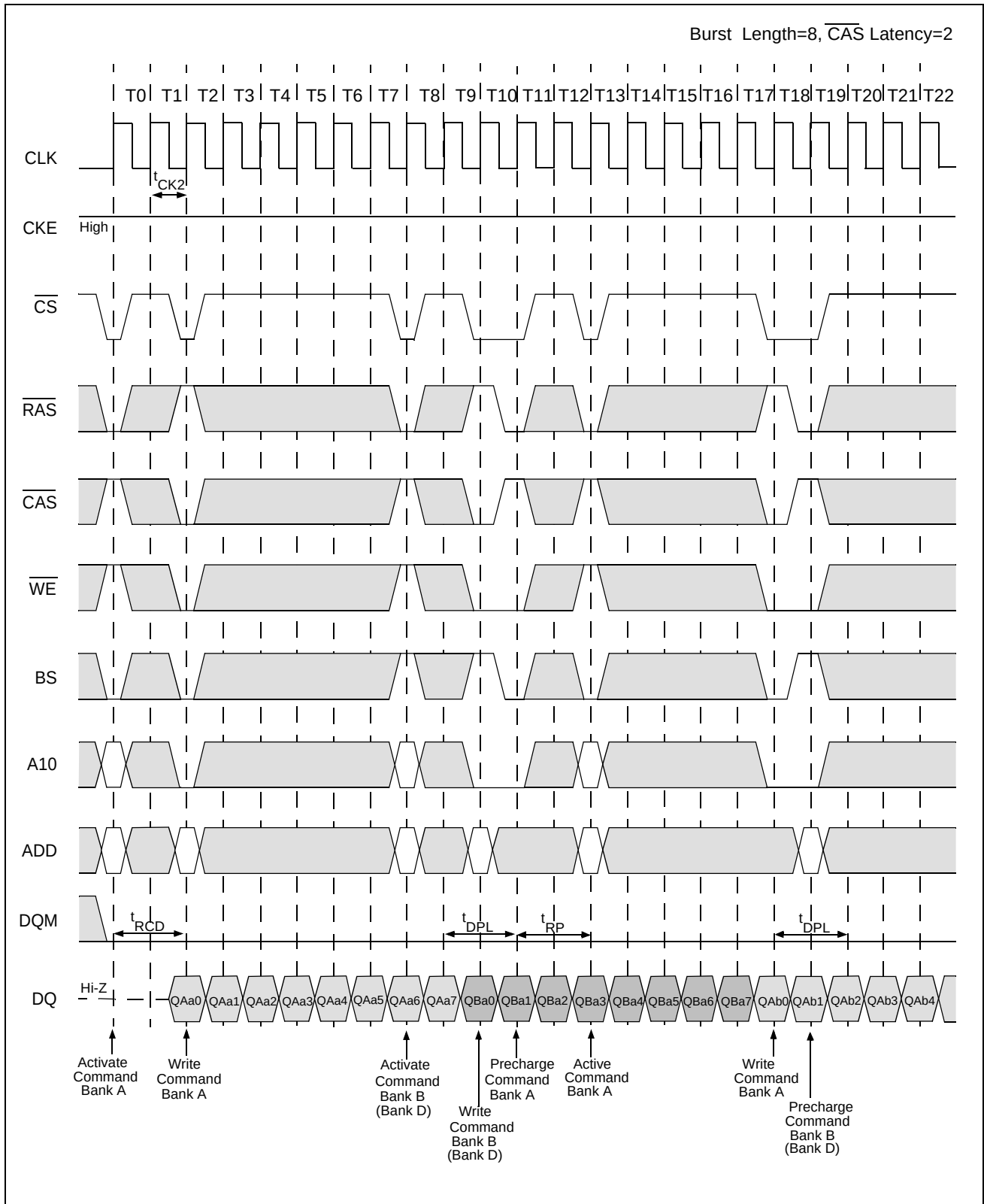
Random Row Read (Interleaving Banks)(1 of 2)



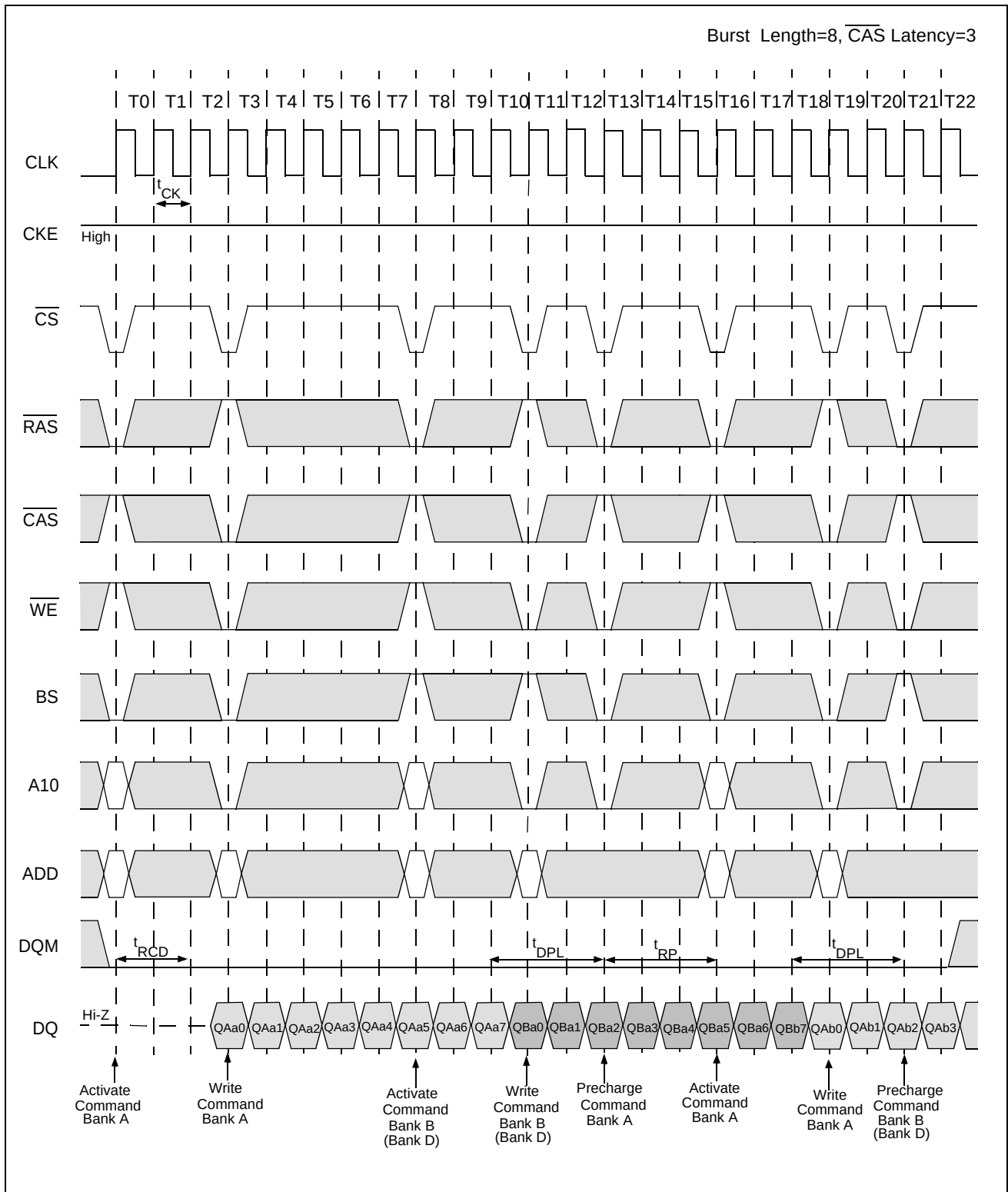
Random Row Read (Interleaving Banks) (2 of 3)



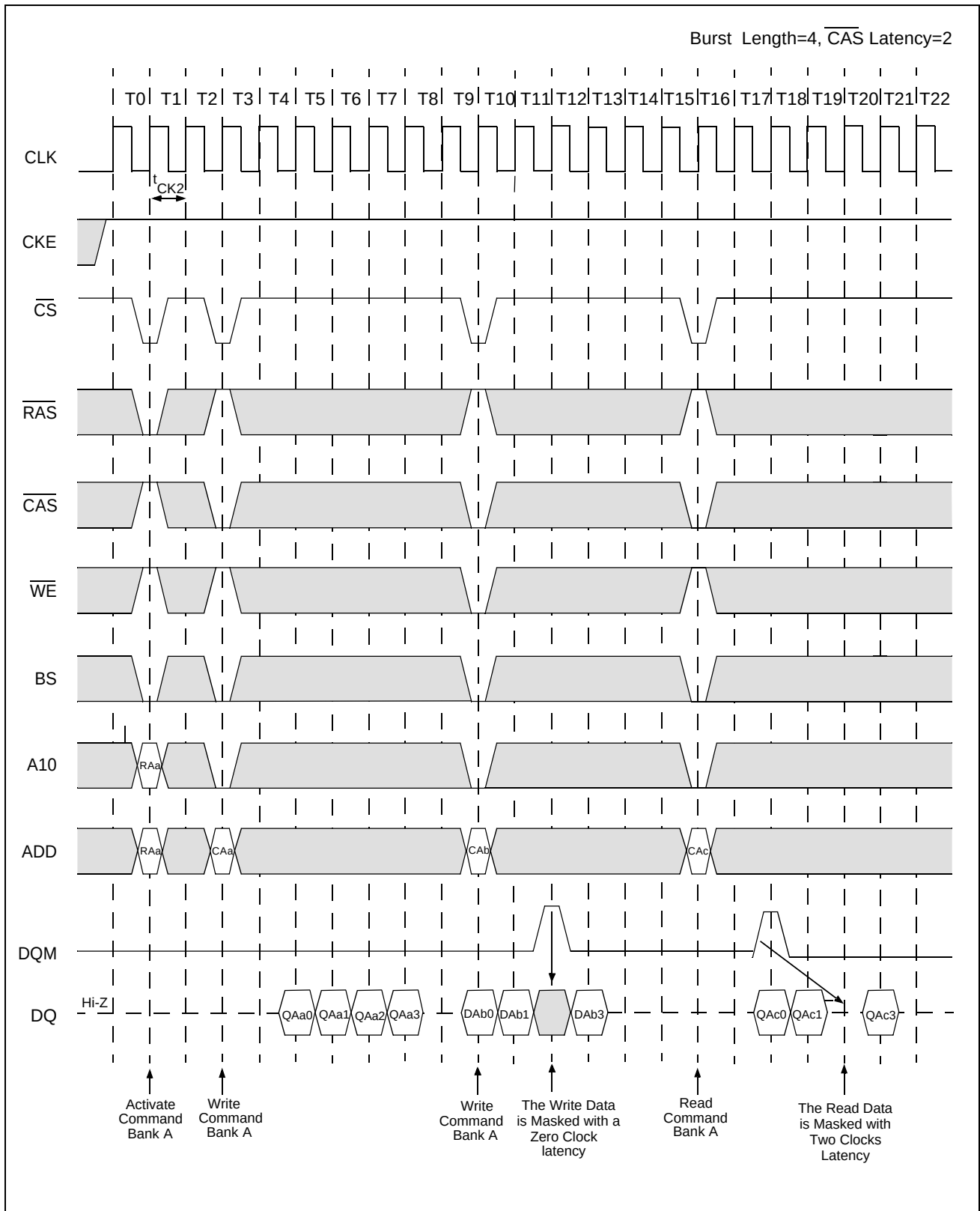
Random Row Write (Interleaving Banks) (1 of 2)



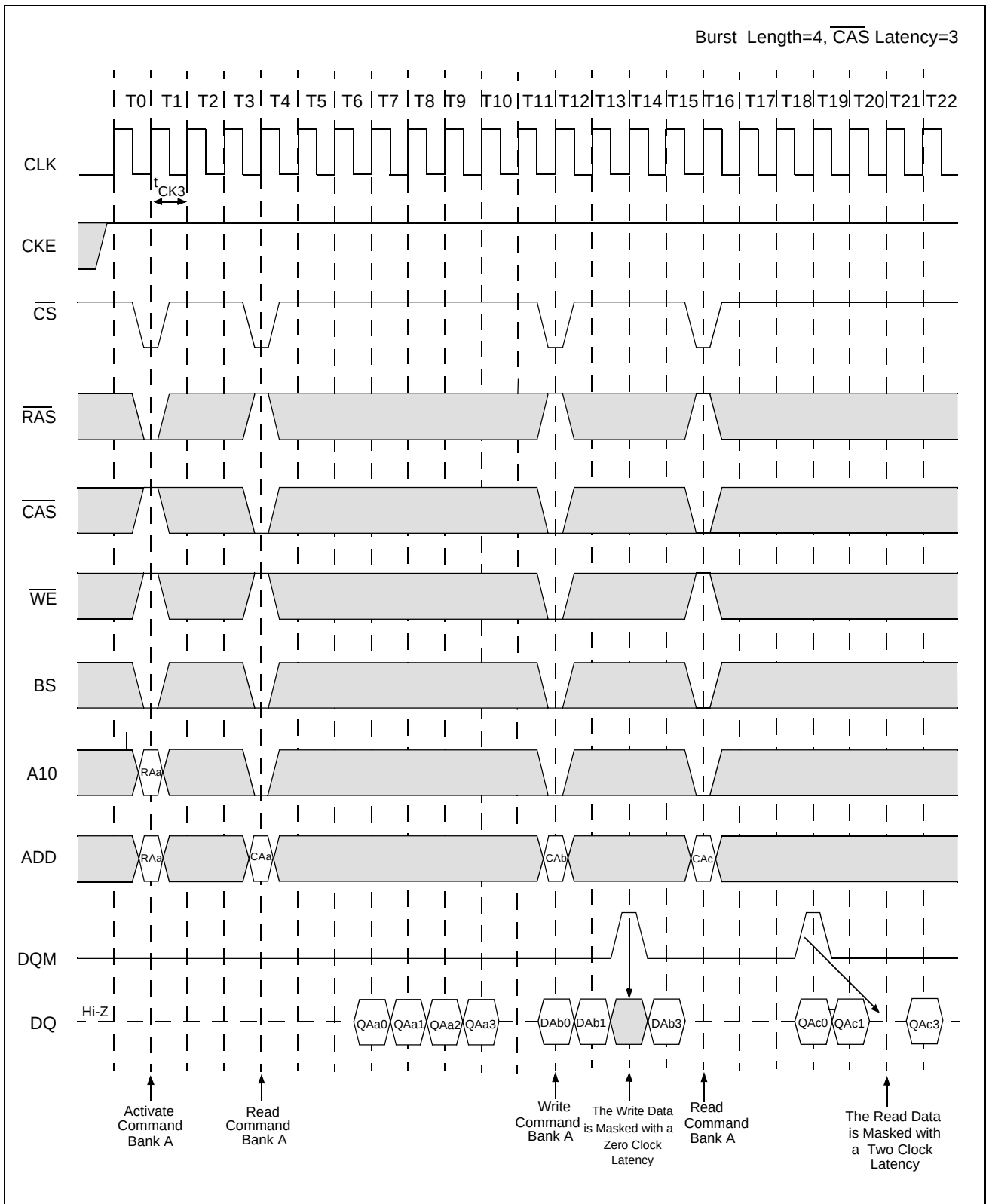
Random Row Write (Interleaving Banks) (2 of 2)



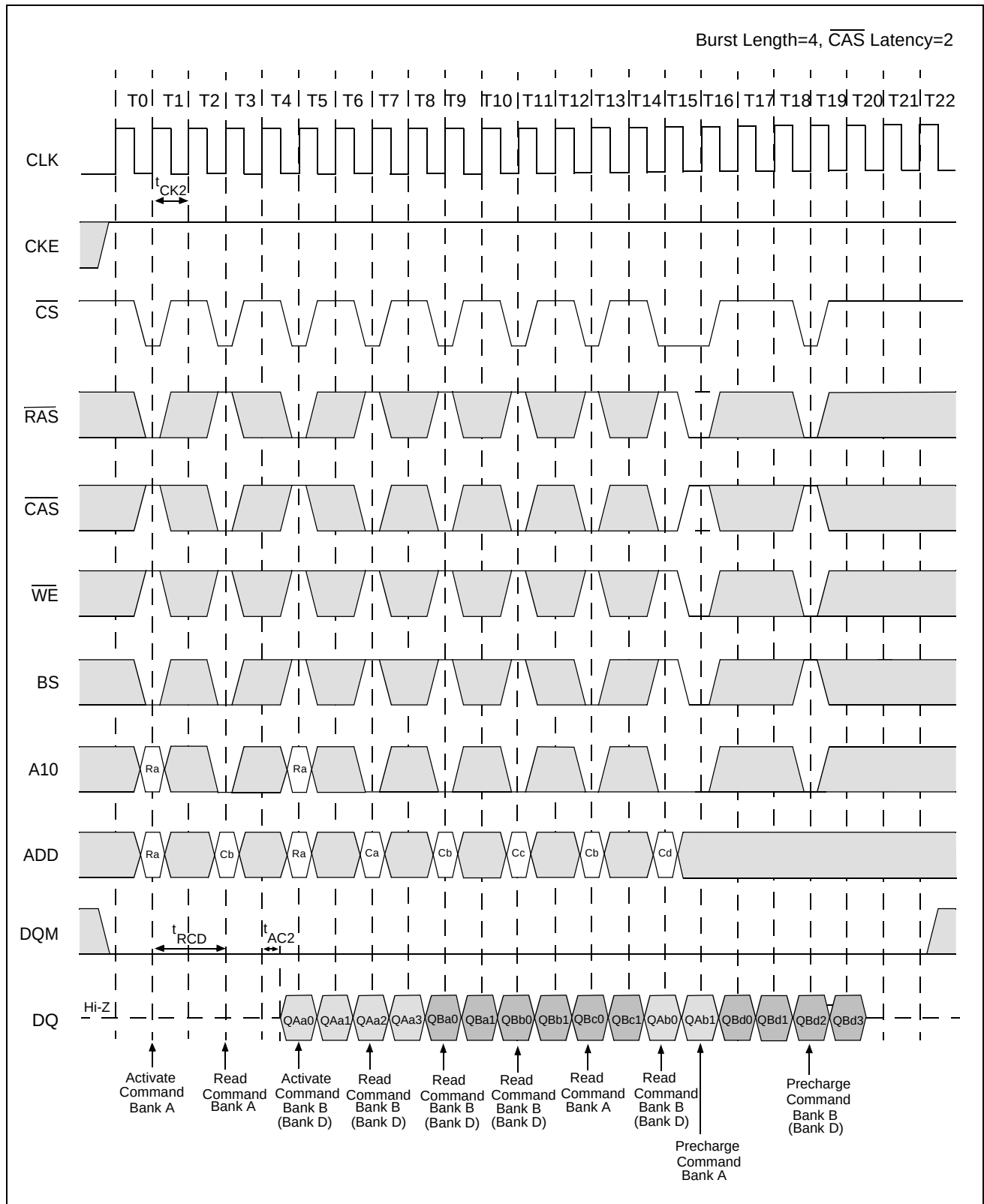
Read and Write Cycle (1 of 2)



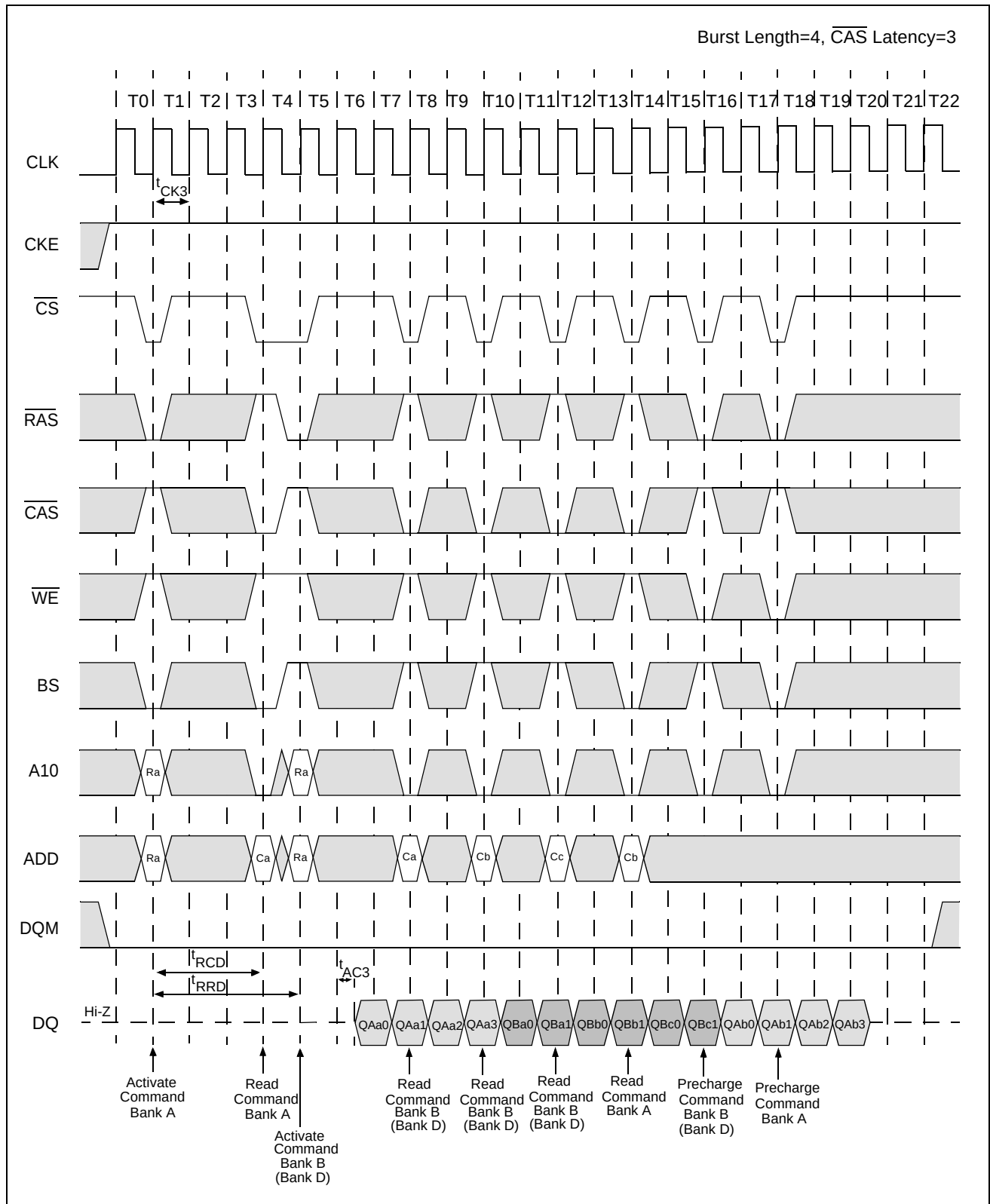
Read and Write Cycle (2 of 2)



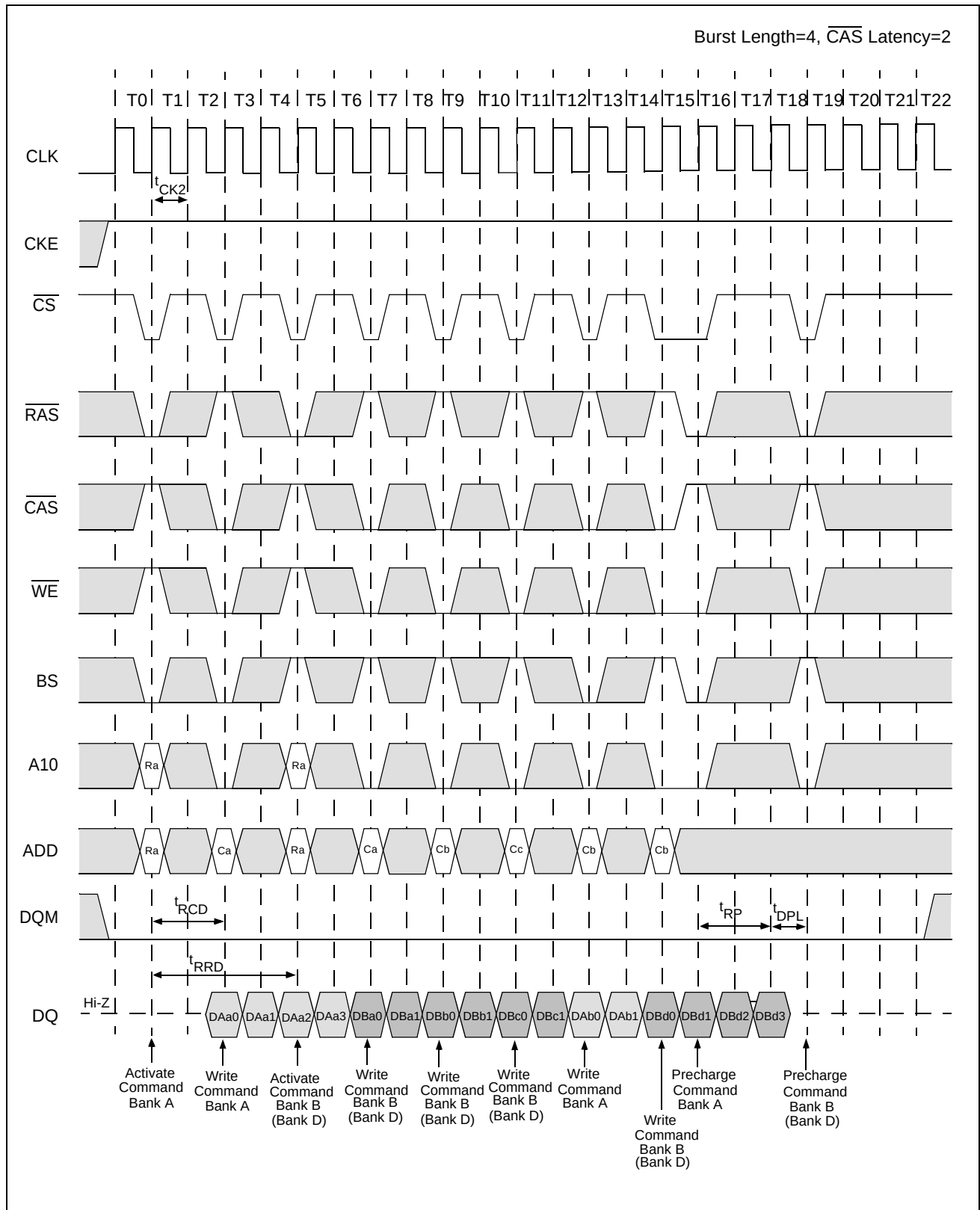
Interleaved Column Read Cycle (1 of 2)



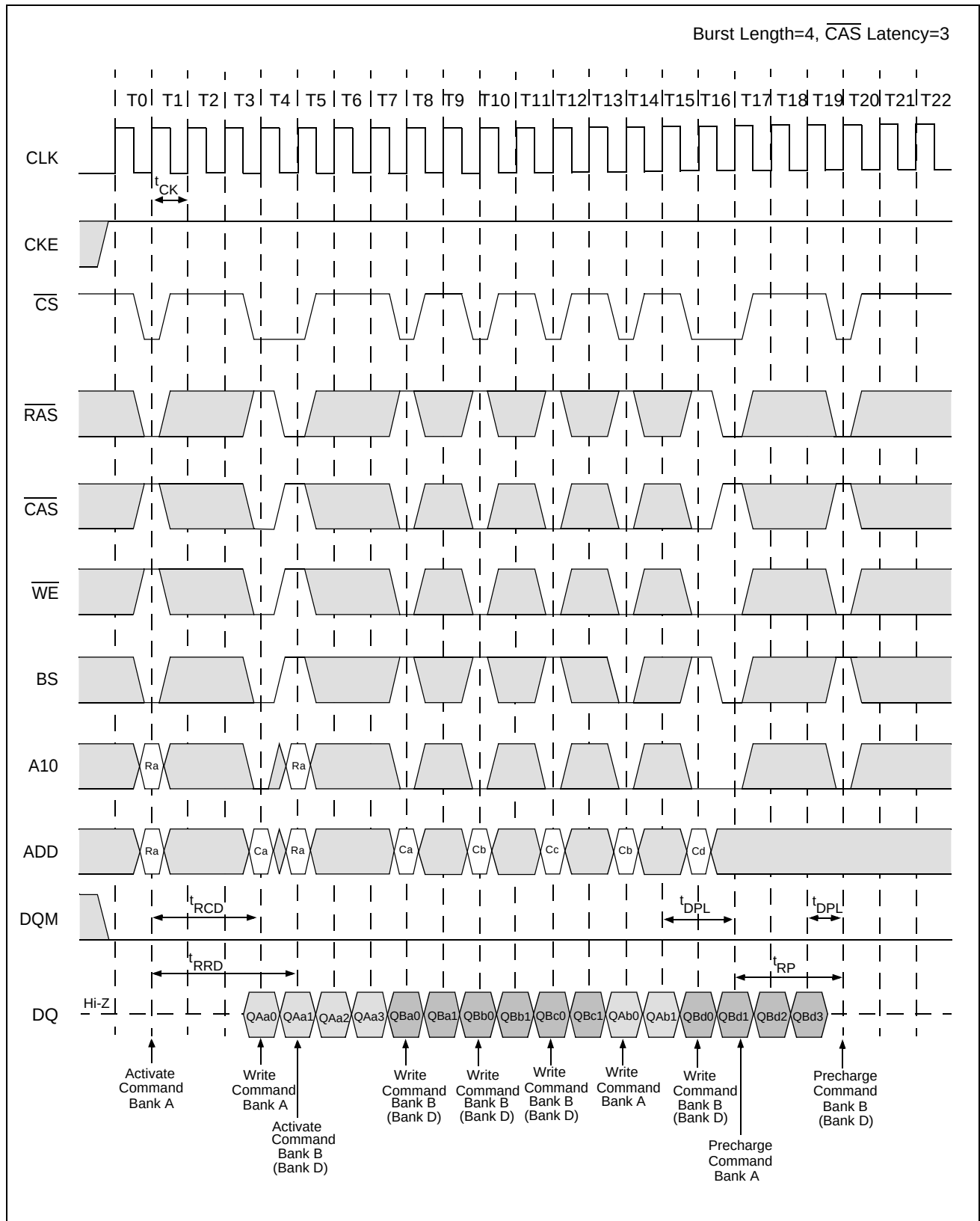
Interleaved Column Read Cycle (2 of 2)



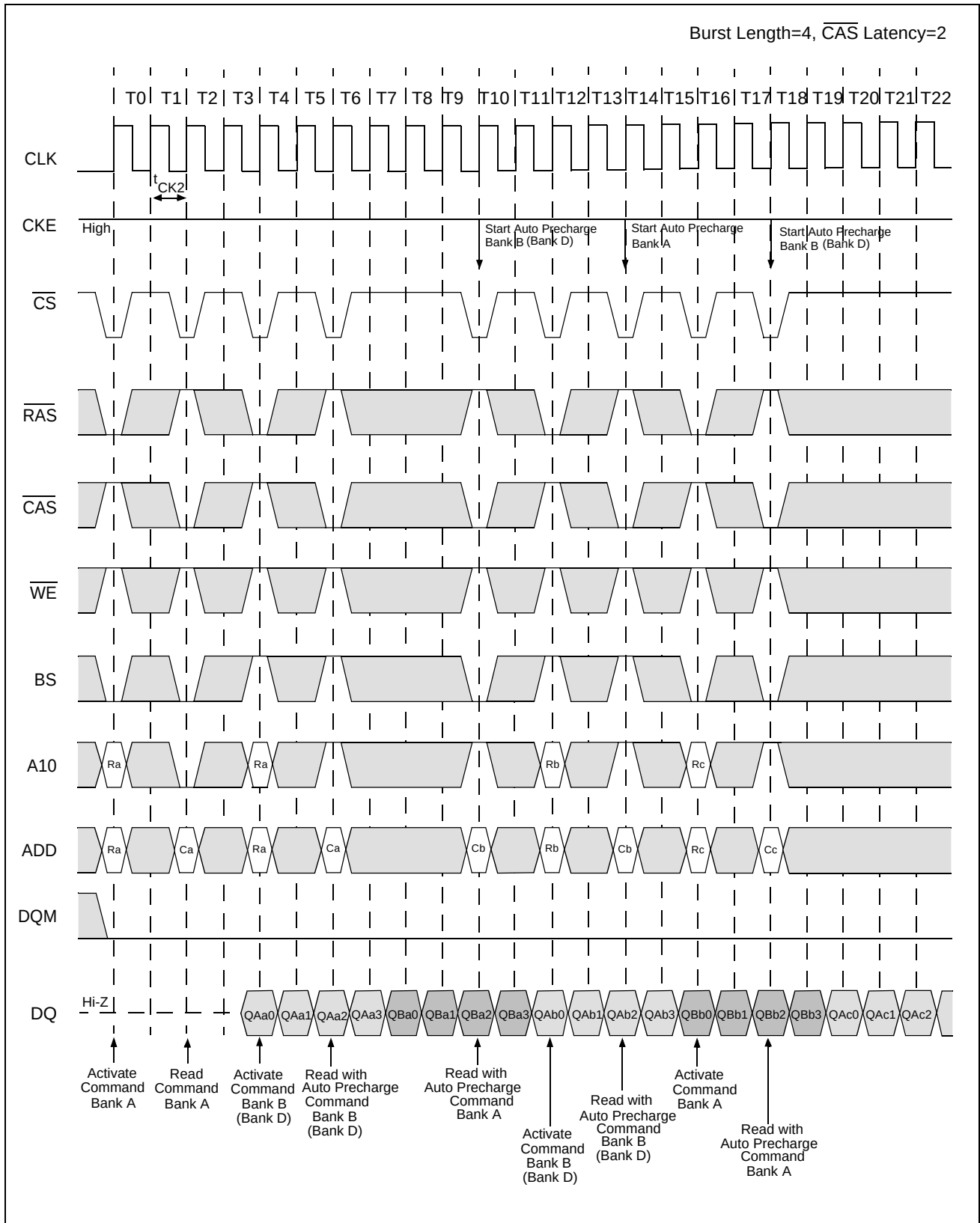
Interleaved Column Write Cycle (1 of 2)



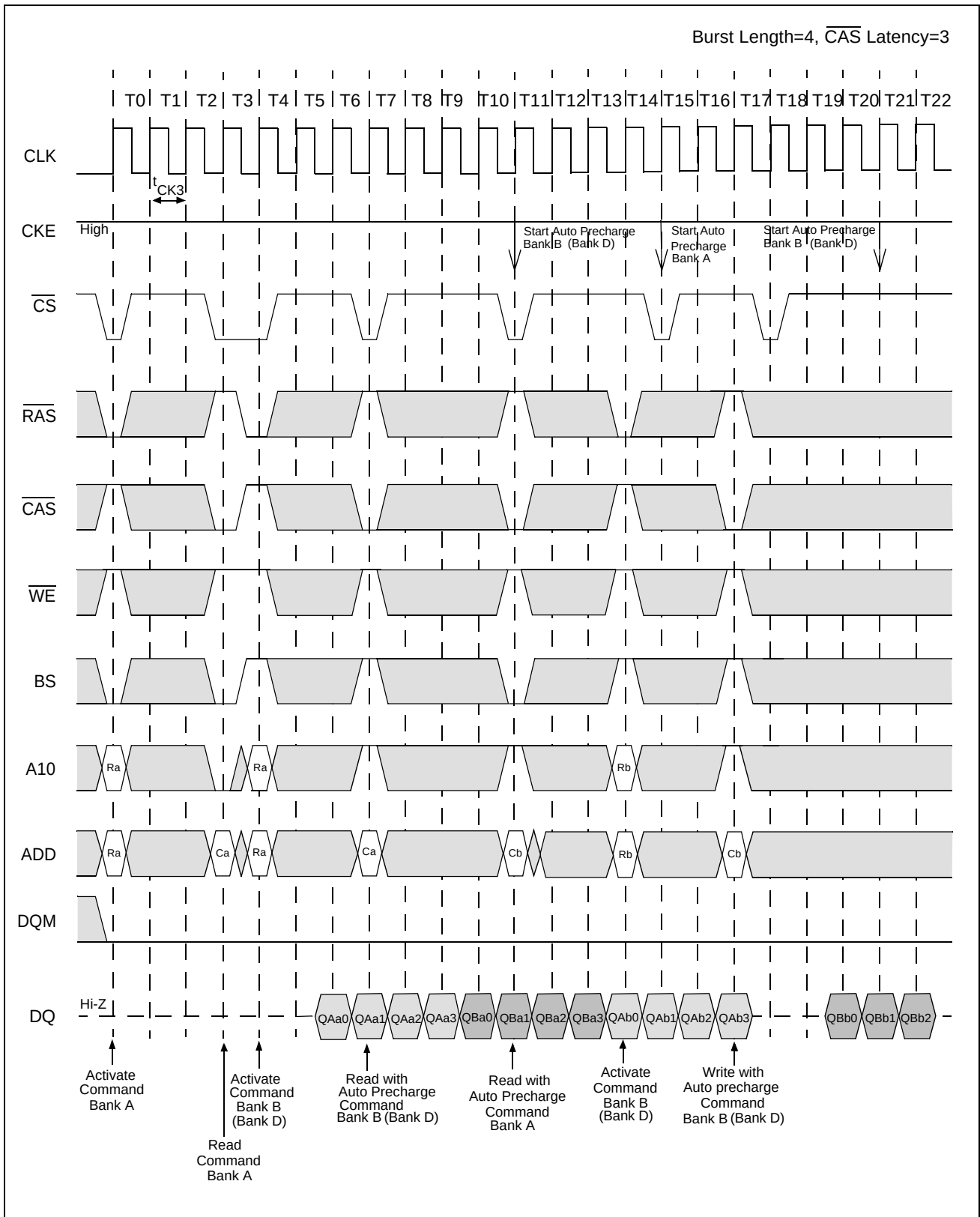
Interleaved Column Write Cycle (2 of 2)



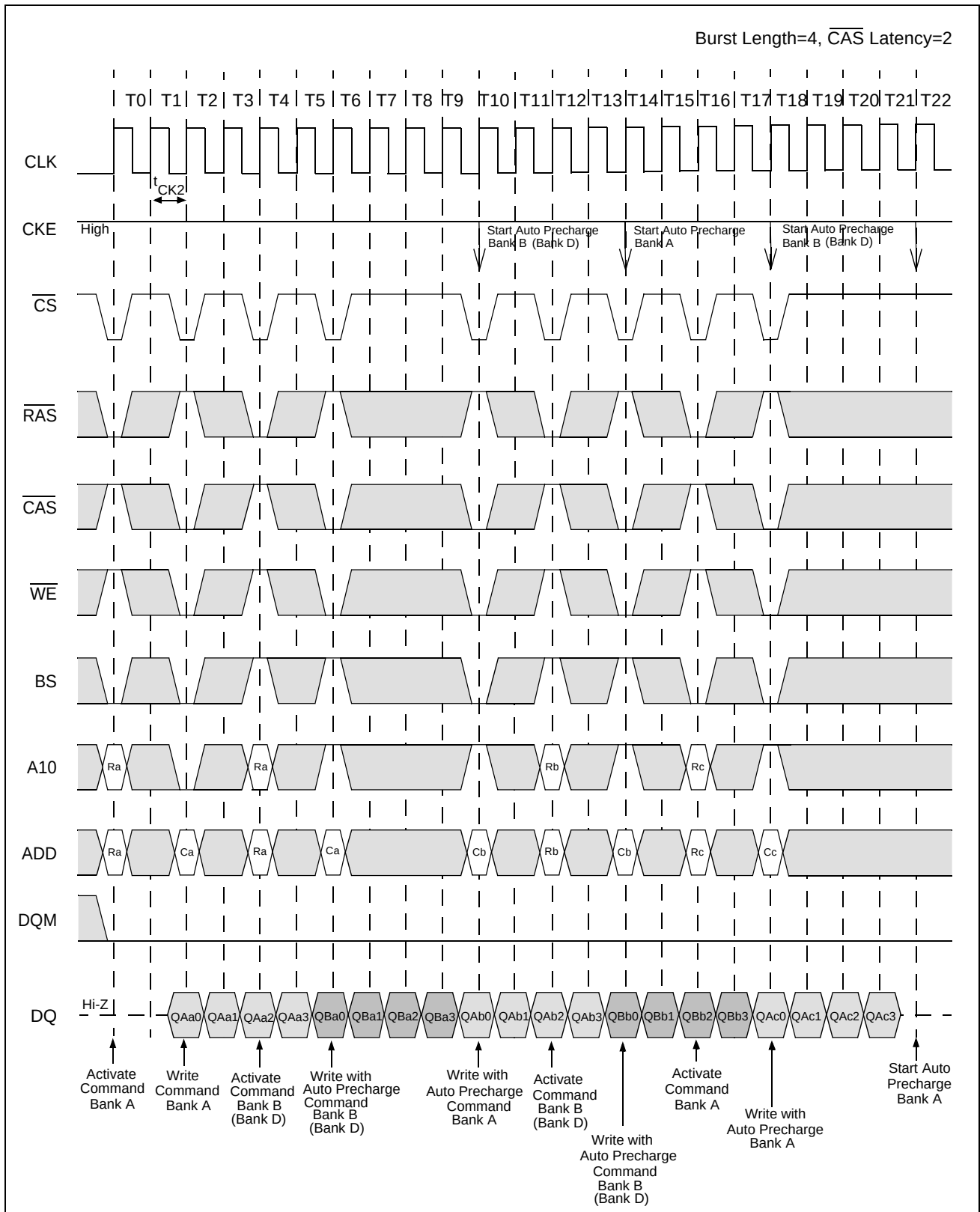
Auto Precharge after Read Burst (1 of 2)



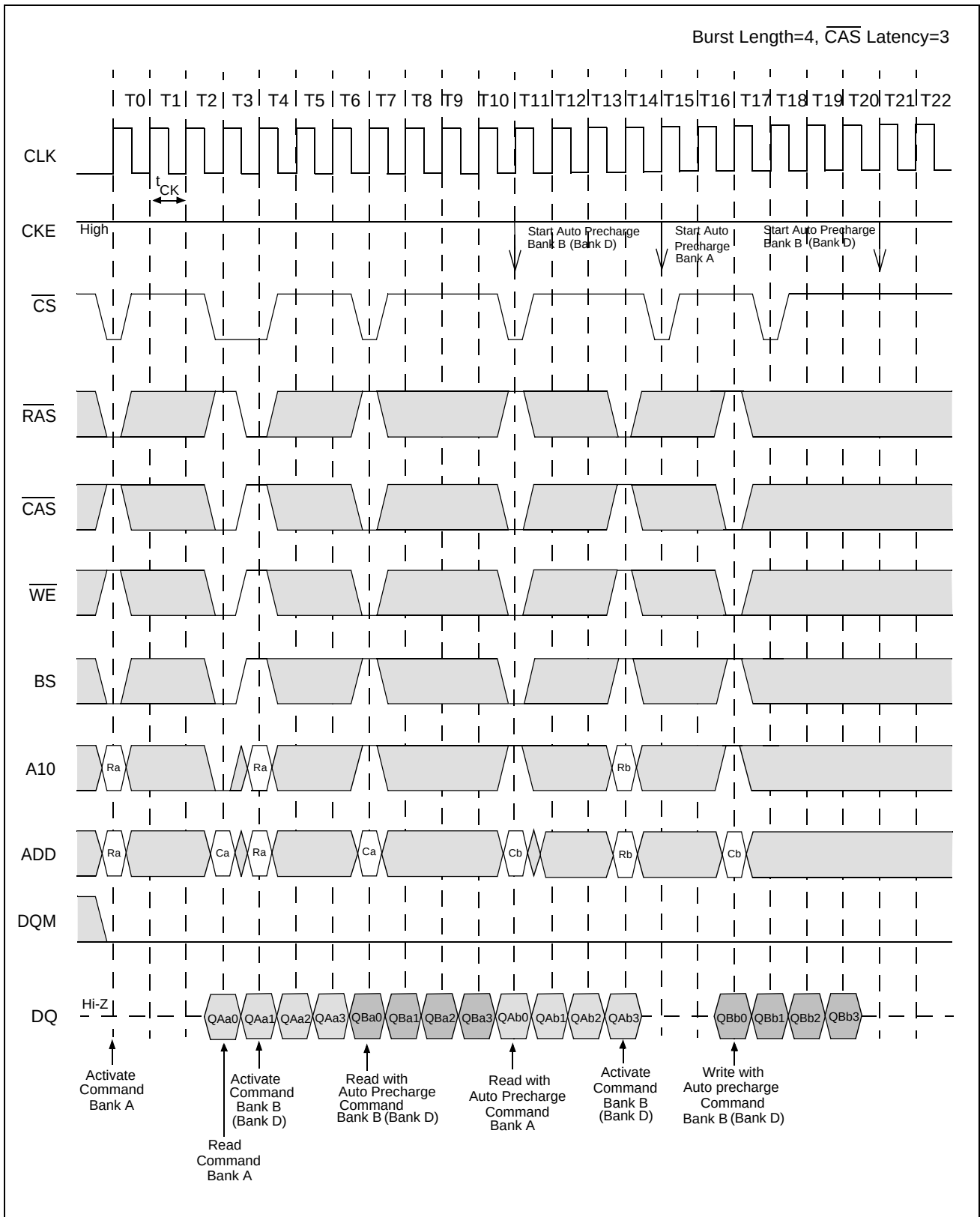
Auto Precharge after Write Burst (2 of 2)



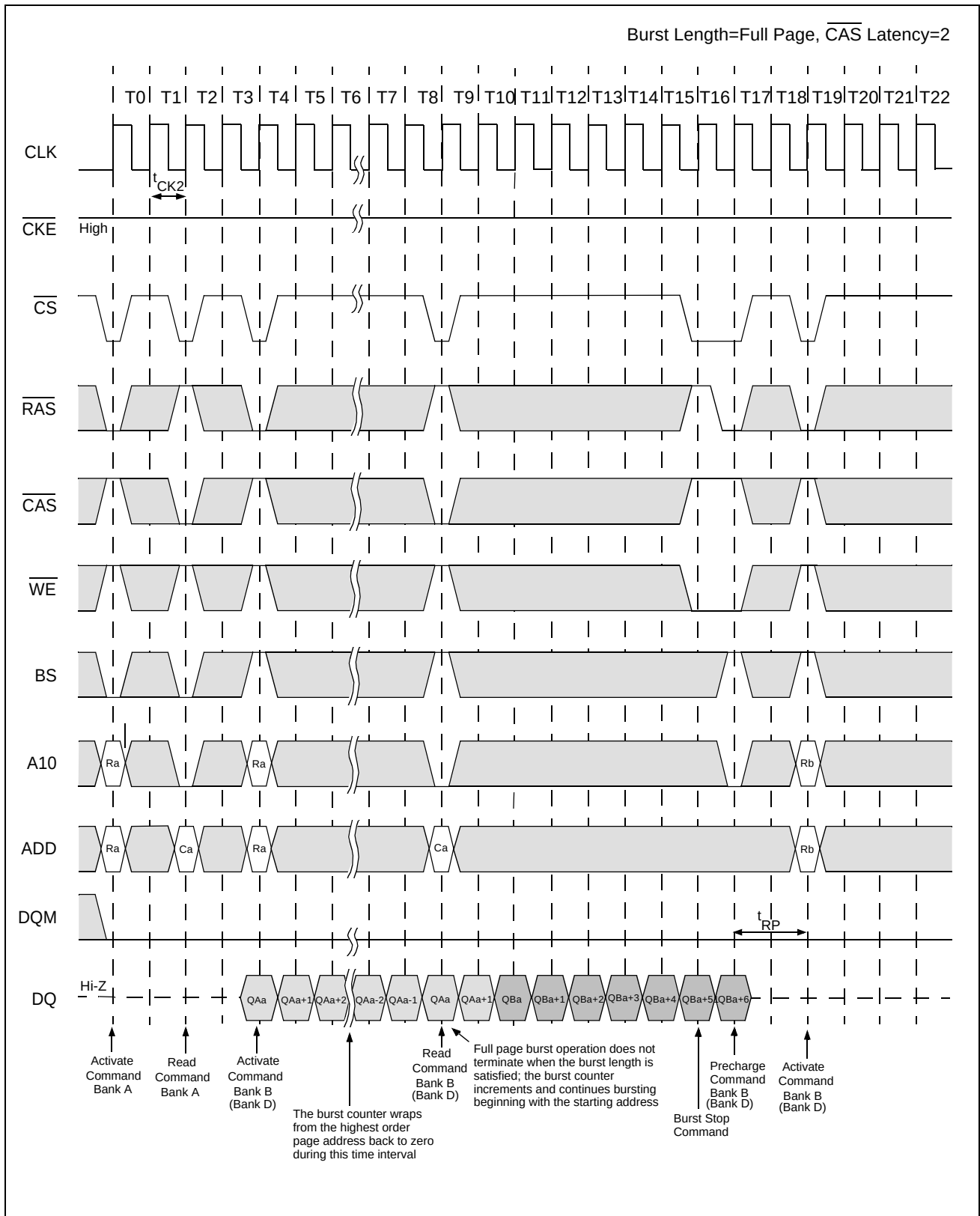
Auto Precharge after Write Burst (1 of 2)



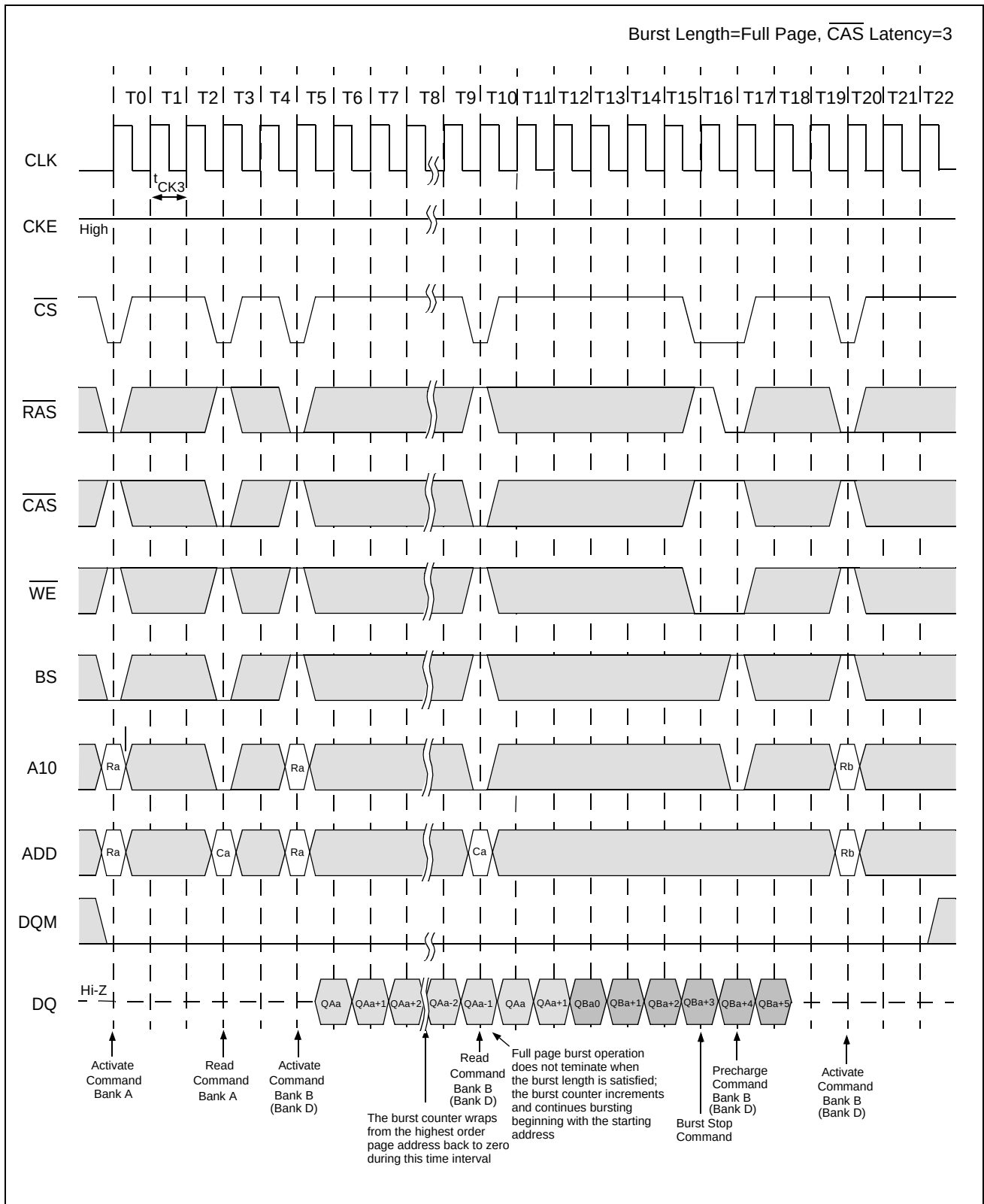
Auto Precharge after Write Burst (2 of 2)



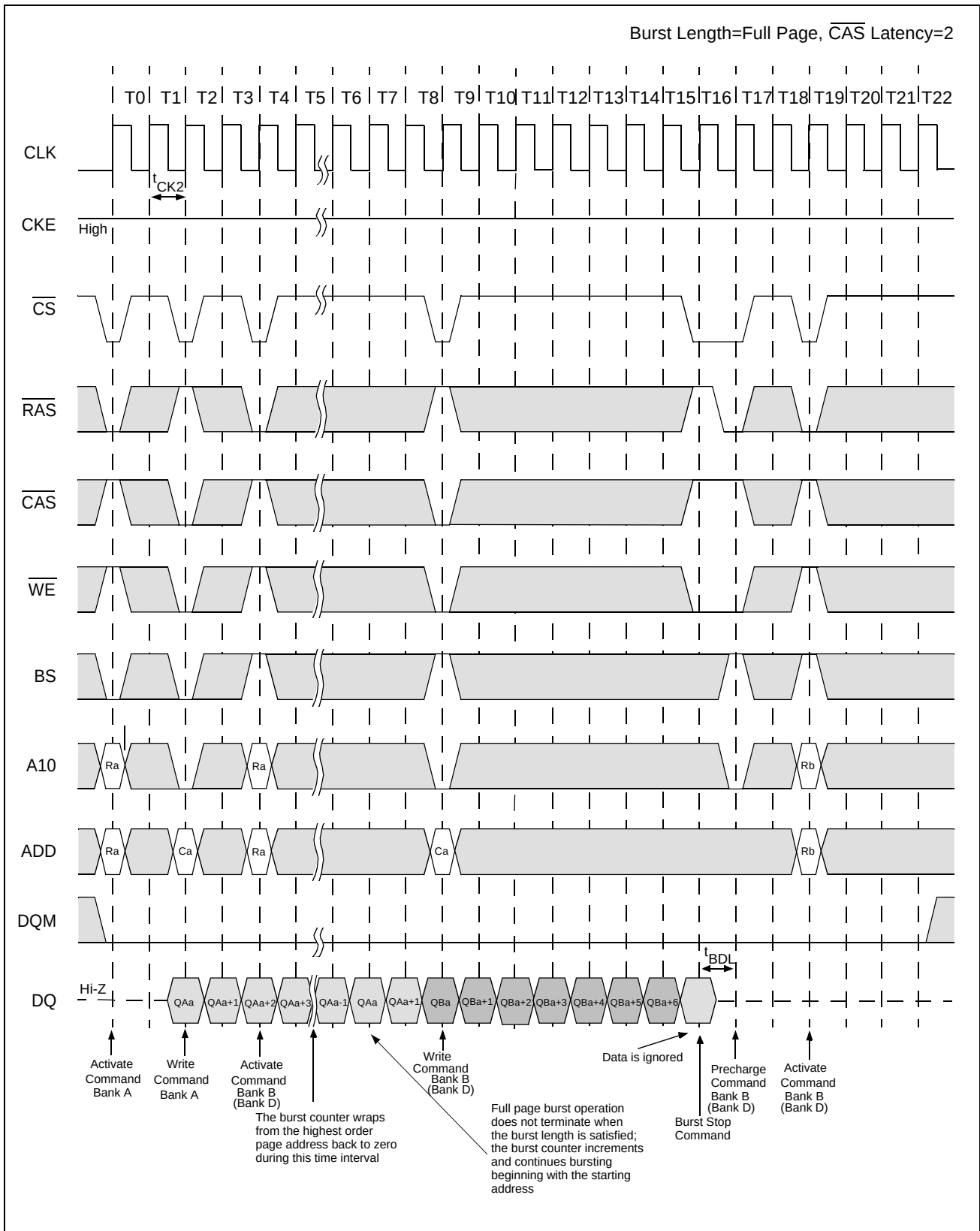
Full Page Read Cycle (1 of 2)



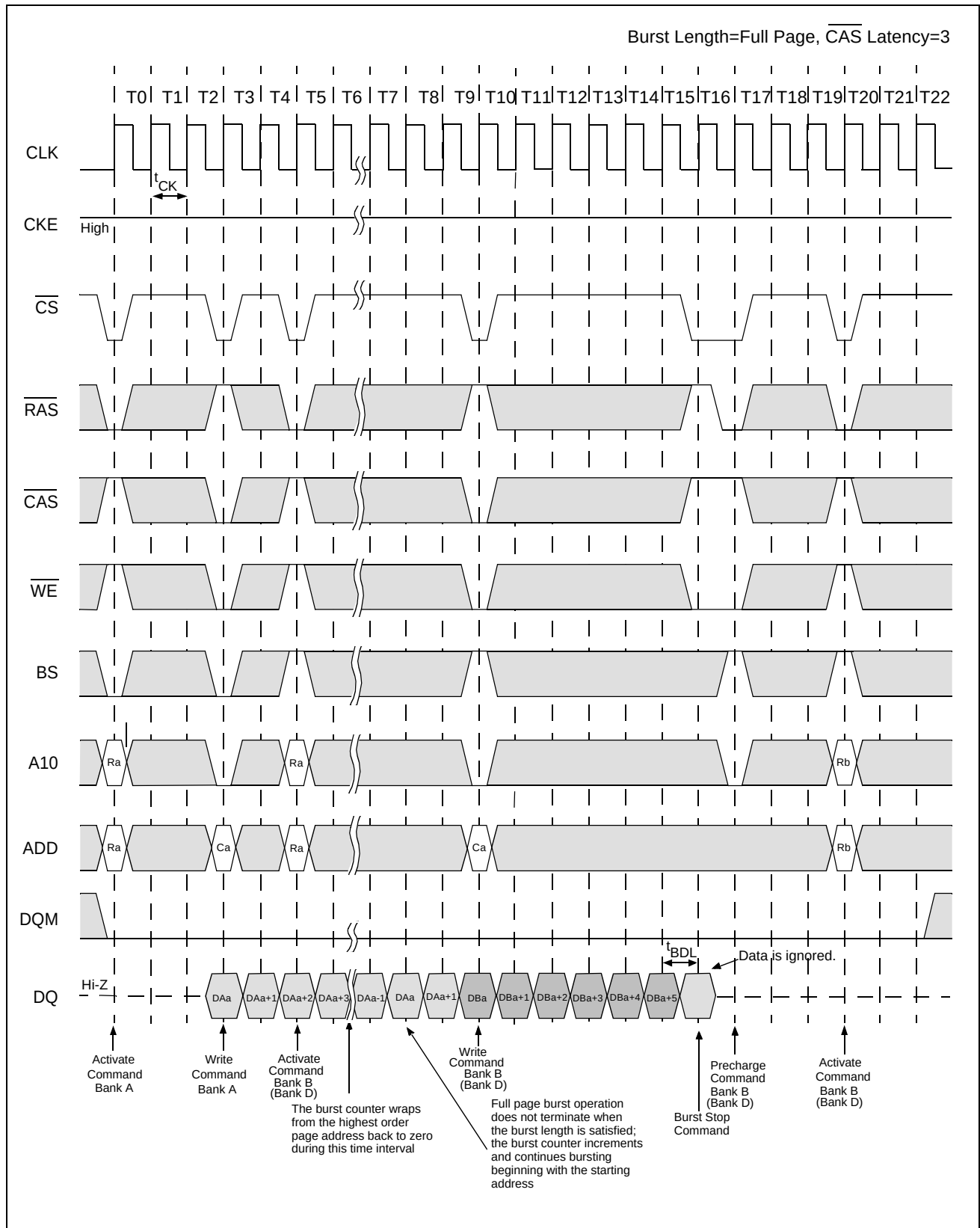
Full Page Read Cycle (2 of 2)



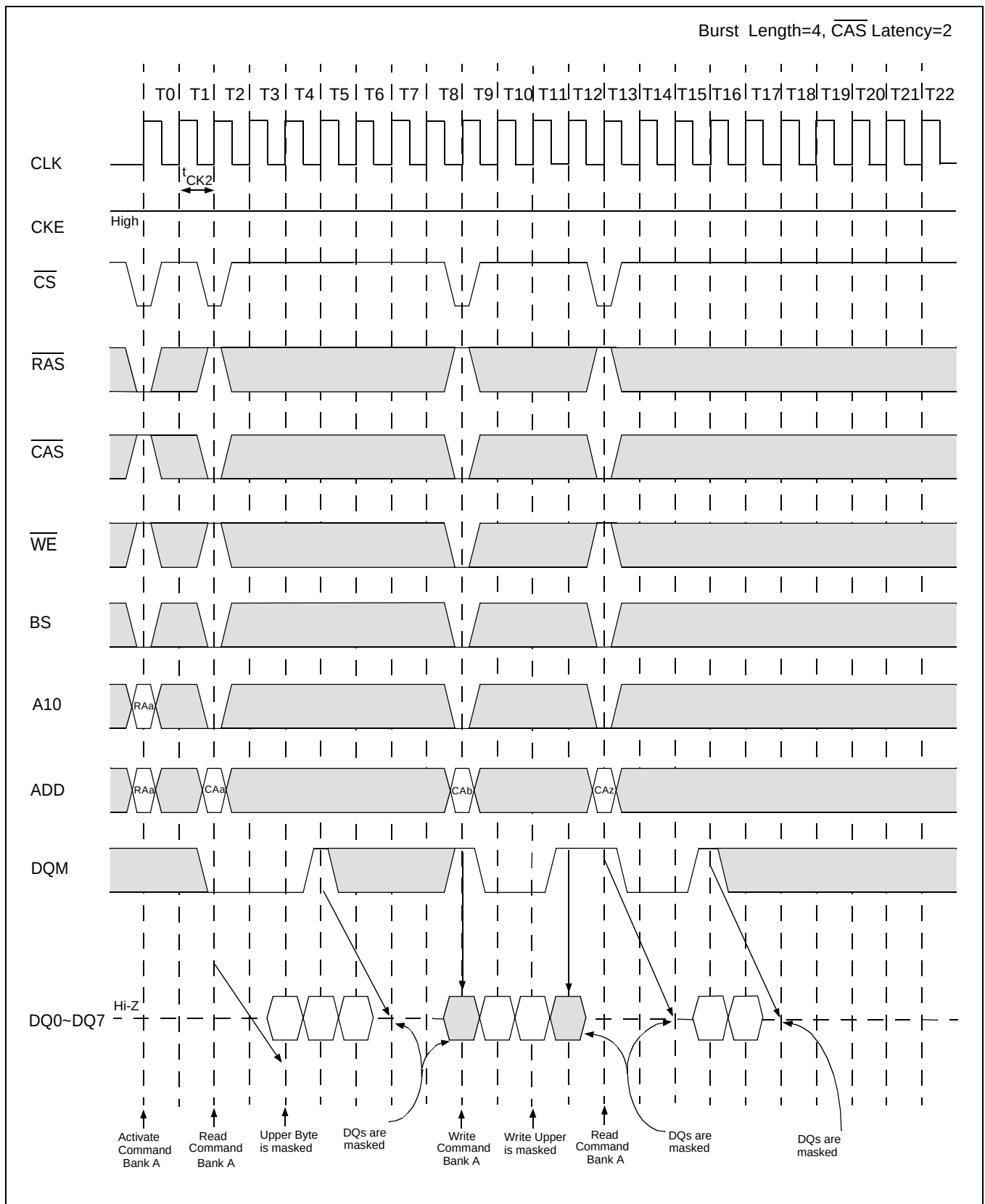
Full Page Write Cycle (1 of 2)



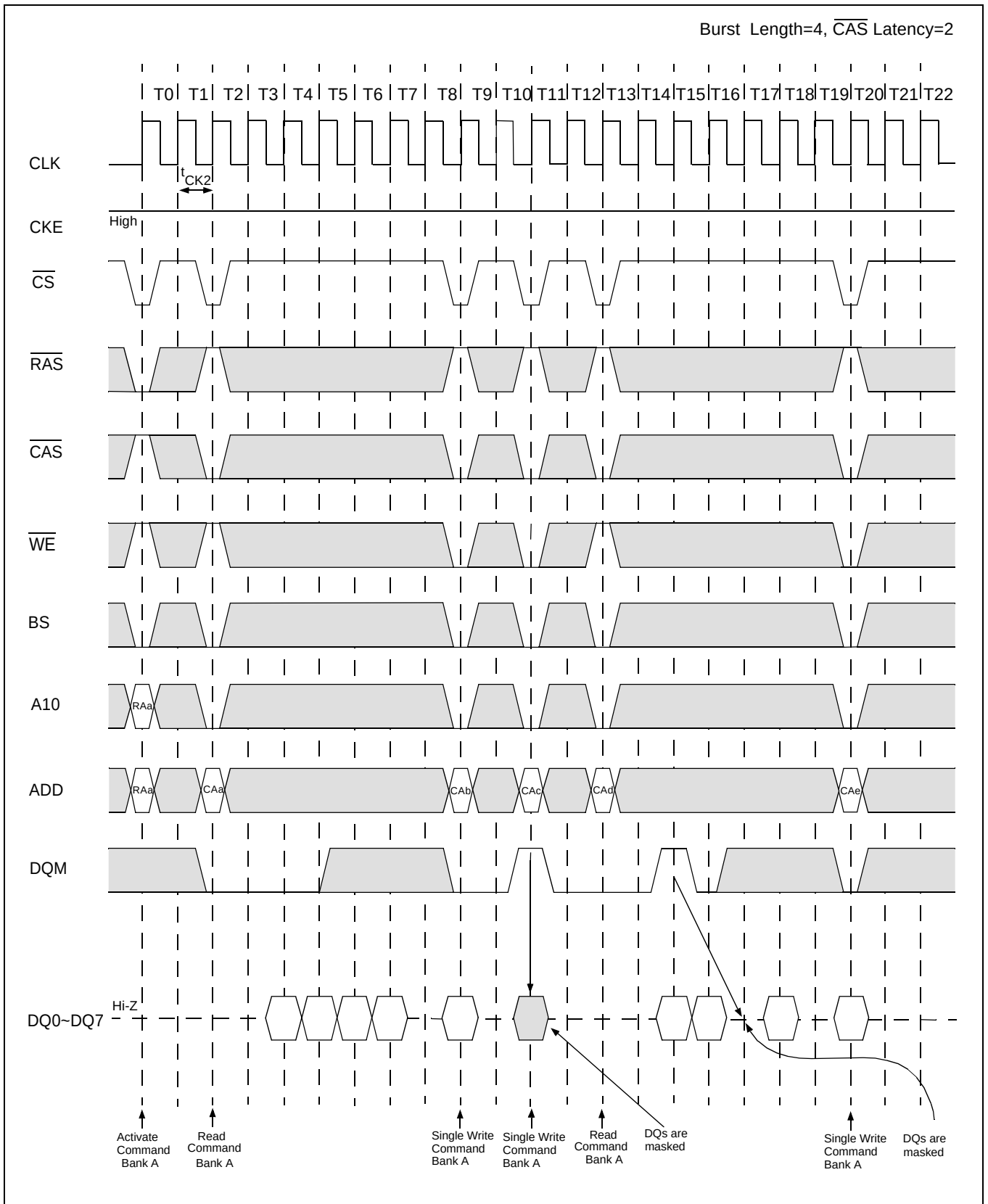
Full Page Write Cycle (2 of 2)



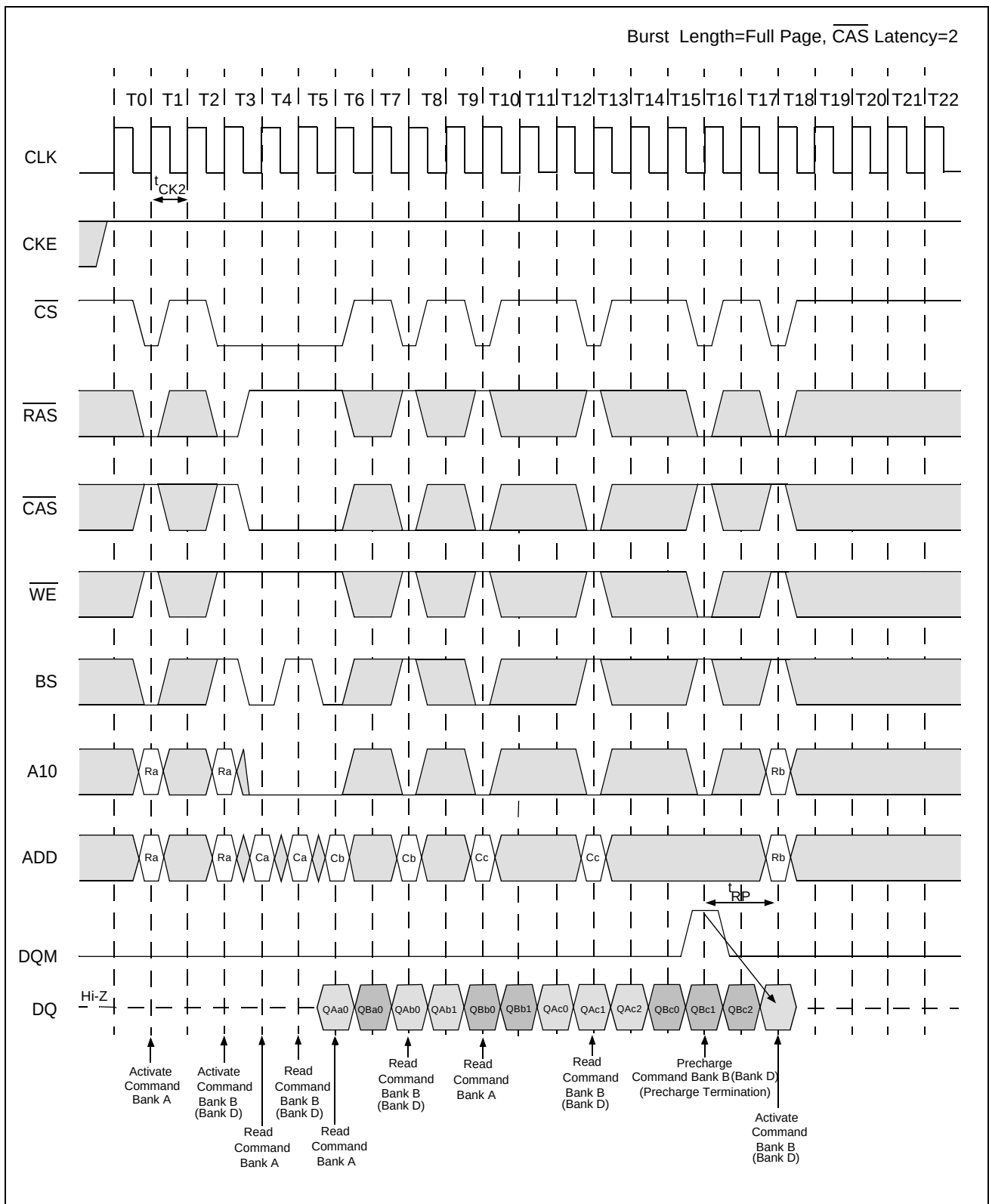
Byte Write Operation



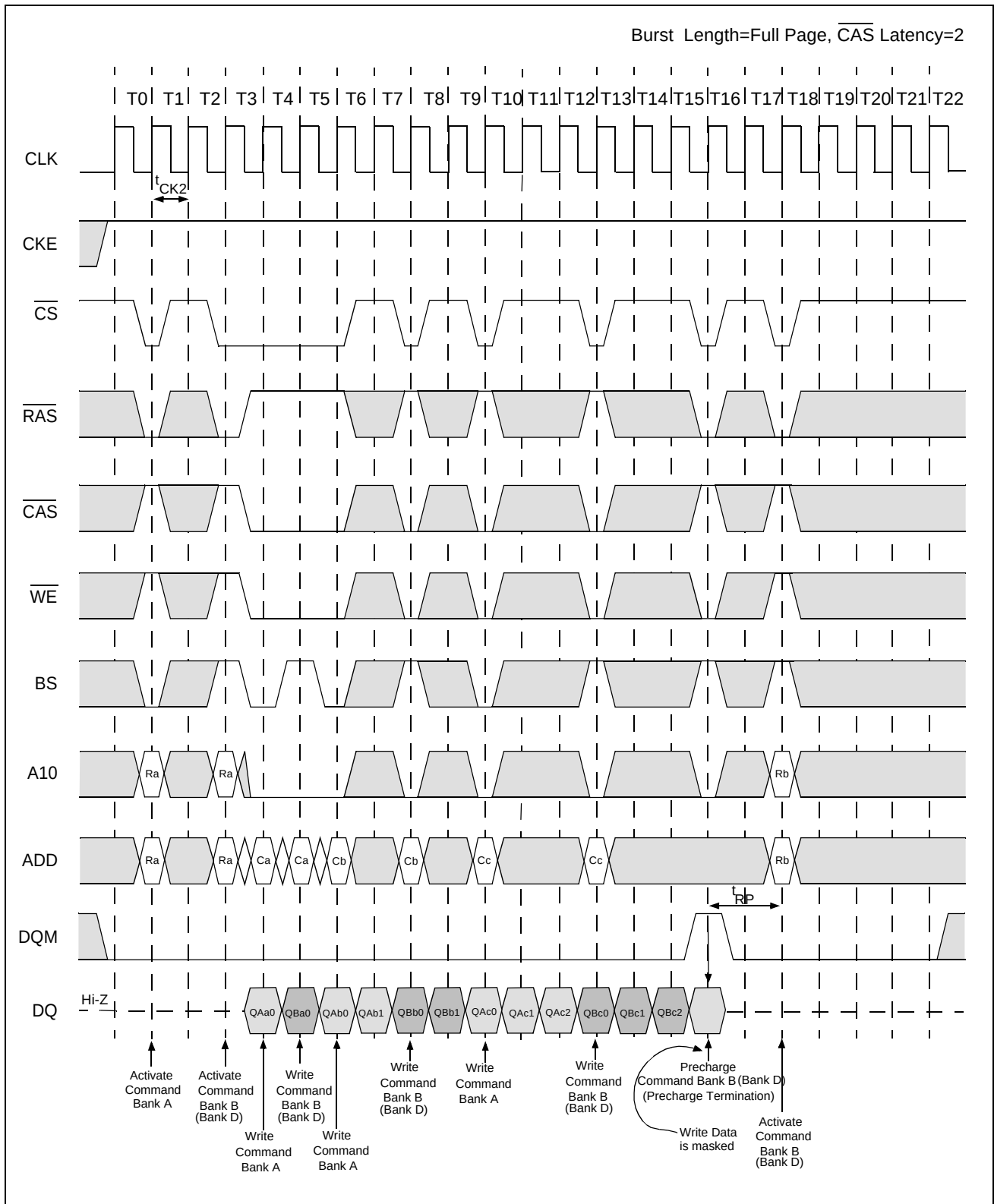
Burst Read and Single Write Operation



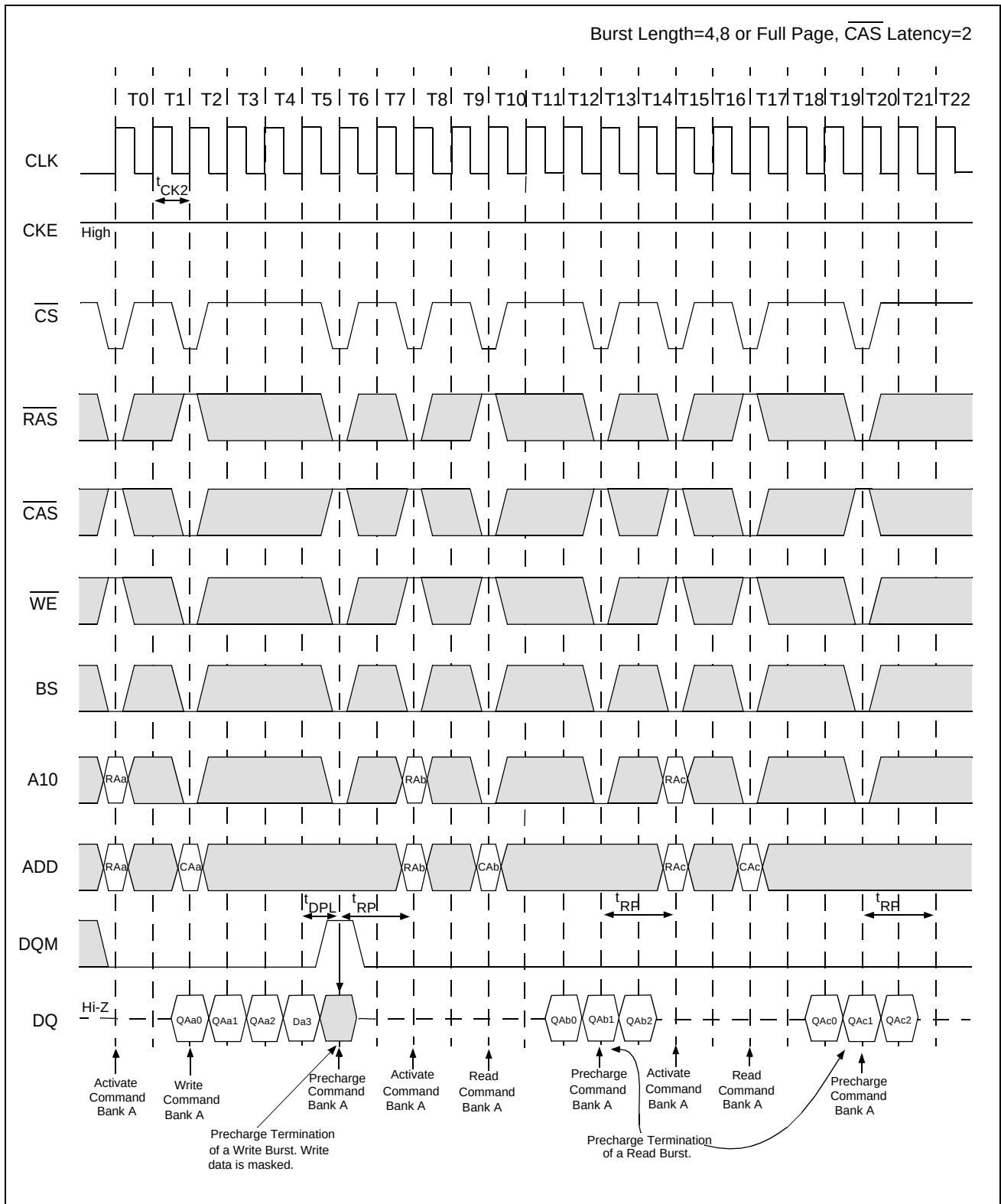
Full Page Random Column Read



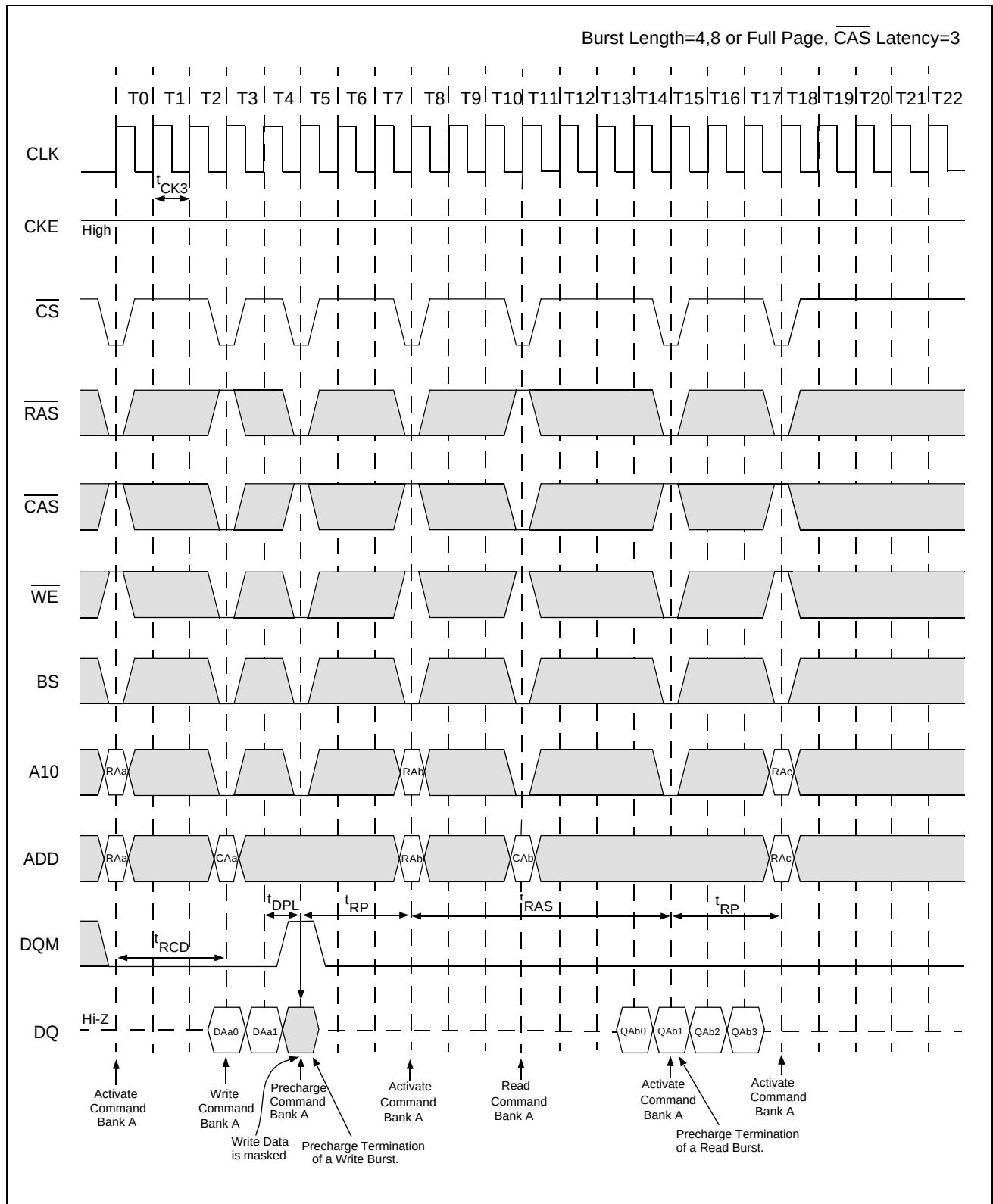
Full Page Random Column Write



Precharge Termination of a Burst (1 of 2)



Precharge Termination of a Burst (2 of 2)



Packaging Information

• 400mil, 86-Pin Plastic TSOPII

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	---	0.27	0.007	---	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.12	---	0.21	(0.005)	---	0.008
c1	0.12	0.125	0.16	(0.005)	0.005	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
e	0.50 BASIC			0.020 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	---	0.25	0.005	---	0.010
R1	0.12	---	---	0.005	---	---
ZD	0.61 REF.			0.024 REF.		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETERS

2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.

MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE.

DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.

INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.

ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.

DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.

