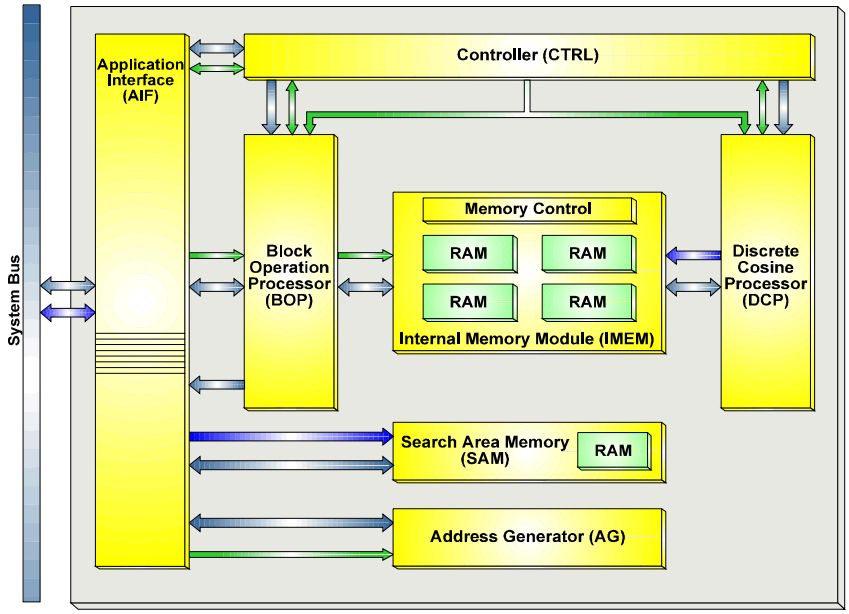
DesignObject™
Video Conferencing Hybrid Accelerator



Features

- Configurable Application Interface
- Top Level Controller Submodule
- Internal Memory Module
- Block Operation Processor
- Discrete Cosine Processor
- Address Generation
- Search Area Memory

Purpose of the Video Conferencing Accelerator

The Video Conferencing Hybrid Accelerator (VCHA) is a set of DesignObjects™ that is tailored to accelerate video processing in low-performance applications such as video conferencing or MPEG-1 Decoding. The VCHA is cascadable and performs MPEG-2 decoding either offline or in realtime with higher system frequency.

The VCHA provides basic operations on compressed and de-compressed video data. After these are programmed by the Digital Signal Processor (DSP), the VCHA directly processes the corresponding data blockwise out of the board memory, which relieves the DSP of computing-bound steps in the video decoding/ encoding process.

SICAN

SICAN GmbH

AIF - Application Interface

The AIF integrates Base Address Register, Control Register and the Status Register of the VCHA as well as the head and tail pointers of two command FIFOs. Because the AIF controls the address generation of the Address Generator (AG), all command block addresses are stored and managed by the AIF internally. Thus, virtual addressing of all other VCHA modules is achieved and the core of the VCHA is decoupled from the external memory. All data transfers to and from the external memory and the DSP command fetching are performed by the AIF using the a protocol defined by the DSP. Therefore, the AIF must be customized according to the chosen DSP.

CTRL - VCHA Top Level Controller

The CTRL module controls the general command scheduling and ensures the right order for the several command processing steps. In particular, the CTRL module synchronizes the data flow between all the VCHA modules using blockwise micro commands. This operation guarantees seemless cooperation between all modules during the motion vector search command execution.

IMEM - Internal memory Module

The Internal Memory IMEM is divided into two halves which are used to store the intermediate results of the BOP and DCP module. Both halves are exclusively accessed by the BOP and the DCP. There are 4 memory blocks in the IMEM module each with a size of 32 x 20 bit. The IMEM module is realized by a fast register file in order to maintain the high system frequency data rates of the VCHA processing units.

BOP - Block Operation Processor

The Block Operation Processor (BOP) performs the motion compensation with an optional pixel interpolation and a picture-to-picture interpolation. In addition, the BOP can accumulate the results from the motion compensation with IDCT-transformed coefficients which were previously calculated and stored into one IMEM half. All data transfers between the external board memory and the IMEM module are passed through the Block Operation Processor.

DCP - Discrete Cosine Processor

The Discrete Cosine Processor calculates the forward and inverse cosine transformation. The calculation is performed completely independently from other processing modules and is controlled only by the Top Level Controller CTRL. Input and output data for the DCP are transferred by the BOP via the IMEM module.

AG - Address Generation

The Address Generator calculates sequences of addresses to reference 32 bit memory words in the 22 bit external memory space. There are different modes for all necessary RAM accesses which are programmed at the beginning of the address generation cycle. During an address generation cycle, the AG calculates addresses as long as the AIF has external bus access. The AG can be stopped by the AIF temporarily, as long as the AIF is waiting for the memory bus.

SAM - Search Area Memory

The Search Area Memory is 1k byte of internal RAM, realized by two 128 x 32 bit RAMs, to hold a coherent part of the whole search area. The controlling of the SAM, including the address generation for read and write accesses, is performed by the AIF and partially by the BOP.

Gate Count and RAM Estimation

Modules	Gates	RAM
VCHA_CTRL	5.000	-
VCHA_IMEM	8.000	5.120 bit
VCHA_BOP	16.000	-
VCHA_DCP	14.000	-
VCHA_AG	3.000	-
VCHA_SAM	8.000	8.192 bit
VCHA_AIF	depending on the application	
	54.000	13.312 bit

sci-worx GmbH, Garbsener Landstr. 10, 30419 Hannover, Germany
Phone +49 511 277.1491, fax .2490, web www.sci-worx.com, email info@sci-worx.com

US Office : sci-worx Microelectronics Corp., 1032 Elwell Court, Suite 222, Palo Alto, CA 94303
Phone +1 650 625.1888, fax .1818, web www.sci-worx.com, email info@sci-worx.com

Technical data is subject to change without notice. All rights reserved. All trademarks are registered trademarks of their respective owner. Copyright © sci-worx GmbH.