3 DS-3 Framers with 84 T1 Framers

VSC9675

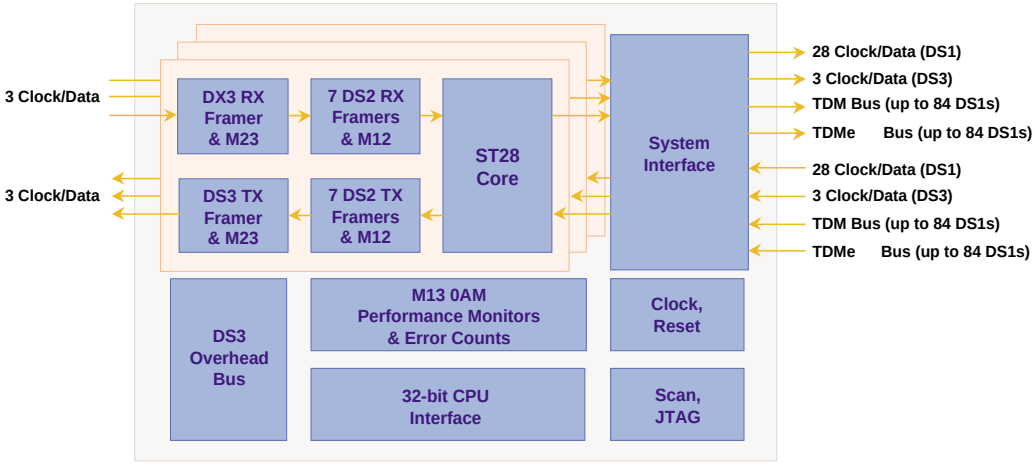
Product Brief

TimeStream Product Family

Features:

- Integrates up to 3 full featured DS3 framers and M13 multiplexers plus 84 DS1 framers in a single device
- Supported formats include M23 and C-bit for DS3, and SF and ESF for DS1
- 32-bit CPU interface supports leading embedded processors, including MPC860, StrongARM, and R3000
- DS3, DS2, DS1 and DS0 line loopback, and DS3 and DS1 local loopback
- Performance monitoring, MDL, far-end block error, and far-end alarm and control for each DS3 channel
- Performance monitoring, FDL, slip buffers, and robbed bit signaling for each DS1 channel
- DS3 framer only (for unchannelized DS3) and DS3 framer by-pass modes
- Receive and transmit DS1 jitter attenuation
- Encodes and decodes B3ZS line codes
- Detects Loss of Frame (LOF), Loss of Signal (LOS), Red, Yellow and AIS alarms
- Transmits Yellow and AIS alarms
- Programmable idle code substitution and data inversion
- Detect and transmit in-band loop-up and loop-down codes

VSC9675 Block Diagram



General Description

The VSC9675 belongs to Vitesse Semiconductors TimeStream™ product family, designed for high-density communication solutions. The VSC9675 is an 84-channel T1 framer with integrated M13 and provides up to 3 channels of T3 framing and multiplexing. It is designed for high channelization, high density points in the access and switching infrastructure such as access concentrators, routers and switches.

The VSC9675 is available with up to 3 DS3 framers with integrated M13 multiplexers/demultiplexers. It also includes 84 T1 framers and supports Operations and Mangement functionality.

This highly flexible device accepts 2-pin Clock/Data or 3-pin Clock/Pos/Neg from an LIU, or 3-pin Clock/Data/FP from an external DS3 Framer.

VITESSE SEMICONDUCTOR CORPORATION

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Features Continued:

- Three clocking modes for system-level flexibility; direct connection to 2/4/8 MHz TDM backplanes

Applications:

- ATM & Frame Relay Switches
- Remote Access Concentrators
- SONET/SDH Add-Drop Mux
- Digital Access Cross Connects
- Routers with T1 interfaces
- Carrier-class IP Telephony Switches

Standards:

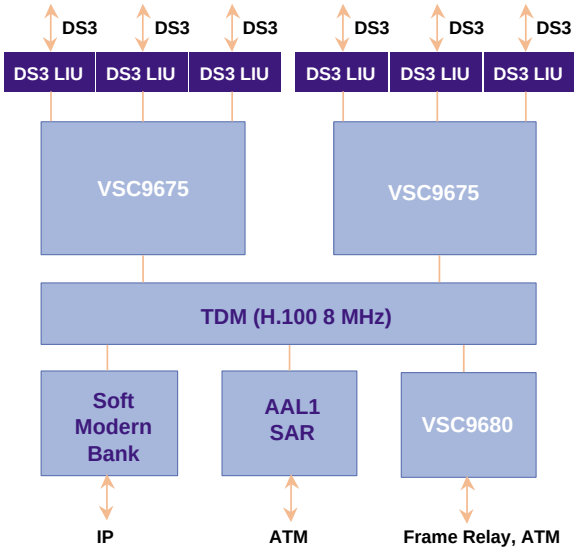
- AT&T Publications TR-62411 - Accunet T1.5 Service Description and Interface Specification 12/90
- AT&T Publication TR-54106 - Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super Frame, 9/89
- AT&T Publication TR-43801 – Channel Bank Requirements & Objectives, 9/82
- ANSI T1.403-1995, Network-to-customer Installation - DS1 Metallic Interface
- TR-303 Integrated Digital Loop Carrier System Generic Requirements 1995
- ANSI T1.107-1995, Digital Hierarchy-Formats Specification
- BELLCORE TR-TSY-000009, Asynchronous Digital Multiplexes Requirements and Objectives, 5/86

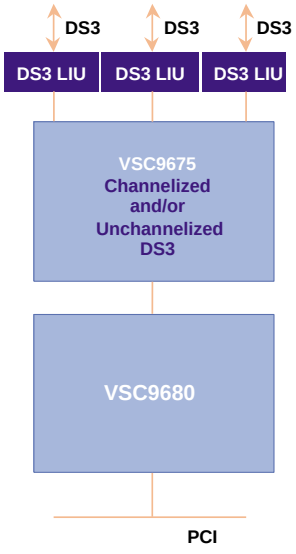
Unique Scalable Time-sliced Architecture

The VSC9675 uses a unique, patent pending, scalable time-sliced state machine architecture with internal context RAM to share logic for framing, error and performance monitoring, Facility Data Link (FDL) and Maintenance Data Link (MDL), robbed-bit signaling, slip buffers and other functions. The advantage of a shared state machine and shared RAM architecture is reduced gate count, resulting in a high density, low power design. Three methods for system-side connection to the VSC9675 are provided:

1) A standard Clk/Data for generic system connectivity, or
2) A high speed interface to a TDM backplane or standard time-slot-interchange, or
3) Vitesse open-architecture TDMe serial interface connecting the VSC9675 to the VSC9680.

Application Diagrams





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