Pointer Processor and Frame Aligner

VSC9184

Product Brief

TimeStream Product Family

Features & Benefits:

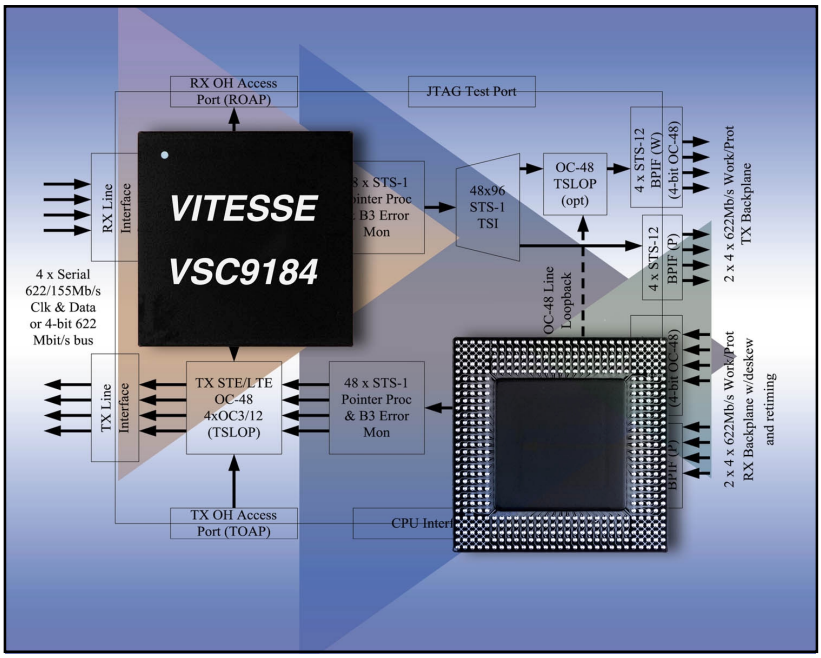
- Bi-directional STS-48/STM-16, Quad STS-12/STM-4, or Quad STS-3/STM-1 Section and Line Termination Device with Integrated Pointer Processing
- Optional STS-3|12/STM-1|4 to STS-48/STM-16 Combiner Mode for Terminal Multiplexer Applications
- Interfaces with other Vitesse Pointer Processor, TSI, and Backplane ICs

Line Interface

- Terminates and Generates SONET/SDH Section/Line Overhead
- Serial Ports allow SONET/SDH Transport Overhead Observation and Modification
- Designed to Work with VSC8115 155/622 Mhz CDR and VSC8144 2.5G Transceiver

2.5G Pointer Processor

- Performs B3 Path Error Monitoring for all STS-1 Tributaries
- Automatically Accommodates any Combination of STS-1, STS-3c, STS-12c, STS-48c Tributaries and SDH equivalents.
- Extensive Support for Loopback, Line and Source Timing Configurations.



Product Description

The VSC9184 is a bi-directional STS-48/STM-16, quad STS-12/STM-4 or quad STS-3/STM-1 Pointer Processor & Frame Aligner. Section and line termination is performed on line inputs and outputs in addition to partial path overhead monitoring. Pointer processing is performed to the STS-1/AU-3 level and automatically accommodates any valid combination of concatenated tributaries up to an STS-48c/AU-4-16c. Working and protection backplane interfaces are built onto the device with integrated retiming and deskew, allowing direct connection to other Timestream devices. This device can be used in SONET/SDH applications such as large TSI switches, digital cross-connects and add/drop as well as in DWDM terminal multiplexer applications.

VITESSE SEMICONDUCTOR CORPORATION

Pointer Processor and Frame Aligner

VSC9184

Product Brief

TimeStream Product Family

TSI Switch

- On Board 48x96 and 96x48 TSI with STS-1/AU-3 Granularity and Hitless Reconfiguration
- TSI Can Be Used as First and Third Layer of Large Switch Architecture for Collapsed Clos Configuration

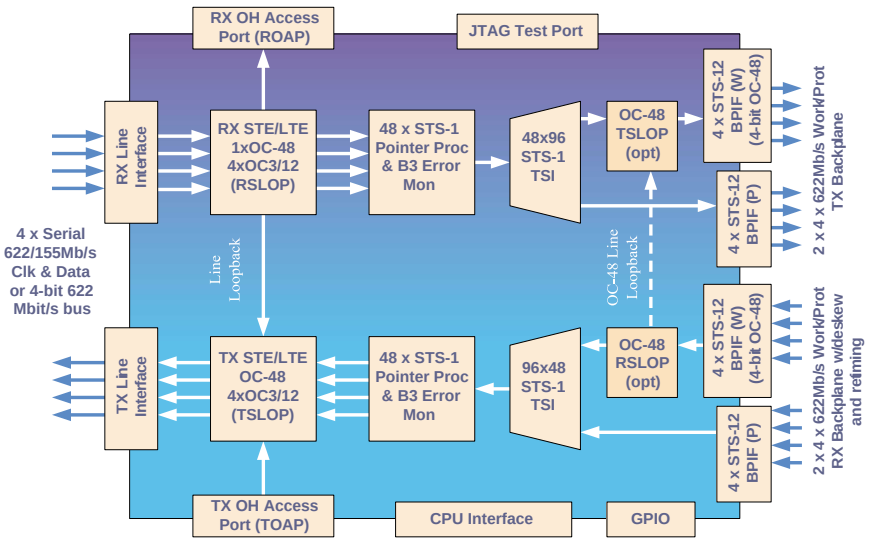
Integrated Backplane

- Uses Standard STS-12 Signaling on Backplane with B1 Byte for BER Monitoring
- Built in Retiming and Deskew of STS-12 Backplane Interface up to +/- 3 Bytes
- Working and Protection 4 x 622.08 Mb/s LVDS STS-12/STM-4 Back-plane Interface

Other

- IEEE 1149.1 JTAG Test Port
- Eight General Purpose I/O Ports
- Thermally Enhanced 474-pin CBGA Package
- 3.3V I/O and 2.5V Core Power Supplies

VSC9184 Block Diagram



VSC9184 Architectures

Two modes of operation are available: SONET/SDH line interface(s) to working and protection STS-12 backplane (ADM mode), or multiple OC-3/12 SONET/SDH line interface(s) to OC-48 line interface (Combiner mode).

ADM Mode: The VSC9184 can interface with one or multiple VSC9182 40G TSI Switch devices as a line interface solution for large SONET/SDH crossconnects, providing OC-48 client services or soft programmable quad OC-3/12 services. Both working and protection ports are provided for interfacing redundant switch fabrics, and the on board TSI can act as the first and third layer of a collapsed Clos architecture. The VSC9184 can also interface to other VSC9184 devices or the VSC9186 10G Pointer Processor and Frame Aligner for small ADM aggregation applications.

Combiner Mode: Four soft programmable OC-3/12 ports can be combined into an outgoing OC-48. Section and Line Termination, path B3 error monitoring and serial TOH access is supported on all five interfaces.

VITESSE
SEMICONDUCTOR CORPORATION
www.vitesse.com

For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com or contact Vitesse Sales at (800) VITESSE or sales@vitesse.com