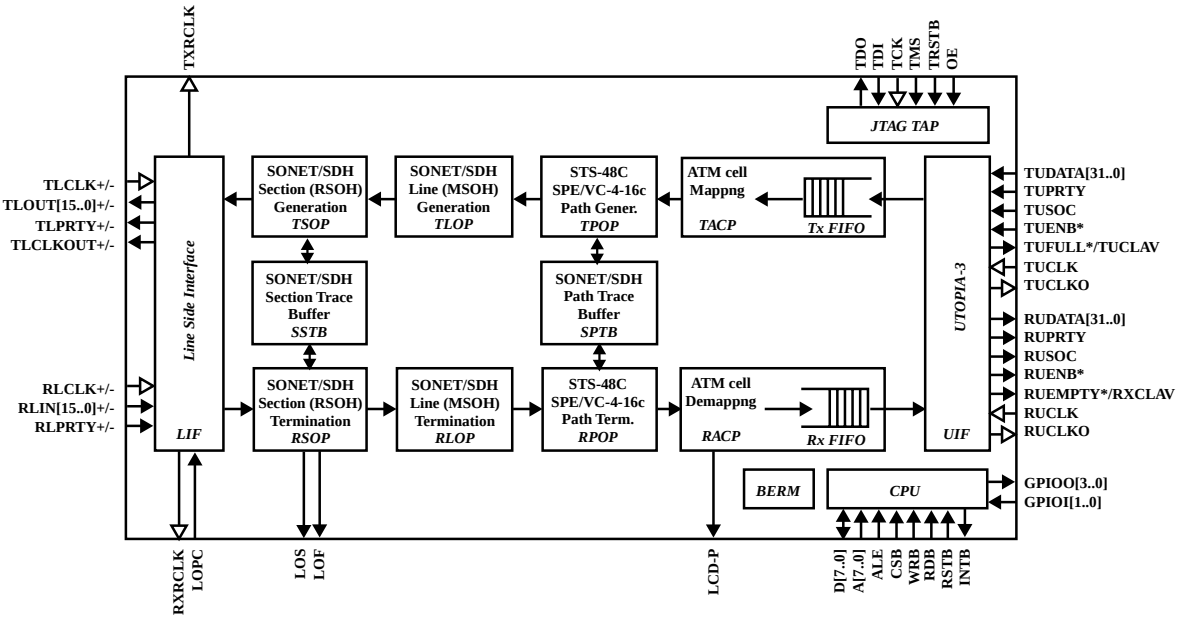
Data Sheet
VSC9110

STS-48 Physical Layer
ATM UNI/NNI Device

Features

- STS-48c ATM Framing Device for User Network Interface and Network Node Interface Applications
- STS-48c / STM-16c Support. Terminates and Generates SONET/SDH Section, Line, and Path Layers
- UTOPIA-3 Interface
- 16 bit PECL Interface to High-speed MUX/ DEMUX Transceivers
- Generic 8-bit Microprocessor Interface
- +3.3V Power Supply
- +5V Tolerant TTL I/O
- Compliant with SONET and SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 Documents
- 0.35 Micron CMOS Technology
- Thermally Enhanced 256 BGA Package
- Provides JTAG TAP Controller Conforming to the IEEE 1149.1 Standard

VSC9110 Block Diagram



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Functional Overview

The VSC9110 is a SONET/SDH to ATM framing device that can be used in equipment interconnecting ATM switches over public or private SONET/SDH networks. When used in conjunction with a high-speed mux/demux transceiver, the device provides a complete physical layer solution for ATM over SONET/SDH at the STS-48/STM-16 rate. By using this device, highly integrated OC-48 single line card solutions can be developed. The basic features of the receive and transmit datapaths along with features of other interfaces are listed below.

Line Interface (LIF)

- A parity bit, programmable for even/odd parity, is provided each for the incoming and outgoing datapaths.
- A reference clock output derived from the receive clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the receive clock.
- A reference clock output derived from the transmit clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the transmit clock.
- A Loss of Optical Carrier (LOPC) input signal is provided for monitoring and alarm purposes.

Receive Section Overhead Processor (RSOP)

- 12/24/48-bit A1/A2 framing patterns are supported.
- Out Of Frame (OOF) and Loss Of Frame (LOF) alarm condition are detected.
- The incoming data stream is optionally descrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.
- Section BIP-8 (B1) errors are detected and accumulated. Both individual and block mode accumulation of B1 error indications are supported.
- The incoming data stream, before descrambling, is monitored for absence of transitions or “all-zero patterns”. The Loss Of Signal (LOS) detection and termination criterias are programmable.
- It is possible to force insertion of all “1” in the data stream, except for the Section overhead. The Line AIS (AIS-L) condition may be automatically inserted in case of LOS, LOF, or Loss of Optical Carrier (LOPC) alarm events.

Receive Line Overhead Processor (RLOP)

- The Line Remote Defect Indication (RDI-L) and Line Alarm Indication Signal (AIS-L) alarms carried in the K2 byte are extracted and filtered. The filter constants are programmable.
- Line BIP-384 errors carried in the B2 bytes are detected and accumulated. Both individual and block mode accumulation of B2 errors are supported.
- Line REI error indications carried in the M1 byte are accumulated. Both individual and block mode accumulation of M1 error indications are supported.
- The Synchronization Status carried in the S1 byte is extracted and filtered. Unstable and mismatch alarms are supported. The filter constants are programmable.

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- The Automatic Protection Switching (APS) bytes, K1 and K2, are extracted and filtered. Unstable alarm is supported. The filter constants are programmable.

Receive Path Overhead Processor (RPOP)

- The H1 and H2 pointer bytes are detected and interpreted according to ANSI T1.105 and ITU-T G.707. The mechanism is programmable to support both SONET and SDH. Path Alarm Indication Signal (AIS-P) and Loss of Pointer (LOP-P) alarm declarations are provided. Several pointer functions are also provided for diagnostic purposes.
- The H1 and H2 pointer bytes are monitored for Concatenation Indication (CI). Loss of Pointer (LOPX) and AIS (AISX) alarm declarations are provided.
- Path BIP-8 errors carried in the B3 byte are detected and accumulated. Both individual and block mode accumulation of B3 errors are supported.
- Path REI error indications carried in the G1 byte are detected and accumulated. Up to 64000 individual errors can be detected per second. Both individual and block mode accumulation of Path REI error indications are supported.
- The Path RDI carried in the G1 byte is detected and programmable.
- The Signal Label carried in the C2 byte is detected, alarmed and is programmable.

Receive ATM Cell Processor (RACP)

- Cell Delineation is provided using shortened cyclic code with a generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^8$ can be added to the calculated HEC check bits before comparison.
- Single-bit header error correction is supported. The dropping of cells during single or multiple error detection is programmable.
- The 48 byte information field is descrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Descrambling can be enabled/disabled.
- Cells can be filtered based on a programmable cell header pattern in the GFC, PTI, or CLP fields.
- The number of correctable and uncorrectable HEC errors detected, and the number of cells written to the Rx FIFO are monitored.
- The Rx FIFO can accommodate storage of eight ATM cells.

Drop Side Interface (ATM UTOPIA Interface)

- A parity bit, programmable for even/odd parity, is provided for each transmit and receive datapaths.
- It is possible to force reset/flush the contents in the Tx FIFO via the CPU interface.
- It is possible to force reset/flush the contents in the Rx FIFO via the CPU interface.
- The Drop Side Interface provides a Single-PHY UTOPIA-3 interface for ATM operations.
- Two formats of the ATM cells are supported: 52 byte cell or 56 byte cell containing the HEC.
- The UTOPIA-3 interface supports both word-level and cell-level flow control.

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Transmit ATM Cell Processor (TACP)

- The ATM cells are mapped into the STS-48c SPE or equivalent SDH VC-16-16c. Programmable idle/ unassigned cells are inserted into the cell stream.
- The 48 byte information field is scrambled with a self-synchronizing descrambler polynomial $1 + x^{43}$. Scrambling can be enabled/disabled.
- The HEC generator performs a CRC-8 calculation over the first four header octets using the generating polynomial $1 + x + x^2 + x^8$. The coset polynomial $1 + x^2 + x^4 + x^6$ can be added to the result. The HEC is optionally inserted into the fifth octet of the header of cells read from the Tx FIFO.
- The Tx FIFO can accomodate storage of eight ATM cells.

Transmit Path Overhead Processor (TPOP)

- The H1 and H2 pointer byte values are programmable to support both SONET and SDH. Several pointer functions are provided for diagnostics purposes. The remaining 47 H1 and H2 bytes are programmable.
- The Path BIP-8 is computed and placed in the B3 byte of the current frame. It is possible to insert B3 errors for diagnostic purposes.
- The number of Path BIP-8 errors detected in the Receive Path Overhead Processor (RPOP) is backreported as Path REI in the G1 byte. Both individual and block mode backreporting for G1 are supported.
- It is possible to enable/disable RDI-P insertion for each of the following alarms: LOS, LOF, AIS-L, AIS-P, LOP-P, TIM-P, UNEQ-P, LCD-P and PLM-P. Both the latest and earlier definitions of RDI-P are supported.
- The Path Signal Label (C2) byte value is programmable.
- The Path Trace (J1) byte value is programmable.
- The F2, H4, Z3, Z4, and Z5 bytes are programmable.

Transmit Line Overhead Processor (TLOP)

- It is possible to insert programmable sets of K1 and K2 bytes into the outgoing data stream.
- RDI-L can be automatically inserted during the detection of an LOS, LOF, or AIS-L alarm in the receive data stream.
- The Line BIP-384 code is computed and placed in the B2 bytes of the current frame. It is possible to insert B2 errors for diagnostics purposes.
- The number of Line BIP-384 errors detected in the Receive Line Overhead Processor (RLOP) is backreported as Line REI in the M1 byte. Up to 255 errors can be backreported per frame in individual mode. Both individual and block mode backreporting for M1 are supported. It is possible to insert M1 error indications for diagnostics purposes.
- The Synchronization Status value inserted in the S1 byte is programmable.
- All bytes in the line overhead that are reserved for national or future international standardization use can be overwritten with 0x00.

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• The H1, H2, and H3 bytes from the Transmit Overhead Access Port (TOAP) can be inserted into the H1, H2, and H3 overhead bytes, or applied as an error mask to the H1, H2, and H3 overhead bytes.

Transmit Section Overhead Processor (TSOP)

• It is possible to forced insert all "1"s into the data stream, before scrambling, with the exception of the section overhead. The AIS-L condition can be automatically inserted through activity from the special purpose serial interfaces.

• The Section BIP-8 code is computed and can be placed in the B1 byte of the current frame. It is possible to insert B1 errors for diagnostics purposes.

• The A1 and A2 framing bytes can be inserted into the frame. It is also possible to introduce bit errors in the framing word.

• The J0 byte supports both SONET and SDH formats. The J0 byte can be programmed to a fixed value for interworking with older equipment implementing the C1 indentification byte.

• The Z0 growth bytes supports both SONET and SDH formats. The Z0 bytes can be programmed to carry the C1 identification bytes for interworking with older equipment.

• The outgoing data stream is optionally scrambled using the generating polynomial $1 + x^6 + x^7$ with a sequence length of 127.

• It is possible to force insert all “0”s in the outgoing data stream after scrambling for diagnostic purposes (LOS).

• All bytes in the section overhead that are reserved for national or future international standardization use can be overwritten with 0x00.

SONET/SDH Section Trace Buffers (SSTB)

• Three different Section Trace Message (J0) formats are supported in both transmit and receive directions: one byte (SONET) message, 16 byte (SDH) message, and 64 byte (SONET CLLI) message.

• The received section trace message is checked for persistency. A mismatch alarm is supported.

CPU Interface

• All configuration bits are both writeable and readable and can be accessed regardless of the device clock source status, except for the reset state. Configuration bits include selection bits, interrupt masking bits, and programmable counter/control values.

• Eight programmable General Purpose Input/Output (GPIO) ports are available for monitoring and controlling external signals. All GPIOs support bistable interrupts when configured as input ports.

• Clock activity monitors are implemented for all input clocks.

Bit Error Rate Monitoring

• Bit error rate monitoring is based on the Line BIP (B2) error code and is capable of measuring BERs down to 10^{-10} .

• Two bit error rate thresholds are implemented on the device.

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JTAG

- Standard IEEE 1149.1 compliant JTAG interface.

Loopback Modes

- Equipment loopback is supported by looping the output from the Transmit Section Overhead Processor (TSOP), in the transmit direction, back to the input of the Receive Section Overhead Processor (RSOP), in the receive direction.
- Facility loopback is supported by looping the data received on the receive Line Side Interface back to the transmit Line Side Interface.
- Utopia loopback is supported by looping the output from the Tx FIFO to the input of the Rx FIFO.

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AC Characteristics

Figure 1: Rx Line Interface Timing Dependencies

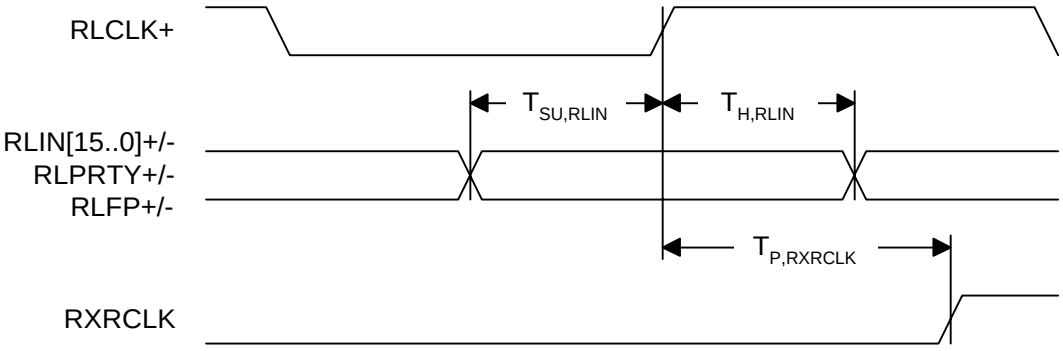

Table 1: Rx Line Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{RLCLK}	RLCLK+/- Clock Frequency (nominal)	-	155.52	MHz
dc_{RLCLK}	RLCLK+/- Duty Cycle	40	60	%
$T_{R/F, RLCLK}$	RLCLK+/- Rise/Fall Time	-	1.0	ns
$T_{SU, RLIN}$	RLIN[15..0]+/-, RLPRTY+/-, RLFP+/- Setup Time to RLCLK+ Rising Edge	1.5	-	ns
$T_{H, RLIN}$	RLIN[15..0]+/-, RLPRTY+/-, RLFP+/- Hold Time to RLCLK+ Rising Edge	1.0	-	ns
$T_{P, RXRCLK}$	RLCLK+ Rising Edge to RXRCLK Rising/Falling Edge	1.0	20.0	ns
f_{RXRCLK}	f_{RLCLK} Divided by 2/4/8/19440	-	-	MHz
dc_{RXRCLK}	RXRCLK Duty Cycle	30	70	%
RXRCLK times are for 50 pF load.				

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Figure 2: Tx Line Interface Timing Dependencies

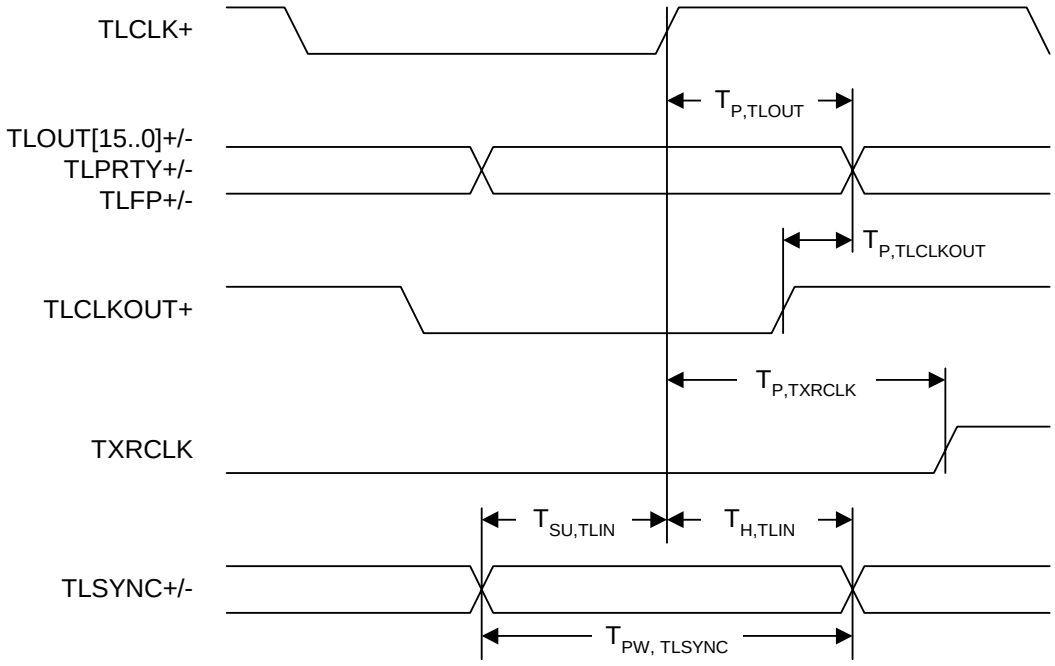

Table 2: Tx Line Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TLCLK}	TLCLK+/- Clock Frequency (nominal)	-	155.52	MHz
dc_{TLCLK}	TLCLK+/- Duty Cycle	40	60	%
$T_{R/F,\ TLCLK}$	TLCLK+/- Rise/Fall Time	-	1.0	ns
$T_{P,\ TLOUT}$	TLCLK+ Rising Edge to TLOUT[15..0]+/- and TLPRTY+/-, TLFP+/- Valid	1.0	4.0	ns
$T_{P,\ TXRCLK}$	TLCLK+ Rising Edge to TXRCLK Rising/Falling Edge	1.0	20.0	ns
$T_{P,\ CLKOUT}$	TLCLKOUT+ Rising Edge to TLOUT[15..0]+/-, TLPRTY+/-, TLFP+/- Valid	0	1.3	ns
f_{TXRCLK}	f_{TLCLK} Divided by 2/4/8/19440	-	-	MHz
dc_{TXRCLK}	TXRCLK Duty Cycle	30	70	%
$T_{SU,\ TLIN}$	TLSYNC +/- Setup Time to TLCLK+ Rising Edge [1)]	2.0		ns
$T_{H,\ TLIN}$	TLSYNC +/- Hold Time to TLCLK+ Rising Edge [1)]	1.0		ns
$T_{PW,\ TLSYNC}$	Minimum Pulse Width of TLSYNC (measured in TLCLK Clock Cycles)	2		-

[1)] It is not required that $T_{SU,\ TLIN}$ and $T_{H,\ TLIN}$ are met.
TXRCLK times are for 50 pF load.
TLOUT[15..0], TLFP, TLPRTY and TLCLKOUT are for 0.5 pF load. Add 0.3 ns for each pF of extra load.

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Figure 3: Rx UTOPIA Interface Timing Dependencies

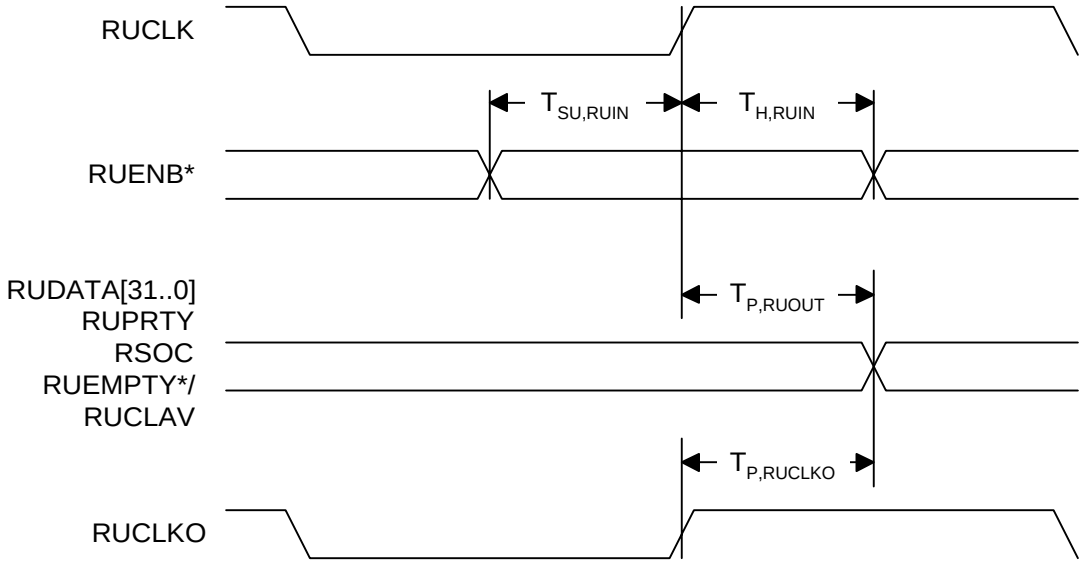

Table 3: Rx UTOPIA Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{RUCLK}	RUCLK clock frequency (nominal)	50	104	MHz
dc_{RUCLK}	RUCLK duty cycle	40	60	%
$T_{R/F, RUCLK}$	RUCLK rise/fall time	-	2.0	ns
$T_{SU, RUIN}$	RUENB* setup time to RUCLK rising edge	2.0	-	ns
$T_{H, RUIN}$	RUENB* hold time to RUCLK rising edge	0.5	-	ns
$T_{P, RUOUT}$	RUCLK rising edge to RUDATA[31..0], RUPRTY, RUSOC, RUEMPTY*/RUCLAV valid	1.0	6.0	ns
$T_{P, RUCLKO}$	RUCLKO rising edge to RUDATA[31..0], RUPRTY, RUSOC and RUEMPTY*/RUCLAV valid.	0.0	1.5	ns
Output times are for 25 pF load.				

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Figure 4: Tx UTOPIA Interface Timing Dependencies

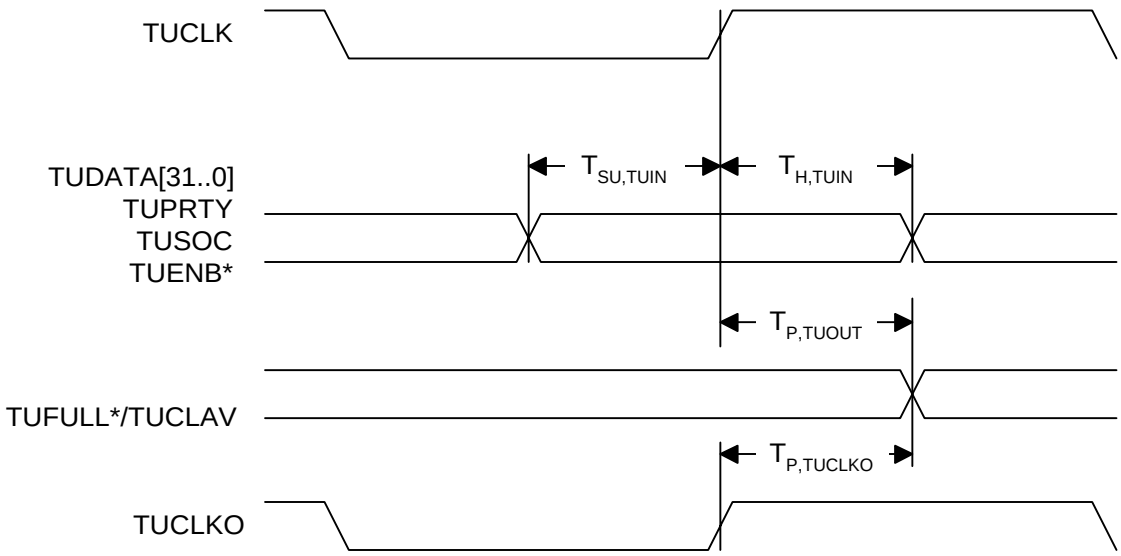

Table 4: Tx UTOPIA Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TUCLK}	TUCLK clock frequency (nominal)	50	104	MHz
dc_{TUCLK}	TUCLK duty cycle	40	60	%
$T_{R/F, TUCLK}$	TUCLK rise/fall time	-	2.0	ns
$T_{SU, TUIN}$	TUDATA[31..0], TUPRTY, TUSOC and TUENB* setup time to TUCLK rising edge	2.0	-	ns
$T_{H, TUIN}$	TUDATA[15..0], TUPRTY, TUSOC and TUENB* hold time to TUCLK rising edge	0.5	-	ns
$T_{D, TUOUT}$	TUCLK rising edge to TUFULL*/TUCLAV valid	1.0	6.0	ns
$T_{P, TUCLKO}$	TUCLKO rising edge to TUFULL*/TUCLAV valid.	0.0	1.5	ns
Outputs are for 25 pF load.				

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Figure 5: JTAG Interface Timing Dependencies

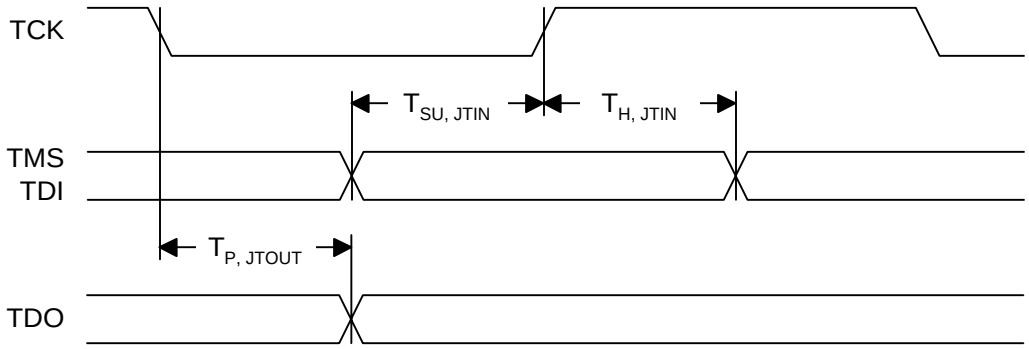

Table 5: JTAG Interface

Symbol	*Description*	*Min*	*Max*	*Unit*
f_{TCK}	TCK Frequency	-	1	MHz
dc_{TCK}	TCK Duty Cycle	40	60	%
$T_{SU, JTIN}$	TMS/TDI Setup Time to TCK Rising Edge	50	-	ns
$T_{H, JTIN}$	TMS/TDI Hold Time to TCK Rising Edge	50	-	ns
$T_{P, JOUT}$	TCK Falling Edge to TDO Valid	1.5	50	ns

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Figure 6: CPU Read Access Timing Dependencies

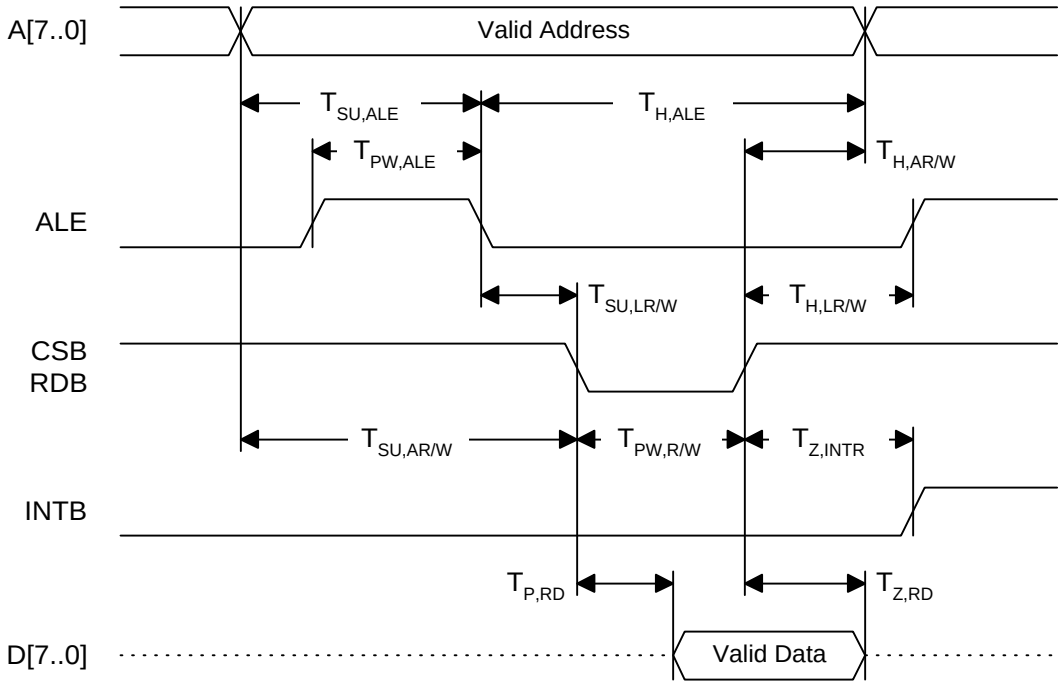

Figure 7: CPU Write Access Timing Dependencies

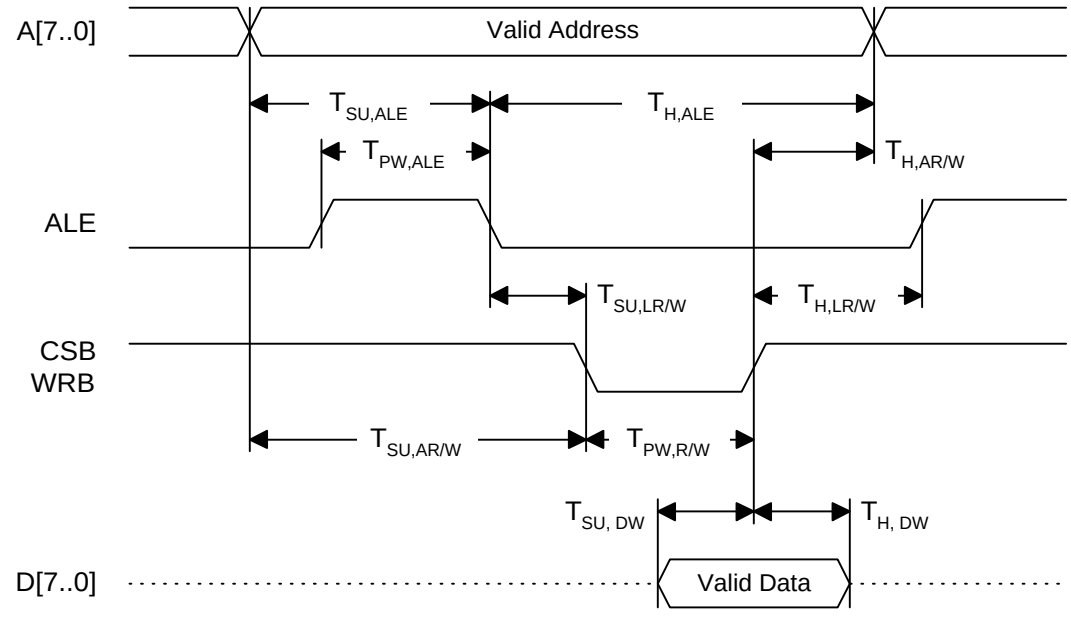

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Table 6: CPU Read/Write Access

Symbol	*Description*	*Min*	*Max*	*Unit*
$T_{SU, ALE}$	Address to Address Latch Setup Time	10	-	ns
$T_{H, ALE}$	Address to Address Latch Hold Time	10	-	ns
$T_{PW, ALE}$	Address Latch Pulse Width	20	-	ns
$T_{SU, LR/W}$	Latch to Valid Read/Write Setup Time	0	-	ns
$T_{H, LR/W}$	Latch to Valid Read/Write Hold Time	5	-	ns
$T_{SU, AR/W}$	Address to Valid Read/Write Setup Time	10	-	ns
$T_{H, AR/W}$	Address to Valid Read/Write Hold Time	10	-	ns
$T_{PW, R/W}$	Valid Read/Write Pulse Width	20	-	ns
$T_{SU, DW}$	Data to Valid Write Setup Time	20	-	ns
$T_{H, DW}$	Data to Valid Write Hold Time	10	-	ns
$T_{P, RD}$	Valid Read to Valid Data Propagation Delay		80	ns
$T_{Z, RD}$	Valid Read Negated to Output Tristate	1	25	ns
$T_{Z, INTH}$	Valid Read Negated to Interrupt Release/Pull-down		100	ns
All output times are for 100 pF load.				

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DC Characteristics

Parameters	Description	Min	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	V	I_{OH} = -2,-4,-12,-16 mA
V_{OL}	Output LOW voltage (TTL)	—	0.5	V	I_{OL} = 2,4,12,16 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	0.8	V	—
I_{IT}	Input current (TTL)	—	10	µA	0V< V_{IN} < 5V
V_{OD50}	Differential output swing (PECL)	0.800	1.200	V	50¾ to V_{DD} - 2.0V
V_{OH50}	Output HIGH voltage (PECL)	V_{DD} - 1.050	V_{DD} - 0.750	V	50¾ to V_{DD} - 2.0V
V_{OL50}	Output LOW voltage (PECL)	V_{DD} - 1.950	V_{DD} - 1.850	V	50¾ to V_{DD} - 2.0V
V_{OD75}	Differential output swing (PECL)	1.050	1.450	V	75¾ to V_{DD} - 2.0V
V_{OH75}	Output HIGH voltage (PECL)	V_{DD} - 0.850	V_{DD} - 0.550	V	75¾ to V_{DD} - 2.0V
V_{OL75}	Output LOW voltage (PECL)	V_{DD} - 2.0000	V_{DD} - 1.900	V	75¾ to V_{DD} - 2.0V
V_{ID}	Required diff. input voltage (PECL)	0.300	—	V	—
V_{IH}	Input HIGH voltage (PECL)	V_{DD} - 1.32	V_{DD}	V	—
V_{IL}	Input LOW voltage (PECL)	0.0	V_{IH} - 0.300	V	—
I_{IP}	Input current (PECL)	-1000	1000	µA	0V <V_{IN} <3.3V

NOTE: Negative current flow into the device (sinking), positive currents flow out of the device (sourcing)

Power Dissipation

Parameter	*Description*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	830	mA
P_D	Power dissipation	2.5	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND .....-0.5V to +4V
Power Supply Voltage (V_{DD5}) Potential to GND.....-0.5V to +6V
DC Input Voltage (PECL inputs)..... -0.5V to V_{DD} + 0.5V
DC Input Voltage (TTL inputs) .....-0.5V to V_{DD5} + 0.5V
DC Output Voltage (TTL Outputs)..... -0.5V to V_{DD} + 0.5V
DC Output Voltage (TTL 5V Tolerant Outputs) .....-0.5V to V_{DD5} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs).....+/-50mA
Case Temperature Under Bias .....-55^{o} to +125^{o}C
Storage Temperature.....-65^{o}C to +150^{o}C
Maximum Input ESD (Human Body Model)..... 2000 V

Note: Caution: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) .....+3.3V ±10%
Power Supply Voltage (V_{DD5})..... +5.0V ±10%
Operating Temperature Range* (T)..... -40^{o} to 85^{o}C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

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Package Pin Description

Pin	*Name*	*I/O*	*Type*	*Description*
RLIN[15:0]+/ RLIN[15:0]-	Parallel Line Receive Data.	I	PECL	This parallel data bus carries the incoming STS-48c/ STM-4-16c data stream. RLIN[15] is the most significant bit and RLIN[0] is the least significant bit. RLIN[15] is the first arriving bit on the serial data stream. RLIN[15:0] is sampled on the rising edge of RLCLK+.
RLCLK+/ RLCLK-	Parallel Line Receive Clock.	I	PECL	The clock reference for the 2.5Gb/s receive flow carried in RLIN[15:0]. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
RLPRTY+/ RLPRTY-	Parallel Line Receive Parity.	I	PECL	This input carries the even/odd parity over the parallel data input (RLIN[15:0]+). RLPRTY is sampled on the rising edge of RLCLK+.
TLOUT[15:0]+ /TLOUT[15:0]-	Parallel Line Transmit Data.	O	PECL	This parallel data bus carries the outgoing STS-48c/ STM-4-16c data stream. TLOUT[15] is the most significant bit and TLOUT[0] is the least significant bit. TLOUT[15] is the first transmitted bit on the serial data stream. TLOUT[15:0] is generated on the rising edge of the incoming TLCLK+.
TLCLK+/ TLCLK-	Parallel Line Transmit Clock.	I	PECL	The clock reference for the 2.5Gb/s transmit flow carried in TLOUT[15:0]. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
TLCLKOUT+/ TLCLKOUT-	Looped Parallel Line Transmit Clock.	O	PECL	This signal is the looped TLCLK signal. The timing for the clock is defined with reference to the TLOUT data bus signals. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
TLPRTY+/ TLPRTY-	Parallel Line Transmit Parity.	O	PECL	This signal carries the even/odd parity over the parallel data output (TLOUT[15:0]+). TLPRTY is generated on the rising edge of TLCLK+.
RXRCLK	Receive Reference Clock.	O	TTL	This output is a reference clock derived directly from RLCLK in a 78MHz/38MHz/19MHz/8kHz version
TXRCLK	Transmit Reference Clock.	O	TTL	This output is a reference clock derived directly from TLCLK in a 78MHz/38MHz/19MHz/8kHz version
RUDATA[31:0]	Receive UTOPIA data.	O	TTL	Four-octet wide data driven from PHY to ATM layer. RUDATA[31] is the MSB.
RUPRTY	Receive UTOPIA parity.	O	TTL	RUPRTY is the odd/even (programmable, default odd) parity for RUDATA[31:0]. To support multiple PHY configurations.
RUSOC	Receive UTOPIA Start Of Cell.	O	3TTL	Active high signal asserted by the PHY layer when RUDATA contains the first valid byte of a cell. To support multiple PHY configurations.
$\overline{\text{RUEMPTY}}$/ RUCLAV	Empty/Cell Available.	O	TTL	For UTOPIA flow control. The $\overline{\text{RUEMPTY}}$ definition applies to word level flow control, and RUCLAV definition applies to cell level flow control.
RUCLKO	Receive UTOPIA Clock Out	O	TTL	The RUCLK looped back out.

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Pin	Name	I/O	Type	Description
RUCLK	Receive UTOPIA Clock	I	TTL	Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on RUDATA.
$\overline{\text{RUENB}}$	Receive UTOPIA Enable	I	TTL	Active low signal asserted by the ATM layer to indicate that RUDATA, RUSOC and RXPRTY will be sampled at the end of the next cycle. In MPHY configurations. $\overline{\text{RUENB}}$ is used to tri-state RUDATA, RUSOC and RUPRTY PHY layer outputs
TUDATA[31:0]	Transmit UTOPIA Data	I	TTL	Four-octet true data driven from ATM to PHY layer. TUDATA[31] is MSB.
TUCLK	Transmit UTOPIA Clock	I	TTL	Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TUDATA.
TUPRTY	Transmit UTOPIA Parity	I	TTL	TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31:0], driven by the ATM layer. The signal is only valid when asserted simultaneously with $\overline{\text{TUENB}}$.
TUSOC	Transmit UTOPIA Start Of Cell.	I	TTL	Active high signal asserted by the ATM layer when TUDATA contains the first valid byte of the cell. The signal is only valid when asserted simultaneously with $\overline{\text{TUENB}}$.
$\overline{\text{TUENB}}$	Transmit UTOPIA Enable	I	TTL	Active low signal asserted by the ATM layer during cycles when TUDATA contains valid cell data.
TUCLKO	Transmit UTOPIA Clock Out	O	TTL	The TUCLK input looped back out.
$\overline{\text{TUFULL}}$/ TUCLAV	Full/Cell Available.	O	TTL	For UTOPIA flow control. The $\overline{\text{TUFULL}}$ definition applies to word level flow control, and TUCLAV definition applies to cell level flow control.
D[7:0]	Data Bus	B	TTL	This bidirectional data bus is used to transfer data for microcontroller read/write access to internal UNI registers.
A[7:0]	Address Bus	I	TTL	This address bus selects specific internal registers during register read/write access.
ALE	Address Latch Enable	I	TTL	This signal controls internal latching of the address bus signals. When low the address bus A[7:0] is latched internal. When high the internal address bus latches are transparent. This signal will allow for interfacing to a multiplexed address/ data bus. The ALE signal has an internal pull-up resistor.
$\overline{\text{CSB}}$	Chip Select signal	I	TTL	This signal (active low) must always be asserted during register read/write access cycles. The $\overline{\text{CSB}}$ signal is used in conjunction with either the $\overline{\text{RDB}}$ or the $\overline{\text{WRB}}$ signal. The $\overline{\text{CSB}}$ signal has an internal pull-up resistor.
$\overline{\text{WRB}}$	Write Signal	I	TTL	This signal (active low) is used for register write operations. The D[7:0] value is written into the register selected by A[7:0] when $\overline{\text{WRB}}$ and $\overline{\text{CSB}}$ are both asserted (low). The $\overline{\text{WRB}}$ signal has an internal pull-up resistor.
$\overline{\text{RDB}}$	Read Signal	I	TTL	This signal (active low) is used for register read operations. The content of the register selected by A[7:0] is driving D[7:0] when $\overline{\text{RDB}}$ and $\overline{\text{CSB}}$ are both asserted (low). The $\overline{\text{RDB}}$ signal has an internal pull-up resistor.

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Pin	*Name*	*I/O*	*Type*	*Description*
$\overline{\text{RSTB}}$	Reset Signal	I	TTL	This signal (active low) provides (asynchronous) reset of the UNI device. The device is held in a reset state while the $\overline{\text{RSTB}}$ signal is low. All outputs are tri-state when RSTB is asserted. All outputs are tri-state when $\overline{\text{RSTB}}$ is asserted.
$\overline{\text{INTB}}$	Interrupt Signal	O	TTL	This signal (active low) is asserted when an internal interrupt source is pending and the interrupt is unmasked (enabled). The $\overline{\text{INTB}}$ signal is negated when the interrupt pending bits have been cleared. The $\overline{\text{INTB}}$ is an open drain signal.
GPIOO[3:0]	General Purpose Outputs	O	TTL	These general purpose outputs are programmable via internal CPU registers.
GPIOI[1:0]	General Purpose Inputs	I	TTL	These general purpose inputs are accessible via internal status registers.
LOS	Loss Of Signal	O	TTL	This is a status signal indicating if Loss Of Signal (LOS) has been detected. The LOS status is also available in an internal status register bit.
LOF	Loss Of Frame	O	TTL	This is a status signal indicating if Loss Of Frame (LOF) has been detected and declared. The LOF status is also available in an internal status register bit.
LCD-P	Loss of Cell Delineation	O	TTL	This signal is asserted when the cell delineation state machine is not in SYNC state. This alarm indication is also available via internal register access.
LOPC	Loss of Optical Carrier	I	TTL	This signal is being monitored and changes in the signal status may cause generation of an interrupt. This will allow for monitoring of the LOPC signal via the UNI device CPU interface.
TDO	Test Data Output	O	TTL	This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output which is inactive except when data scan shifting is in progress.
TDI	Test Data Input	I	TTL	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TCK	Test Clock	I	TTL	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Test Mode Select	I	TTL	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
$\overline{\text{TRSTB}}$	Test Reset	I	TTL	This signal (active low) provides an asynchronous test access port reset via the IEEE P1149.1 test access port. $\overline{\text{TRSTB}}$ is a schmitt triggered input with an internal pull-up resistor.
OE	Output Enable	I	TTL	When deasserted (set low), all TTL device outputs are tri-stated. The OE signal has an internal pull-up.

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Package Pin List

Signal	BGA pin	Signal	BGA pin	Signal	BGA pin
D[7]	W4	RUDATA[23]	W15	TUDATA[25]	K19
D[6]	Y4	RUDATA[22]	V15	TUDATA[24]	J19
D[5]	V5	RUDATA[21]	Y16	TUDATA[23]	J18
D[4]	U6	RUDATA[20]	W16	TUDATA[22]	H20
D[3]	W5	RUDATA[19]	U15	TUDATA[21]	J17
D[2]	Y5	RUDATA[18]	V16	TUDATA[20]	H19
D[1]	V6	RUDATA[17]	Y17	TUDATA[19]	H18
D[0]	W6	RUDATA[16]	W17	TUDATA[18]	G20
A[7]	Y6	RUDATA[15]	U16	TUDATA[17]	G19
A[6]	V7	RUDATA[14]	V17	TUDATA[16]	H17
A[5]	U8	RUDATA[13]	U18	TUDATA[15]	G18
A[4]	W7	RUDATA[12]	T17	TUDATA[14]	F20
A[3]	Y7	RUDATA[11]	U19	TUDATA[13]	F19
A[2]	V8	RUDATA[10]	U20	TUDATA[12]	F18
A[1]	U9	RUDATA[9]	T18	TUDATA[11]	E20
A[0]	W8	RUDATA[8]	R17	TUDATA[10]	E19
ALE	V9	RUDATA[7]	T19	TUDATA[9]	F17
CSB	W9	RUDATA[6]	T20	TUDATA[8]	E18
WRB	Y9	RUDATA[5]	R18	TUDATA[7]	D20
RDB	U10	RUDATA[4]	R19	TUDATA[6]	D19
RSTB	V10	RUDATA[3]	R20	TUDATA[5]	E17
OE	W10	RUDATA[2]	P18	TUDATA[4]	D18
VDD5	Y10	RUDATA[1]	N17	TUDATA[3]	C17
INTB	V11	RUDATA[0]	P19	TUDATA[2]	D16
LOPC	W11	RUPRTY	P20	TUDATA[1]	B17
LOS	W12	RUSOC	N18	TUDATA[0]	A17
LOF	V12	RUEMPTY*/ RUCLAV	M17	TUPRTY	C16
LCD-P	Y13	RUCLKO	N19	TUSOC	D15
RUDATA[31]	U12	RUCLK	M18	TUCLK	B16
RUDATA[30]	W13	RUENB*	M19	TUENB*	A16
RUDATA[29]	V13	TUDATA[31]	M20	TUCLKO	C15
RUDATA[28]	Y14	TUDATA[30]	L17	TUFULL*/ TUCLAV	B15
RUDATA[27]	W14	TUDATA[29]	L18	RXRCLK	A15
RUDATA[26]	U13	TUDATA[28]	L19	TXRCLK	C14
RUDATA[25]	V14	TUDATA[27]	L20	TRSTB	D13

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Signal	*BGA pin*	*Signal*	*BGA pin*	*Signal*	*BGA pin*
RUDATA[24]	Y15	TUDATA[26]	K18	TDO	B14
TDI	A14	RLIN[2]-	F4	TLOUT[14]+	U1
TCK	C13	RLIN[3]-	E2	TLOUT[14]-	U2
TMS	D12	RLIN[3]+	E1	TLOUT[15]-	T4
GPIOO[3]	B13	RLIN[0]-	F3	TLOUT[15]+	U3
GPIOO[2]	C12	RLIN[0]+	F2	TLPRTY+	V4
GPIOO[1]	B12	RLIN[1]+	F1	TLPRTY-	U5
GPIOO[0]	A12	RLIN[1]-	G3	GND	A1
GPIOI[1]	D11	TLCLK+	H4	GND	A2
GPIOI[0]	C11	TLCLK-	G2	GND	A3
VDD5	B11	TLCLKOUT-	G1	GND	A9
RLCLK+	A11	TLCLKOUT+	H3	GND	A10
RLCLK-	C10	TLOUT[0]-	J4	GND	A13
RLPRTY+	B10	TLOUT[0]+	H2	GND	A18
RLPRTY-	B9	TLOUT[2]-	J3	GND	A19
RLIN[15]-	C9	TLOUT[2]+	J2	GND	A20
RLIN[15]+	A8	TLOUT[1]+	J1	GND	B1
RLIN[14]-	D9	TLOUT[1]-	K4	GND	B20
RLIN[14]+	B8	TLOUT[4]-	K3	GND	C1
RLIN[13]-	C8	TLOUT[4]+	K2	GND	C20
RLIN[13]+	A7	TLOUT[3]+	K1	GND	H1
RLIN[12]+	B7	TLOUT[3]-	L3	GND	J20
RLIN[12]-	D8	TLOUT[5]+	L2	GND	K20
RLIN[11]-	C7	TLOUT[5]-	M2	GND	L1
RLIN[11]+	A6	TLOUT[6]-	M3	GND	M1
RLIN[10]+	B6	TLOUT[6]+	N1	GND	N20
RLIN[10]-	C6	TLOUT[7]-	M4	GND	V1
RLIN[9]+	A5	TLOUT[7]+	N2	GND	V20
RLIN[9]-	B5	TLOUT[8]-	N3	GND	W1
RLIN[8]-	D6	TLOUT[8]+	P1	GND	W20
RLIN[8]+	C5	TLOUT[9]+	P2	GND	Y1
RLIN[7]+	A4	TLOUT[9]-	N4	GND	Y2
RLIN[7]-	B4	TLOUT[10]-	P3	GND	Y3
RLIN[6]-	D5	TLOUT[10]+	R1	GND	Y8
RLIN[6]+	C4	TLOUT[11]+	R2	GND	Y11
RLIN[4]+	D3	TLOUT[11]-	R3	GND	Y12
RLIN[4]-	E4	TLOUT[12]+	T1	GND	Y18
RLIN[5]-	D2	TLOUT[12]-	T2	GND	Y19
RLIN[5]+	D1	TLOUT[13]-	R4	GND	Y20

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Signal	*BGA pin*	*Signal*	*BGA pin*	*Signal*	*BGA pin*
RLIN[2]+	E3	TLOUT[13]+	T3	VDD	B2
VDD	B3	VDD	D17	VDD	U17
VDD	B18	VDD	G4	VDD	V2
VDD	B19	VDD	G17	VDD	V3
VDD	C2	VDD	K17	VDD	V18
VDD	C3	VDD	L4	VDD	V19
VDD	C18	VDD	P4	VDD	W2
VDD	C19	VDD	P17	VDD	W3
VDD	D4	VDD	U4	VDD	W18
VDD	D7	VDD	U7	VDD	W19
VDD	D10	VDD	U11		
VDD	D14	VDD	U14		

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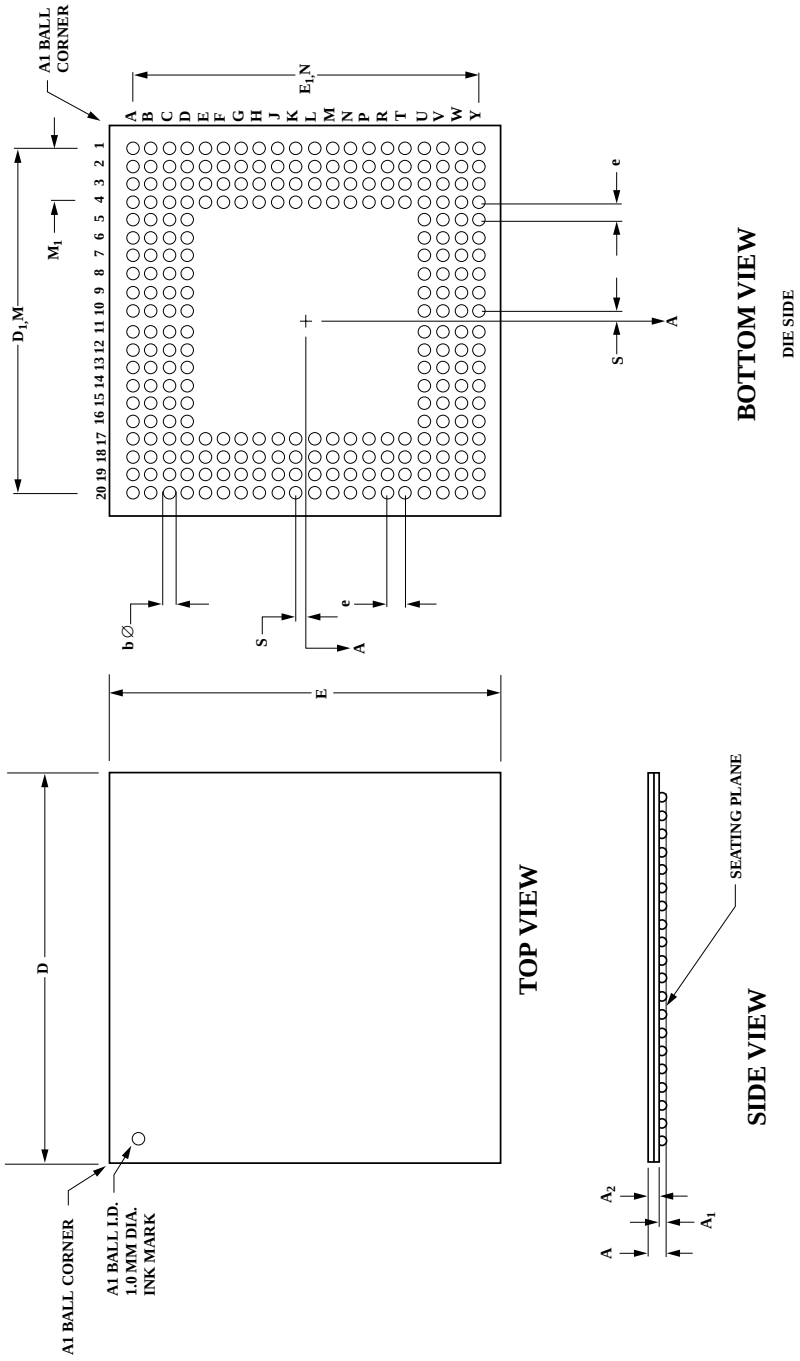
Package Information

BGA Package Dimensions



Item	*mm*	*Tolerance*
A	1.54	+/- .13
A1	0.63	+/- .07
A2	0.91	+/- .06
D	27.00	+/- .10
D1	24.13	+/- .10
E	27.00	+/- .10
E1	24.13	+/- .10
M,N	20 x 20	
M1	2-4	
b	0.75	+/- .15
e	1.27	
S	0.635	MAX

Package #: 101-324-6
Issue #: 1

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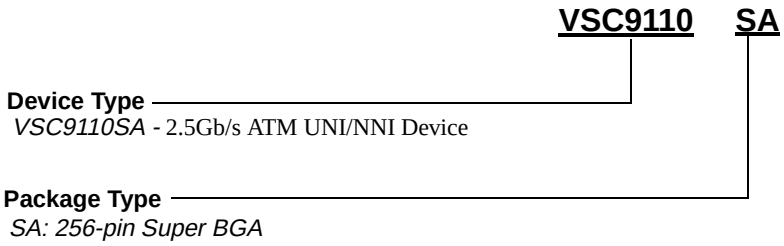
Ordering Information

The order number for this product is formed by a combination of the device number and package type.



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