reliminary Datasheet

SC8169

2.488 Gbit/sec / 2.7Gbit/sec
16:1 SONET/SDH Mux with Clock Generator

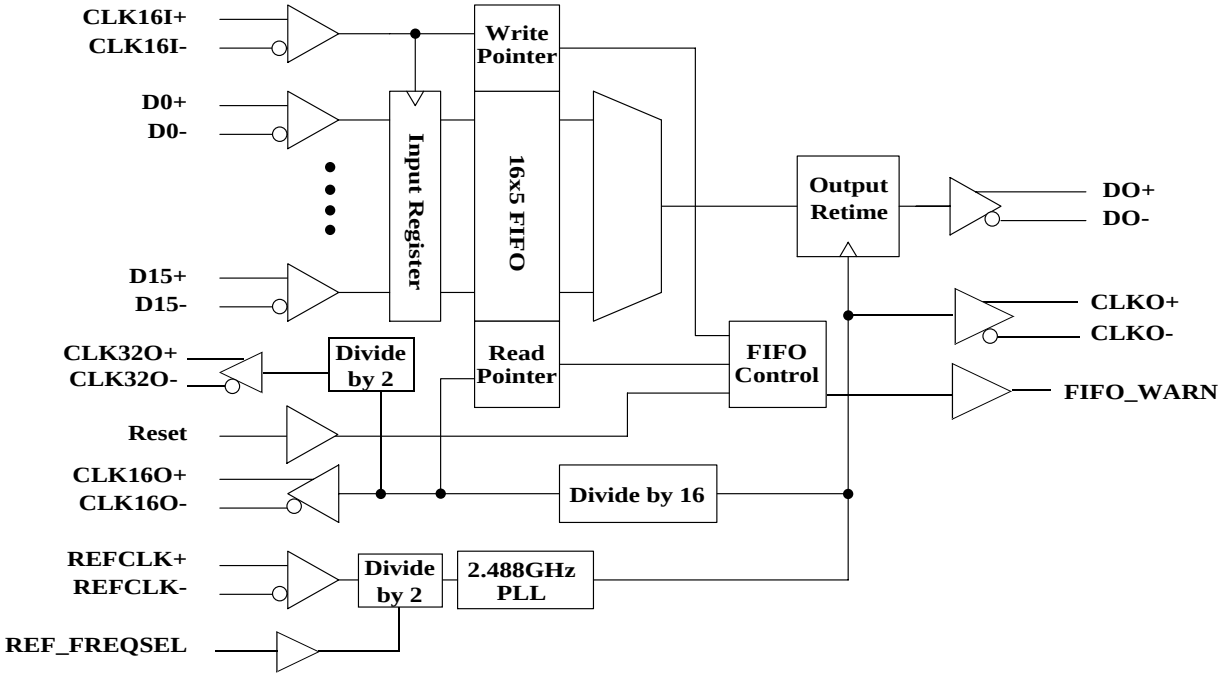
Features

- 2.488Gb/s 16:1 Multiplexer
- Targeted for SONET OC-48 / SDH STM-16 Applications
- Differential LVPECL Low Speed Interface
- On-chip PLL Based Clock Generator
- 128 Pin 14x20 mm PQFP Package
- Single +3.3V Supply

General Description

The VSC8169 is a 16:1 multiplexer with integrated clock generator for use in SONET/SDH systems operating at a standard 2.488Gb/s data rate or a forward error correction (FEC) data rate up to 2.7Gb/s. The internal clock generator uses a phase locked loop to multiply either a 77.76MHz (up to 84.38MHz- FEC) or a 155.52MHz (up to 168.75Mhz - FEC) reference clock in order to provide the 2.488GHz (up to 2.7GHz - FEC) clock for internal logic and output retiming. For use with the VSC9210 FEC Encoder / Decoder chipset running at 2.654Gbps, a reference clock of 82.944MHz (serial rate divided by 32) should be used. The 16 bit parallel interface incorporates an on-board FIFO eliminating loop timing design issues by providing a flexible parallel timing architecture. The device operates using a 3.3V power supply, and is packaged in a thermally enhanced plastic package. The thermal performance of the 128PQFP allows the use of the VSC8169 without a heat sink under most thermal conditions.

VSC8169 Block Diagram



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Functional Description

Low Speed Interface

The Upstream Device should use the CLK16O as the timing source for its final output latch (see Figure 1). The Upstream Device should then generate a CLK16I phase aligned with the data. The VSC8169 will latch D[15:0]± on the rising edge of CLK16I+. The data must meet setup and hold times with respect to CLK16I (see Table 2).

A FIFO exists within the VSC8169 to eliminate difficult system loop timing issues. Once the PLL has locked to the reference clock, RESET must be held low for a minimum of five CLK16 cycles to initialize the FIFO, then RESET should be set high and held constant for continuous FIFO operation. For the transparent mode of operation (no FIFO), simply hold RESET at a constant low state. (See Figure 2)

The use of a FIFO permits the system designer to tolerate an arbitrary amount of delay between CLK16O and CLK16I. Once RESET is asserted and the FIFO initialized, the delay between CLK16O and CLK16I can decrease or increase up to one period of the low speed clock (6.4ns). Should this delay drift exceed one period, the write pointer and the read pointer could point to the same word in the FIFO, resulting in a loss of transmitted data (a FIFO overflow). In the event of a FIFO overflow, an active low FIFO_WARN signal is asserted (for a minimum of 5 CLK16I cycles) which can be used to initiate a reset signal from an external controller.

The CLK16O± output driver is a LVPECL output driver designed to drive a 50Ω transmission line. The transmission line can be DC terminated with a split end termination scheme (see Figure 3), or DC terminated by 50Ω to V_{CC}-2V on each line (see Figure 4). At any time, the equivalent split-end termination technique can be substituted for the traditional 50Ω to V_{CC}-2V on each line. AC coupling can be achieved by a number of methods. Figure 5 illustrates an example AC coupling method for the occasion when the downstream device provides the bias point for AC coupling. If the downstream device were to have internal termination, the line to line 100Ω resistor may not be necessary.

Figure 1: Low Speed Systems Interface

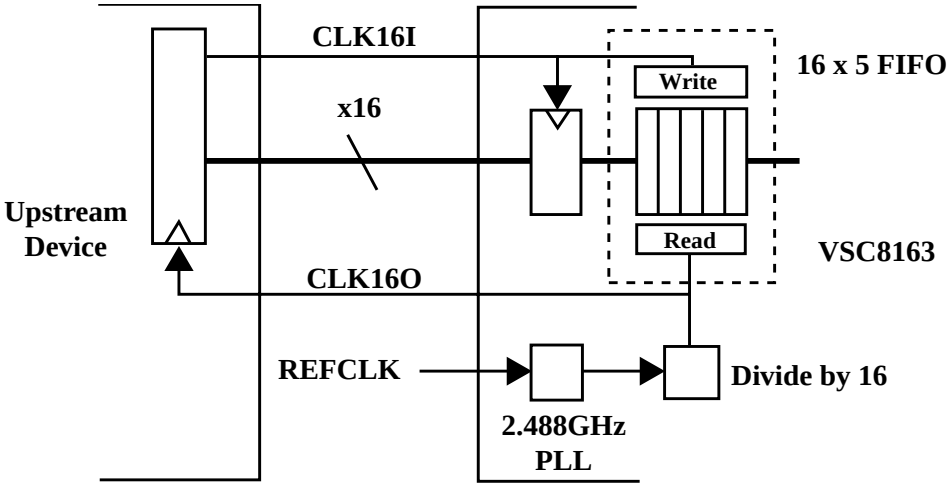
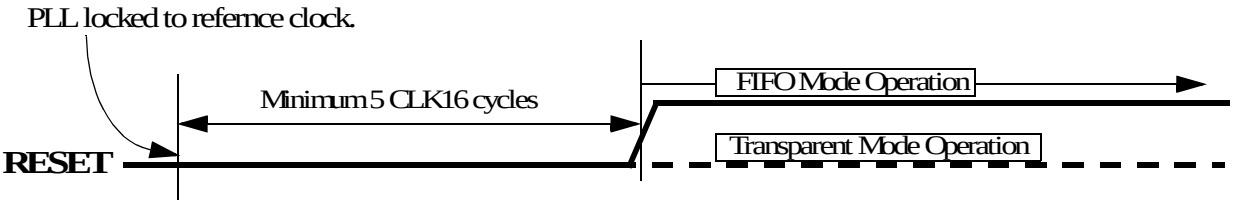


Figure 2: Enabling FIFO Operation



Holding RESET "low" for a minimum of 5 CLK16 cycles, then setting "high" enables FIFO operation. Holding RESET constantly "low" bypasses the FIFO for transparent mode operation.

Figure 3: Split-end DC Termination of CLK16O+/-, CLK32O+/-

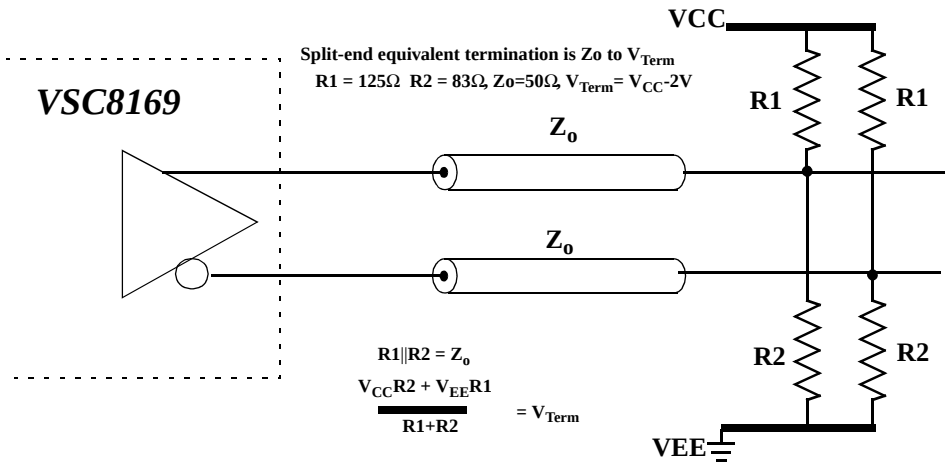


Figure 4: Traditional DC Termination of CLK16O+/-, CLK32O+/-

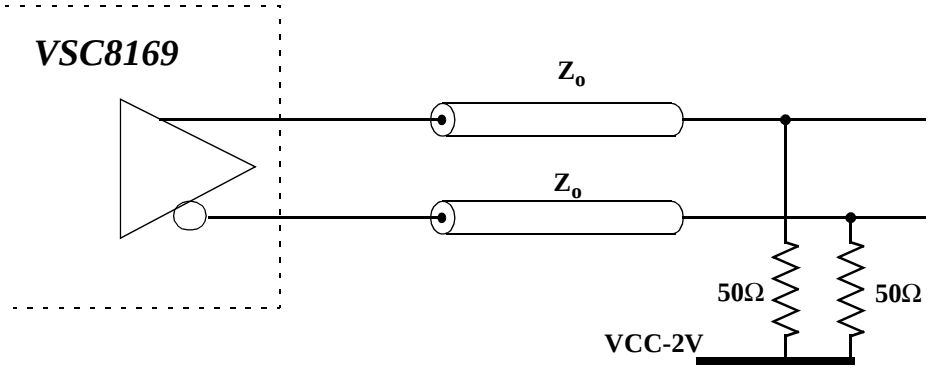


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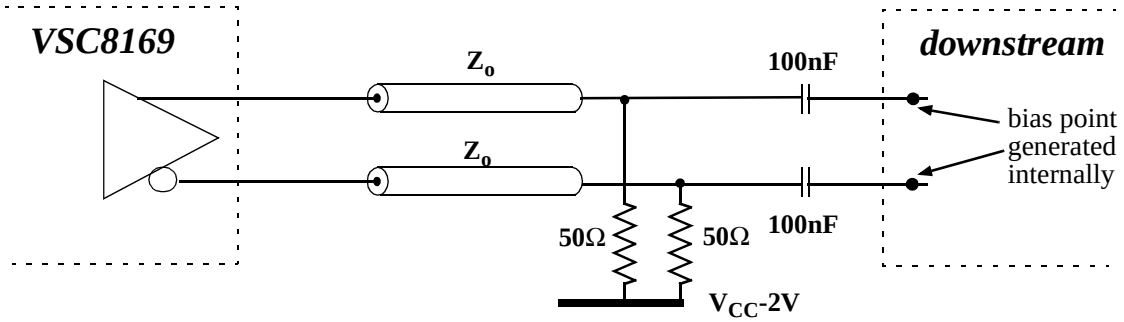
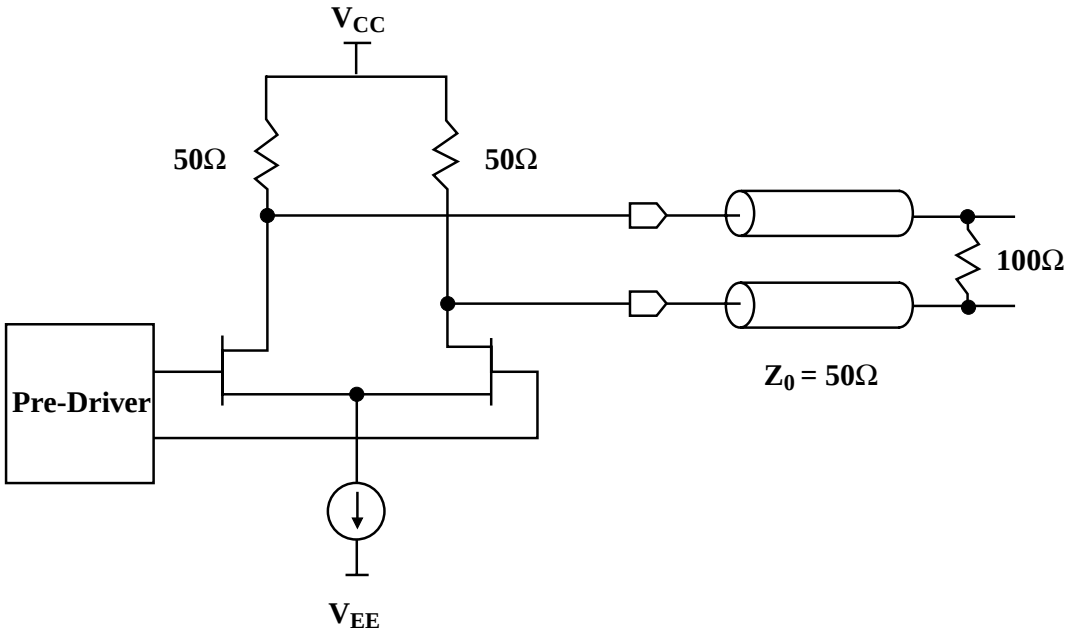
Figure 5: AC termination of CLK16O+/-, CLK32O+/-



High Speed Data & Clock Output

The high speed data and clock output drivers consist of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the load between true and complement outputs (see Figure 6). No connection to a termination voltage is required. The output driver is back terminated to 50Ω on-chip, providing a snubbing of any reflections. If used single-ended, the high speed output driver must still be terminated differentially at the load with a 100Ω resistor between true and complement outputs. The high speed clock output can be powered down for additional power savings. To power down the high speed clock, tie the associated pins to $3.3V_{CC}$ (see Table 3, Package Pin Descriptions, pins 5,6,7).

Figure 6: High Speed Output Termination



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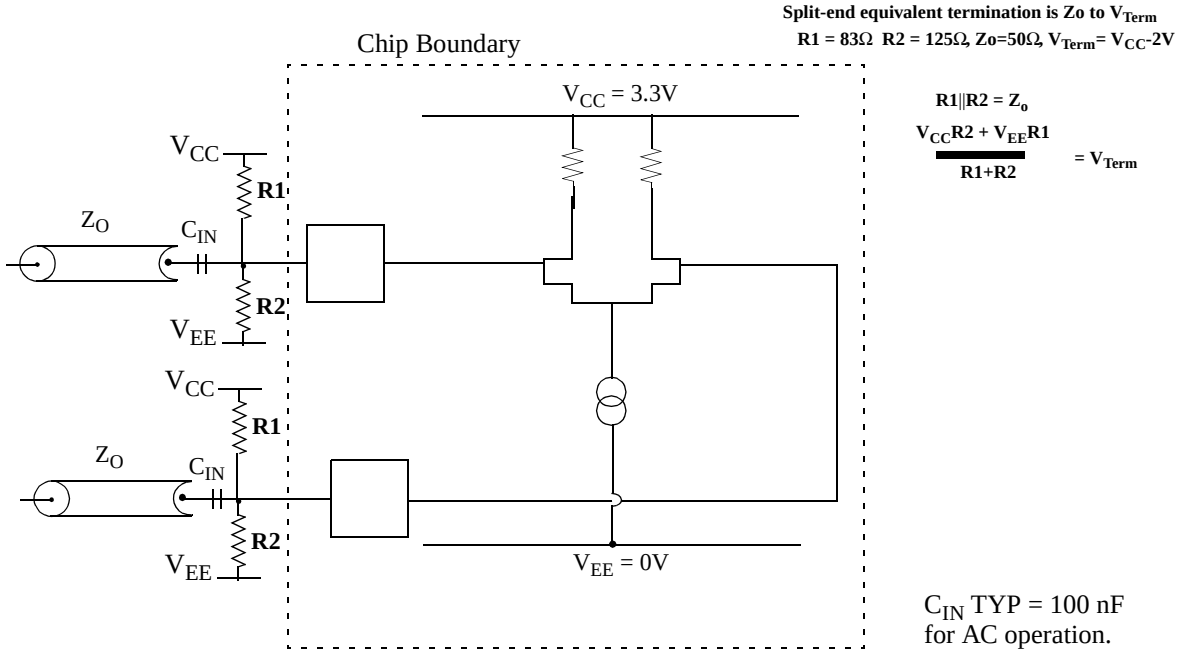
Clock Generator

An on-chip Phase Locked Loop (PLL) generates the 2.488GHz (2.67GHz - FEC) transmit clock from the externally provided REFCLK input. The on-chip PLL uses a low phase noise reactance based Voltage Controlled Oscillator (VCO) with an on-chip loop filter. The loop bandwidth of the PLL is within the SONET specified limit of 2MHz.

The customer can select to provide either a 77.76MHz (up to 84.38MHz- FEC) reference (recommended), or the 2x of that reference, 155MHz (up to 168.75Mhz - FEC). REF_FREQSEL is used to select the desired reference frequency. REF_FREQSEL = "0" designates REFCLK input as 77.76MHz (up to 84.38MHz- FEC), REF_FREQSEL = "1" designates REFCLK input as 155.52MHz (up to 168.75Mhz - FEC) . For use with the VSC9210 FEC Encoder / Decoder chipset running at 2.654Gbps, REF_FREQSEL = "0" should be selected with the REFCLK input as 82.944MHz (serial rate divided by 32).

The REFCLK should be of high quality since noise on the REFCLK below the loop band width of the PLL will pass through the PLL and appear as jitter on the output. Preconditioning of the REFCLK signal with a VCXO may be required to avoid passing REFCLK noise with greater than 4ps RMS of jitter to the output. The VSC8169 will output the REFCLK noise in addition to the intrinsic jitter from the VSC8169 itself during such conditions.

Figure 7: AC Termination of Low Speed LVPECL REFCLK, D[15:0] Inputs



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Low Speed Inputs

The incoming low speed data and reference clock input are received by LVPECL inputs D[15:0] and REFCLK. Off-chip termination of these inputs is required. For AC coupling, a bias voltage suitable for AC coupling needs to be provided. (See figure 7 for external biasing resistor scheme).

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. All serial data inputs have the same circuit topology, as shown in figure 7. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this common mode reference voltage (V_{CMI}) and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

Supplies

This device is specified as a LVPECL device with a single positive 3.3V supply. Should the user desire to use the device in an ECL environment with a negative 3.3V supply, then V_{CC} will be ground and V_{EE} will be -3.3V. If used with V_{EE} tied to -3.3V, the TTL control signals are still referenced to V_{EE}.

Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0402 packages.

Extra care needs to be taken when decoupling the analog power supply pins (labeled V_{CCANA}). In order to maintain the optimal jitter and loop bandwidth characteristics of the PLL contained in the VSC8169, the analog power supply pins should be filtered from the main power supply with a 10µH C-L-C pi filter. If preferred, a ferrite bead may be used to provide the isolation. The 0.1µF and 0.01µF decoupling capacitors are still required and must be connected to the supply pins between the device and the C-L-C pi filter (or ferrite bead).

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For low frequency decoupling, 47µF tantalum low inductance SMT caps are sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a -3.3V supply, then all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling 3.3V must be changed to -3.3V.

AC Characteristics

Figure 8: Timing Waveforms

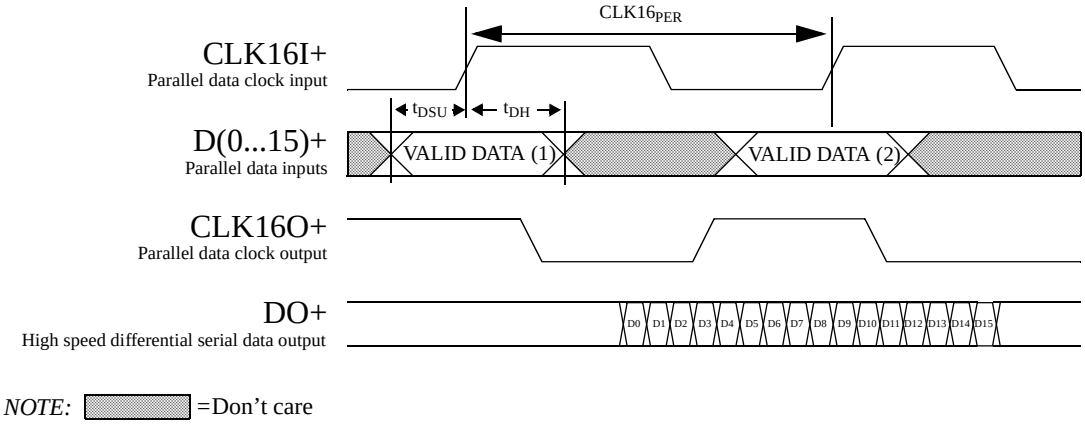

Figure 9: VSC8169 High Speed Output interface

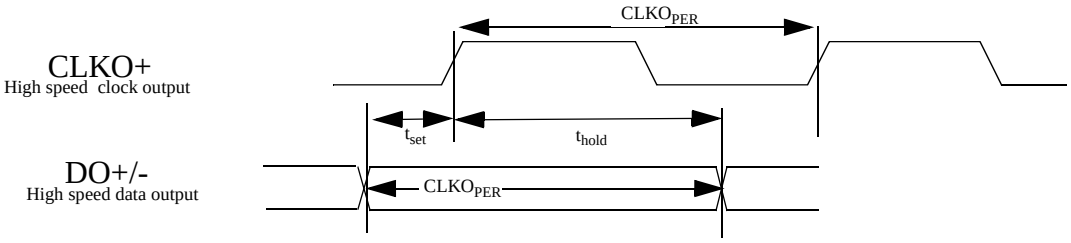

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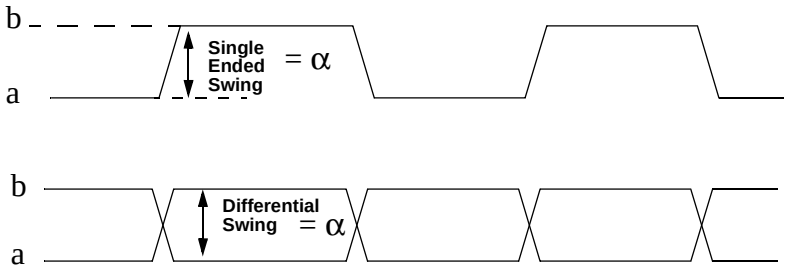
Table 1: AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{DSU}	Data Setup time to the rising edge of CLK16I+	0.75	—	—	ns.	
T_{DH}	Data hold time after the rising edge of CLK16+	1.0	—	—	ns.	
T_{DOR},T_{DOF}	DO± rise and fall time	—	—	120	ps.	20% to 80% into 100Ω load See Figure 6
t_{CLKR}, t_{CLKF}	CLK16O± rise and fall times	—	—	250	ps	See Figures 3 and 4
$CLK16O_D$	CLK16O± duty cycle	40	—	60	%	
$CLKI_D$	CLK16I± duty cycle	30	—	70	%	Assuming 10% distortion of CLKO
RCK_D	Reference Clock duty cycle	40	—	60	%	
$CLKO_D$	CLKO duty cycle	40	—	60	%	
$CLKO_{PER}$	CLKO period	—	401.9	—	ps	SONET based 77.76MHz ref_clk
$CLK16O_{PER}$	CLK16O period	—	6.4	—	ns	SONET based 77.76MHz ref_clk
$CLK32O_{PER}$	CLK32O period	—	12.9	—	ns	SONET based 77.76MHz ref_clk
t_{set}	DO setup time w.r.t. rising CLKO edge	—	90	—	ps	Inverting CLKO will switch (approx) t_{set} and t_{hold} values.
t_{hold}	DO hold time w.r.t. rising CLKO edge	—	310	—	ps	Inverting CLKO will switch (approx) t_{set} and t_{hold} values.
Clock Multiplier Performance						
T_{JF}	Output Data jitter (All Frequencies)	—	TBD	TBD	ps.	RMS, tested over all frequencies with 2ps RMS jitter on REFCLK
T_{JFPeak}	Output Data jitter (All Frequencies)	—	TBD	TBD	ps.	Peak to Peak, , tested over all frequencies with 2ps RMS jitter on REFCLK
T_{JS}	Output Data jitter (SONET Frequencies)	—	TBD	4	ps.	RMS, tested to SONET specification with 2ps RMS jitter on REFCLK
T_{JSPeak}	Output Data jitter (SONET Frequencies)	—	TBD	40	ps.	Peak to Peak, tested to SONET specification with 2ps RMS jitter on REFCLK

Figure 10: Differential and Single Ended Input / Output Voltage Measurement



* Differential swing (α) is specified as | b - a | (or | a - b |), as is the single ended swing. Differential swing is specified as equal in magnitude to single ended swing.

Table 2: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$V_{OH(DO)}$	Output HIGH voltage (DO)	V_{CC}-0.825	—	V_{CC}	V	See Figure 11
$V_{OL(DO)}$	Output LOW voltage (DO)	V_{CC}-1.30	—	V_{CC}-0.50	V	See Figure 11
$\Delta V_{OD(DO)}$	Data Output differential voltage (DO)	550	—	900	mV	100 Ohm Termination between DO± at Load
$\Delta V_{OCLK(CLKO)}$	CLK Output differential voltage (CLKO)	500	—	900	mV	100 Ohm Termination between DO± at Load
V_{CMO}	Output common mode voltage	2.10	—	3.00	V	
R_{DO}	Back Termination Impedance	40	—	60	Ohms	Guaranteed, not tested
V_{OH}	Output HIGH voltage (CLK16O, CLK32O)	V_{CC}-1.020	—	V_{CC}-0.700	V	See Figure 11
V_{OL}	Output LOW voltage (CLK16O, CLK32O)	V_{CC}-2.000	—	V_{CC}-1.620	V	See Figure 11
V_{IH}	Input HIGH voltage (LVPECL)	V_{CC}-1.100	—	V_{CC}-0.700	V	
V_{IL}	Input LOW voltage (LVPECL)	V_{CC}-2.0	—	V_{CC}-1.540	V	
I_{IH}	Input HIGH Current (LVPECL)	—	—	200	uA	$V_{IN}=V_{IH}$(max)
I_{IL}	Input LOW Current (LVPECL)	-50	—	—	uA	$V_{IN}=V_{IL}$(min)
R_i	Input Resistance (LVPECL)	10k	—	—	Ohms	

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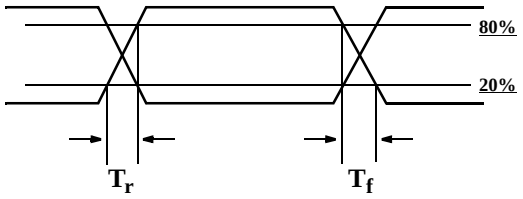
Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔV_I	Input differential voltage (LVPECL)	200	—	—	mV	
V_{CMI}	Input common mode voltage (LVPECL)	V_{CC}-1.5	—	V_{CC}-0.5	V	
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)		—	0.5	V	I_{OL} = +1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0.0	—	0.8	V	
I_{IH}	Input HIGH Current (TTL)	—	—	500	uA	V_{IN} = 2.4V
I_{IL}	Input LOW Current (TTL)	—	—	-500	uA	V_{IN} = 0.4V
V_{CC}	Supply voltage	3.14	—	3.47	V	3.3V± 5%
P_D	Power dissipation	—	1.2	1.7	W	Outputs open, V_{CC} = V_{CC} max
I_{CC}	Supply Current	—	350	490	mA	Outputs open, V_{CC} = V_{CC} max

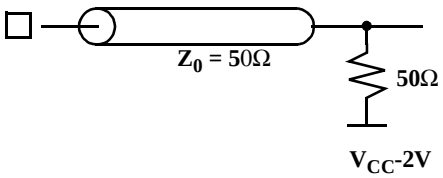
Figure 11: Parametric Measurement Information

PECL Rise and Fall Time



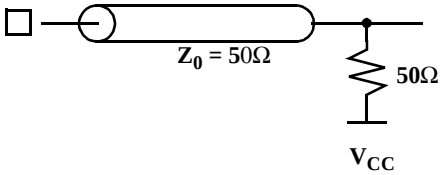
Parametric Test Load Circuit

Serial Output Load



Parametric Test Load Circuit

High Speed Data Output



Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{CC} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to +5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{CC} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +3.3V$\pm$5%

Operating Temperature Range ..... 0^{o}C Ambient to $+85^{o}$C Case Temperature

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8169 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Table 3: Package Pin Identification

Pin #	*Name*	*I/O*	*Level*	*Description*
1	NC	—	—	No connect, leave unconnected
2	NC	—	—	No connect, leave unconnected
3	NC	—	—	No connect, leave unconnected
4	VCC	—	+3.3V typ.	Positive power supply pin
5	VEEP_CLK	—	GND typ.	HS Clock V_{EE} power supply (Tie to $3.3V_{CC}$ for power down)
6	VEEP_CLK	—	GND typ.	HS Clock V_{EE} power supply (Tie to $3.3V_{CC}$ for power down)
7	VEEP_CLK	—	GND typ.	HS Clock V_{EE} power supply (Tie to $3.3V_{CC}$ for power down)
8	VCC	—	+3.3V typ.	Positive power supply pin
9	CLKO+	O	HS	High speed clock output, true
10	CLKO-	O	HS	High speed clock output, complement
11	VCC	—	+3.3V typ.	Positive power supply pin
12	VCC	—	+3.3V typ.	Positive power supply pin
13	NC	—	—	No connect, leave unconnected
14	NC	—	—	No connect, leave unconnected
15	VEE	—	GND typ.	Negative power supply pins
16	VEE	—	GND typ.	Negative power supply pins
17	VEE	—	GND typ.	Negative power supply pins
18	VCC	—	+3.3V typ.	Positive power supply pin
19	DO+	O	HS	High speed data output, true
20	DO-	O	HS	High speed data output, complement
21	VCC	—	+3.3V typ.	Positive power supply pin
22	NC	—	—	No connect, leave unconnected
23	VCC	—	+3.3V typ.	Positive power supply pin
24	VCC	—	+3.3V typ.	Positive power supply pin
25	VCC	—	+3.3V typ.	Positive power supply pin
26	VEE	—	GND typ.	Negative power supply pins
27	VEE	—	GND typ.	Negative power supply pins
28	VEE	—	GND typ.	Negative power supply pins
29	VEE	—	GND typ.	Negative power supply pins
30	VEE	—	GND typ.	Negative power supply pins
31	NC	—	—	No connect, leave unconnected
32	NC	—	—	No connect, leave unconnected
33	NC	—	—	No connect, leave unconnected
34	NC	—	—	No connect, leave unconnected
35	NC	—	—	No connect, leave unconnected
36	NC	—	—	No connect, leave unconnected

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Pin #	*Name*	*I/O*	*Level*	*Description*
37	NC	—	—	No connect, leave unconnected
38	REF_FREQSEL	I	TTL	Reference clock input select
39	VCC	—	+3.3V typ.	Positive power supply pin
40	VEE	—	GND typ.	Negative power supply pins
41	FIFO_WARN	O	TTL	FIFO overflow warning
42	VEE	—	GND typ.	Negative power supply pins
43	VCC	—	+3.3V typ.	Positive power supply pin
44	RESET	I	TTL	Reset to align FIFO Write and Read pointers
45	NC	—	—	No connect, leave unconnected
46	NC	—	—	No connect, leave unconnected
47	NC	—	—	No connect, leave unconnected
48	NC	—	—	No connect, leave unconnected
49	NC	—	—	No connect, leave unconnected
50	VCC	—	+3.3V typ.	Positive power supply pin
51	VEE	—	GND typ.	Negative power supply pins
52	CLK16O+	O	LVPECL	Low speed clock output, true. A divided by 16 version of the 2.488GHz PLL.
53	CLK16O-	O	LVPECL	Low speed clock output, complement. A divided by 16 version of the 2.488GHz PLL.
54	VCC	—	+3.3V typ.	Positive power supply pin
55	CLKI+	I	LVPECL	Low speed clock input for latching low speed data, true
56	CLKI-	I	LVPECL	Low speed clock input for latching low speed data, complement
57	VEE	—	GND typ.	Negative power supply pins
58	D0-	I	LVPECL	Low speed differential parallel data
59	D0+	I	LVPECL	Low speed differential parallel data
60	VCC	—	+3.3V typ.	Positive power supply pin
61	D1-	I	LVPECL	Low speed differential parallel data
62	D1+	I	LVPECL	Low speed differential parallel data
63	NC	—	—	No connect, leave unconnected
64	VCC	—	+3.3V typ.	Positive power supply pin
65	NC	—	—	No connect, leave unconnected
66	VCC	—	+3.3V typ.	Positive power supply pin
67	D2-	I	LVPECL	Low speed differential parallel data
68	D2+	I	LVPECL	Low speed differential parallel data
69	VEE	—	GND typ.	Negative power supply pins
70	D3-	I	LVPECL	Low speed differential parallel data
71	D3+	I	LVPECL	Low speed differential parallel data
72	VCC	—	+3.3V typ.	Positive power supply pin
73	D4-	I	LVPECL	Low speed differential parallel data

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Pin #	Name	I/O	Level	Description
74	D4+	I	LVPECL	Low speed differential parallel data
75	VCC	—	+3.3V typ.	Positive power supply pin
76	D5-	I	LVPECL	Low speed differential parallel data
77	D5+	I	LVPECL	Low speed differential parallel data
78	VEE	—	GND typ.	Negative power supply pins
79	D6-	I	LVPECL	Low speed differential parallel data
80	D6+	I	LVPECL	Low speed differential parallel data
81	VCC	—	+3.3V typ.	Positive power supply pin
82	D7-	I	LVPECL	Low speed differential parallel data
83	D7+	I	LVPECL	Low speed differential parallel data
84	VCC	—	+3.3V typ.	Positive power supply pin
85	D8-	I	LVPECL	Low speed differential parallel data
86	D8+	I	LVPECL	Low speed differential parallel data
87	VEE	—	GND typ.	Negative power supply pins
88	D9-	I	LVPECL	Low speed differential parallel data
89	D9+	I	LVPECL	Low speed differential parallel data
90	VCC	—	+3.3V typ.	Positive power supply pin
91	D10-	I	LVPECL	Low speed differential parallel data
92	D10+	I	LVPECL	Low speed differential parallel data
93	VCC	—	+3.3V typ.	Positive power supply pin
94	D11-	I	LVPECL	Low speed differential parallel data
95	D11+	I	LVPECL	Low speed differential parallel data
96	VEE	—	GND typ.	Negative power supply pins
97	D12-	I	LVPECL	Low speed differential parallel data
98	D12+	I	LVPECL	Low speed differential parallel data
99	VCC	—	+3.3V typ.	Positive power supply pin
100	D13-	I	LVPECL	Low speed differential parallel data
101	D13+	I	LVPECL	Low speed differential parallel data
102	VCC	—	+3.3V typ.	Positive power supply pin
103	VCC	—	+3.3V typ.	Positive power supply pin
104	NC	—	—	No connect, leave unconnected
105	D14-	I	LVPECL	Low speed differential parallel data
106	D14+	I	LVPECL	Low speed differential parallel data
107	VCC	—	+3.3V typ.	Positive power supply pin
108	D15-	I	LVPECL	Low speed differential parallel data
109	D15+	I	LVPECL	Low speed differential parallel data
110	VEE	—	GND typ.	Negative power supply pins
111	NC	—	—	No connect, leave unconnected
112	NC	—	—	No connect, leave unconnected

Pin #	*Name*	*I/O*	*Level*	*Description*
113	NC	—	—	No connect, leave unconnected
114	NC	—	—	No connect, leave unconnected
115	NC	—	—	No connect, leave unconnected
116	REFCLK+	I	LVPECL	Reference clock input, true
117	REFCLK-	I	LVPECL	Reference clock input, complement
118	VCC	—	+3.3V typ.	Positive power supply pin
119	VEE	—	GND typ.	Negative power supply pins
120	CLK32O+	O	LVPECL	Low speed clock output, true. A divided by 32 version of the 2.488GHz PLL.
121	CLK32O-	O	LVPECL	Low speed clock output, complement. A divided by 32 version of the 2.488GHz PLL.
122	VEE_ANA	—	GND typ.	Negative power supply pins for analog parts of CMU
123	VCC_ANA	—	+3.3V typ.	Positive power supply pins for analog parts of CMU
124	NC	—	—	No connect, leave unconnected
125	NC	—	—	No connect, leave unconnected
126	VEE	—	GND typ.	Negative power supply pins
127	VEE	—	GND typ.	Negative power supply pins
128	VCC	—	+3.3V typ.	Positive power supply pin

Note: No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative power supply rails may cause improper operation or failure of the device; or in extreme cases, cause permanent damage to the device.

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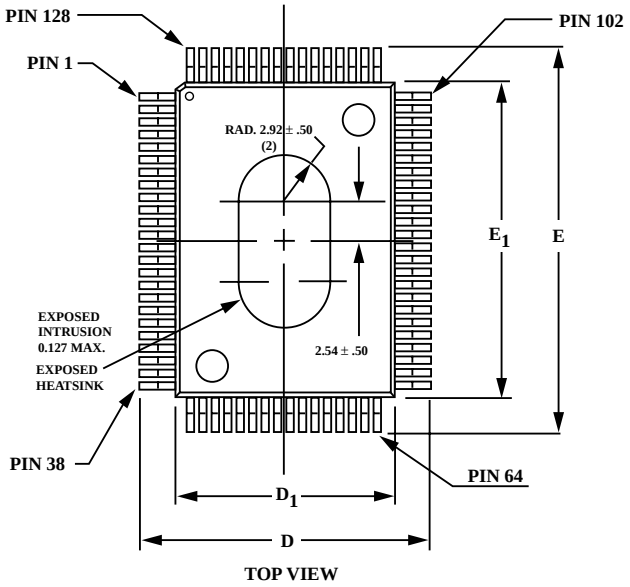
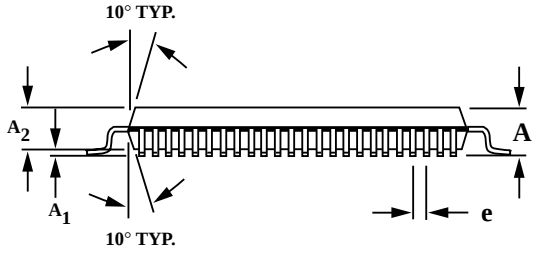
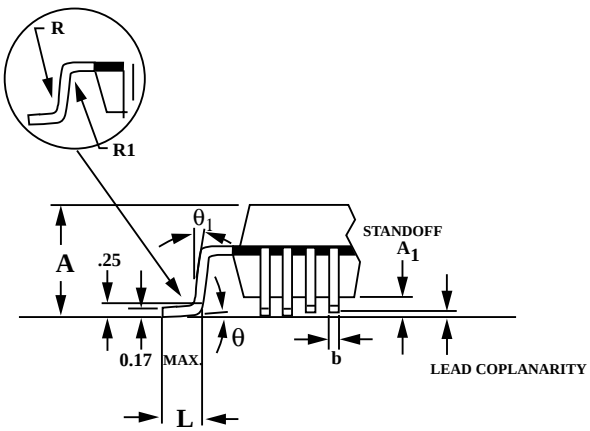
Package Information

128 PQFP Package Drawings



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

NOTES:

Package #: 101-322-5
Issue #: 2

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Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table

Table 4: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{jc}	Thermal resistance from junction to case.	1.34
θ_{ca}	Thermal resistance from case to ambient with no airflow, including conduction through the leads.	25.0

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 5: Thermal Resistance with Airflow

Airflow	θ_{ca} *(°C/W)*
100 lfpm	21
200 lfpm	18
400 lfpm	16
600 lfpm	14.5

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} Theta case to ambient at appropriate airflow
$T_{A(MAX)}$ Ambient Air temperature
$T_{C(MAX)}$ Case temperature (85°C for VSC8169)
$P_{(MAX)}$ Power (1.7 W for VSC8169)

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The results of this calculation are listed below:

Table 6: Maximum Ambient Air Temperature without Heatsink

Airflow	Max Ambient Temp ^{0}C
none	43
100 lfpm	49
200 lfpm	54
400 lfpm	58
600 lfpm	60

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8169 **QR**

Device Type
VSC8169:
2.488Gb/s to 2.7Gb/s
16:1 SONET/SDH Mux with Clock Generator

Package
QR: 128PQFP, 14x20mm Body

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

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