

Data Sheet
VSC8117**ATM/SONET/SDH 622/155Mb/s Transceiver MUX/DEMUX**
with Integrated Clock Generation and Clock Recovery**Features**

- Operates at Either STS-3/STM-1 (155.52Mb/s) or STS-12/STM-4 (622.08Mb/s) Data Rates
- Compatible with Industry ATM UNI Devices
- On-Chip Clock Generation of the 155.52MHz or 622.08MHz High-Speed Clock (Mux)
- On-Chip Clock Recovery of the 155.52MHz or 622.08MHz High-Speed Clock (Demux)
- 8-Bit Parallel TTL Interface
- SONET/SDH Frame Recovery
- Loss of Signal (LOS) Input and LOS Detection
- +3.3V/5V Programmable PECL Serial Interface
- Provides Equipment, Facilities and Split Loopback Modes as well as Loop Timing Mode
- Provides TTL and PECL Reference Clock Inputs
- Meets Bellcore, ITU and ANSI Specifications for Jitter Performance
- Low Power: 1.0 Watts Typical
- 64-Pin PQFP Package

General Description

The VSC8117 is an ATM/SONET/SDH compatible transceiver integrating an on-chip Clock Multiplication Unit (CMU) for the high-speed clock as well as a Clock and Data Recovery (CDR) unit with 8-bit serial-to-parallel and parallel-to-serial data conversion. The PLL clock is used for serialization in the transmit direction (MUX). The recovered clock is used for deserialization in the receive direction (DEMUX). The demultiplexer contains SONET/SDH frame detection and recovery. The device provides facility loopback, equipment loopback, and loop timing modes. The part is packaged in a 64-pin PQFP with integrated heat spreader for optimum thermal performance and reduced cost. The VSC8117 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

Functional Description

The VSC8117 is designed to provide a SONET/SDH-compliant interface between the high-speed optical networks and the lower speed User Network Interface devices such as the PM5355 S/UNI-622. The VSC8117 converts 8-bit parallel data at 77.76Mb/s or 19.44Mb/s to a serial bit stream at 622.08Mb/s or 155.52Mb/s, respectively. The VSC8117 also provides a Facility Loopback function which loops the received high-speed data and clock (optionally recovered on-chip) directly to the high-speed transmit outputs. A Clock Multiplier Unit (CMU) is integrated into the transmit circuit to generate the high-speed clock for the serial output data stream from input reference frequencies of 19.44 or 77.76MHz. The CMU can be bypassed with the recovered clock in loop timing mode thus synchronizing the entire part to a single clock. See the Block Diagram for the major functional blocks associated with the VSC8117.

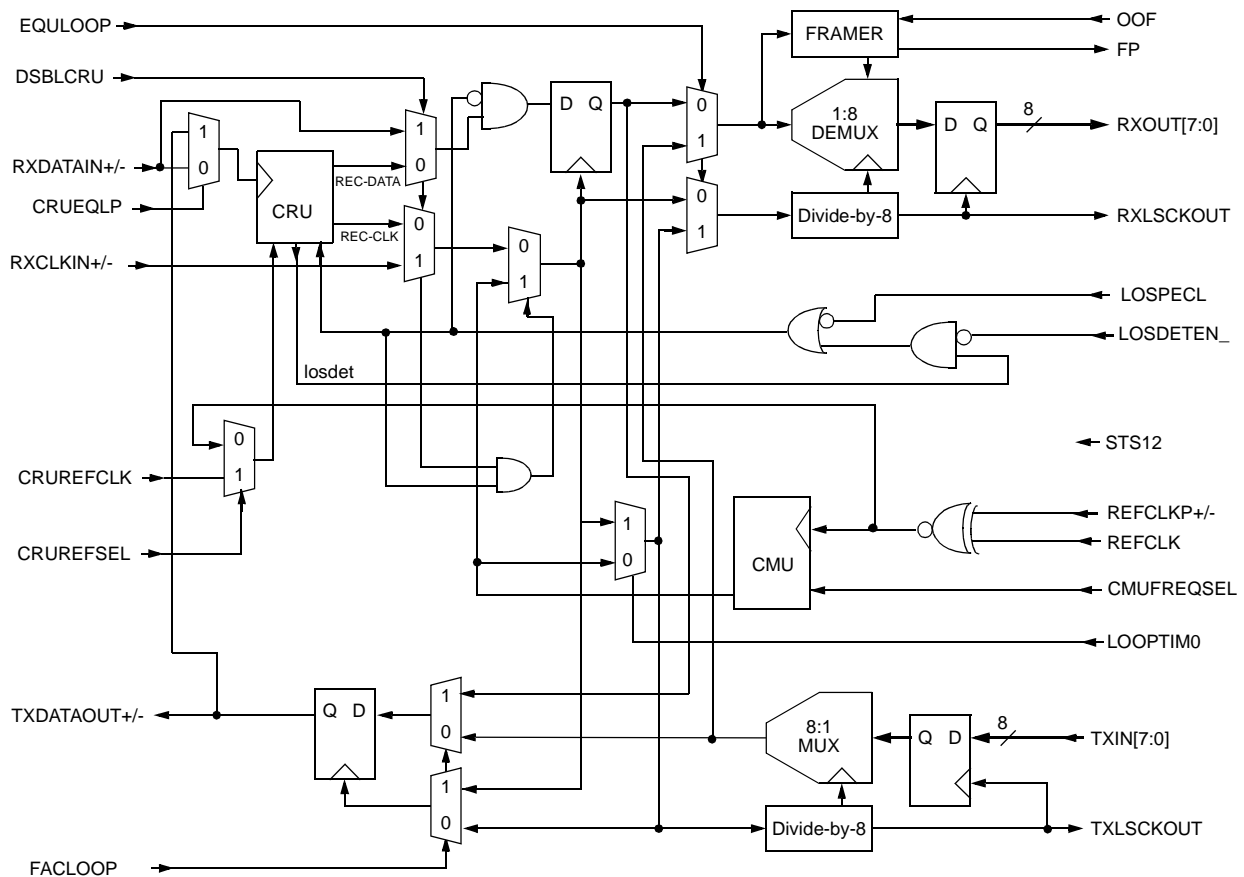
The receive section provides the serial-to-parallel conversion, converting the 622.08Mb/s or 155.52Mb/s bit stream to an 8-bit parallel output at 19.44Mb/s or 77.76Mb/s, respectively. A Clock Recovery Unit (CRU) is integrated into the receive circuit to recover the high-speed clock from the received serial data stream. The receive section provides an Equipment Loopback function which will loop the low-speed transmit data and clock back through the receive section to the 8-bit parallel data bus and clock outputs. The VSC8117 also provides the option of selecting between either its internal CRU's recovered clock and data signals or optics con-

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taining a CRU clock and data signals. (In this mode the VSC8117 operates just like the VSC8111 and VSC8116). The receive section also contains a SONET/SDH frame detector circuit which is used to provide frame pluses during the A1, A2 boundary in the serial to parallel converter. This only occurs when OOF is HIGH. Both internal and external LOS functions are supported. The high-speed serial signals can be made PECL-compatible or LVPECL-compatible by setting the proper voltage on the V_{DDP} supply pins.

VSC8117 Block Diagram



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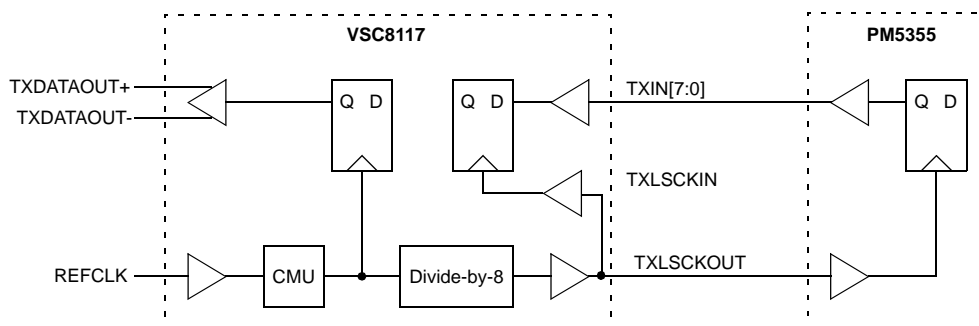
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Transmit Section

Byte-wide data is presented to TXIN[7:0] and is clocked into the part on the rising edge of TXLSCKOUT. TXLSCKOUT also latches TXIN[7:0] into the part as shown in Figure 1. The data is then serialized (MSB leading) and presented at the TXDATAOUT+/- pins. The serial output stream is synchronized to the CMU generated clock which is a phase-locked and frequency scaled version of the input reference clock. External control inputs CMUFREQSEL and STS-12 select the multiply ratio of the CMU for either STS-3 (155Mb/s) or STS-12 (622Mb/s) transmission (see Table 10). A divide-by-8 version of the CMU clock (TXLSCKOUT) should be used to synchronize the transmit interface of the UNI device to the transmit input registers on the VSC8117.

Figure 1: Data and Clock Transmit Block Diagram



Receive Section

High speed Non-Return to Zero (NRZ) serial data at 155Mb/s or 622Mb/s are received by the RXDATAIN inputs. The CRU recovers the high-speed clock from the serial data input. The serial data is converted to byte-wide parallel data and presented on RXOUT[7:0] pins. A divide-by-8 version of the high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT[7:0] data with the receive portion of the UNI device. The on-chip CRU is bypassed by setting the DSBLCRU input HIGH. In this mode, the serial input data and corresponding clock are received by the RXDATAIN and RXCLKIN inputs respectively. RXDATAIN is clocked in on the rising edge of RXCLKIN+ (see Figure 2).

The receive section also includes frame detection and recovery circuitry which detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held HIGH which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8117 will continually perform frame detection and recovery as long as this pin is held HIGH even if one or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT[7:0] will be byte-aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP which is synchronized with the byte-aligned third A2 byte on RXOUT[7:0]. The frame detector sends a FP pulse only if OOF is HIGH.

Loss of Signal

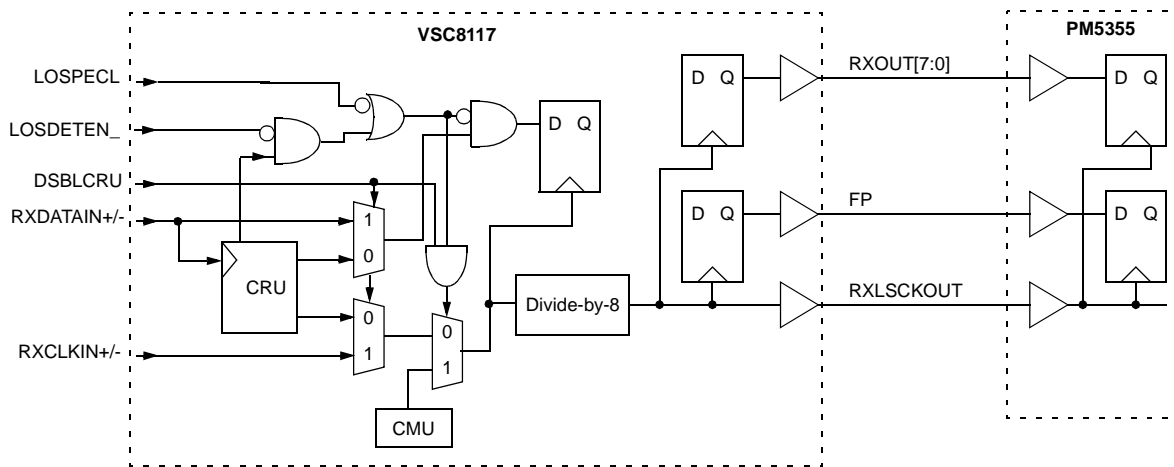
The VSC8117 features Loss of Signal (LOS) detection. Loss of Signal is declared if the incoming serial data stream has no transition continuously for more than 128 bits. During an LOS condition, the VSC8117 forces the receive data LOW which is an indication for any downstream equipment that an optical interface fail-

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ure has occurred. The receive section continues to be clocked by the CRU as it is now locked to the CRUREF-CLK unless DSBLCRU is active or CRUREFSEL is inactive, in which case it will be clocked by the CMU. This LOS condition will be removed when the part detects more than 16 transitions in a 128-bit time window. This LOS detection feature can be disabled by applying a high level to the LOSDETEN_ input. The VSC8117 also has a PECL input LOSPECL to force the part into a LOS state. Most optics have a PECL output usually called “SD” or “FLAG” indicating a lack of or presence of optical power. Depending on the optics manufacturer this signal is either active HIGH or active LOW. The LOSPECL input on the VSC8117 is active LOW.

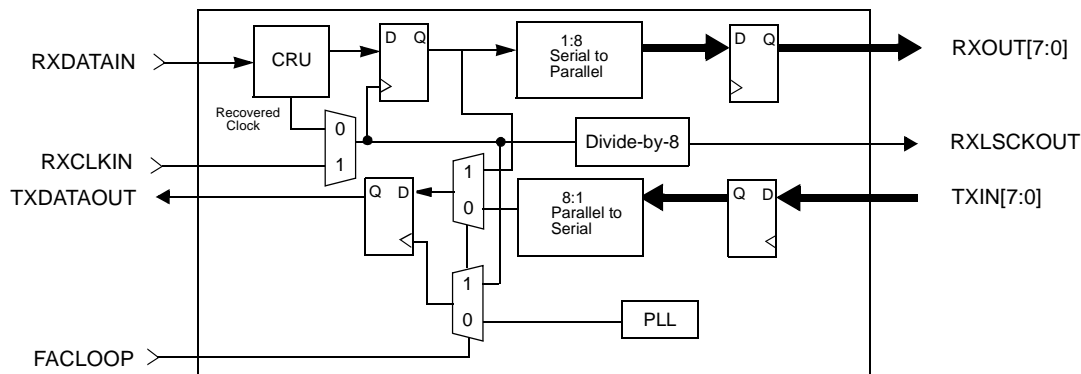
Figure 2: Data and Clock Receive Block Diagram



Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set HIGH, the Facility Loopback mode is activated and the high-speed serial receive data (RXDATAIN) is presented to the high-speed transmit output (TXDATAOUT). See Figure 3. In Facility Loopback mode the high-speed receive data (RXDATAIN) is also converted to parallel data and presented to the low-speed receive data output pins (RXOUT[7:0]). The receive clock (RXCLKIN) or the recovered clock is also divided down and presented to the low-speed clock output (RXLSCKOUT).

Figure 3: Facility Loopback Data Path



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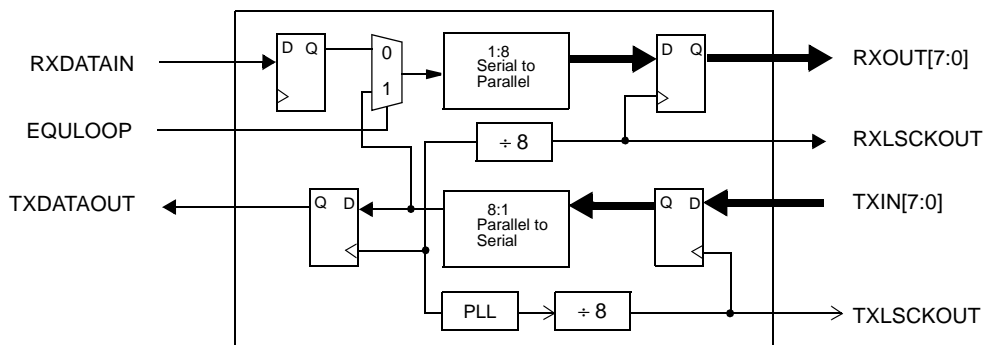
Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set HIGH, the Equipment Loopback mode is activated and the high-speed transmit data generated from the parallel to serial conversion of the low-speed data (TXIN[7:0]) is selected and converted back to parallel data in the receiver section and presented to the low-speed parallel outputs (RXOUT[7:0]). See Figure 4. The internally generated 155/622MHz clock is used to generate the low-speed receive clock output (RXLSCKOUT). In Equipment Loopback mode, the transmit data (TXIN[7:0]) is serialized by the on-chip CMU and presented at the high-speed output (TXDATAOUT).

CRU Equipment Loopback

Exactly the same as equipment loopback, the point where the transmit data is looped back is moved all the way back to the high-speed I/O. When the CRUEQLP signal is set HIGH, transmit data is looped back to the CRU, replacing RXDATAIN±.

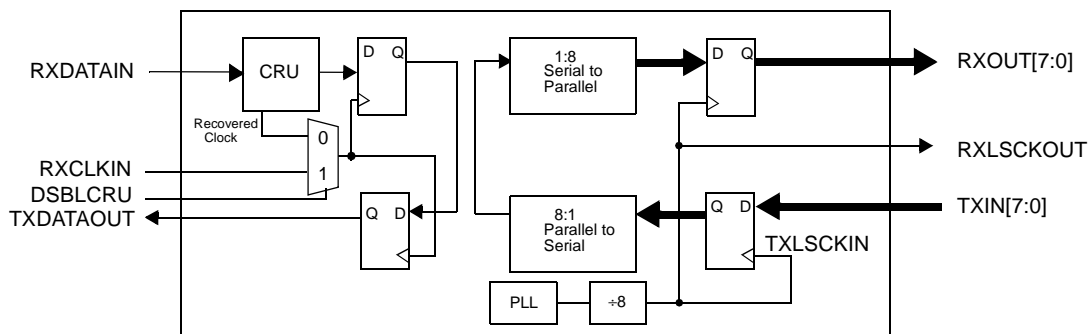
Figure 4: Equipment Loopback Data Path



Split Loopback

Equipment and facility loopback modes can be enabled simultaneously. In this case, high-speed serial data received (RXDATAIN) is mux'd through to the high-speed serial output (TXDATAOUT). The low-speed transmit byte wide bus (TXIN[7:0]) and (TXLSCKIN) are mux'd into the low-speed byte wide receive output bus (RXOUT[7:0]) and (RXLSCKOUT). See Figure 5.

Figure 5: Split Loopback Datapath



Loop Timing

LOOPTIM0 mode bypasses the CMU when the LOOPTIM0 input is asserted HIGH. In this mode, the CMU is bypassed by using the receive clock (RXCLKIN), and the entire part is synchronously clocked from a single external source.

Clock Synthesis

The VSC8117 uses an integrated Phase-Locked Loop (PLL) for clock synthesis of the 622MHz high-speed clock used for serialization in the transmitter section. The PLL is comprised of a Phase-Frequency Detector (PFD), an integrating operation amplifier and a Voltage Controlled Oscillator (VCO) configured in classic feed-back system. The PFD compares the selected divided down version of the 622MHz VCO (pin CMUFREQSEL selects the divide-by ratios of 8 or 32, see Table 10) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage controlled ring-oscillator with a center frequency of 622MHz.

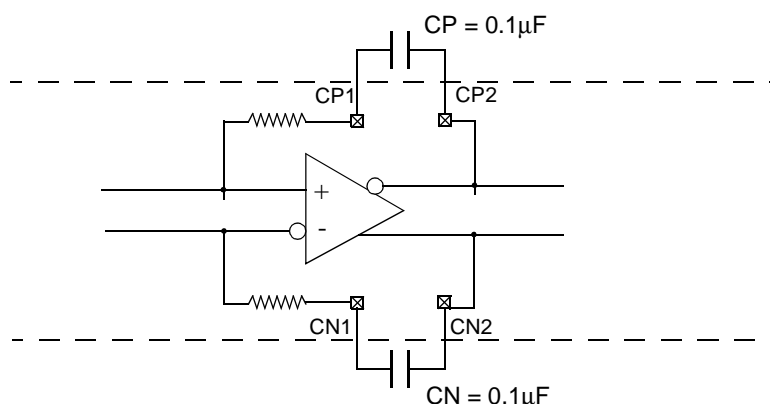
The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the CP1, CP2, CN1 and CN2 pins. The configuration of these external surface-mounted capacitors is shown in Figure 6. Table 1 shows the recommended external capacitor values for the configurable reference frequencies.

Good analog design practices should be applied to the board design for these external components. Tightly controlled analog ground and power planes should be provided for the PLL portion of the circuitry. The dedicated PLL power (VDDA) and ground (VSSA) pins should have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrite bead or a C-L-C choke (π filter) on the (VDDA) power pins. Note: Vitesse recommends a (π filter) C-L-C choke over using a ferrite bead. All ground planes should be tied together using multiple vias.

Table 1: Recommended External Capacitor Values

Reference Frequency [MHz]	Divide Ratio	CP	CN	Type	Size	Tolerance
19.44	32	0.1	0.1	X7R	0603/0805	$\pm 10\%$
77.76	8	0.1	0.1	X7R	0603/0805	$\pm 10\%$

Figure 6: External Integrator Capacitor



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Reference Clocks

To improve jitter performance and to provide flexibility, an additional differential PECL reference clock input is provided. This reference clock is internally XNOR'd with a TTL reference clock input to generate the reference for the CMU. Vitesse recommends using the differential PECL input and tying the unused TTL reference clock LOW. If the TTL reference clock is used, the positive side of the differential PECL reference clock REFCLKP+ should be tied to ground. REFCLKP+/- are internally biased with on-chip resistors to 1.65V (for 3.3V case). See Figure 13 for schematic of internal biasing of differential I/Os.

The CRU has the option of either using the CMU's reference clock or its own independent reference clock CRUREFCLK. This is accomplished with the control signal CRUREFSEL. The CRUREFCLK should be used if the system is being operated in either a regeneration or looptiming mode. In either of these modes, the quality of the CRUREFCLK is not a concern; thus it can be driven by a simple 77.76MHz crystal—the key is its' independence of the CMU's reference clock.

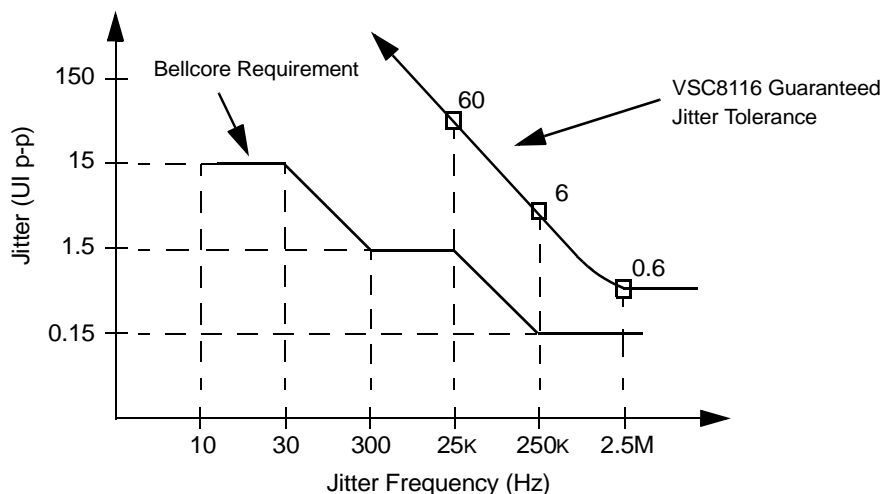
Clock Recovery

The fully monolithic CRU consists of a Phase Detector, a Frequency Detector, a Loop Filter and a VCO. The phase detector compares the phase information of the incoming data with the recovered clock. The frequency detector compares the frequency component of the data input with the recovered clock to provide the pull in energy during lock acquisition. The Loop Filter integrates the phase information from the phase and frequency detectors and provides the control voltage to the VCO.

Jitter Tolerance

Jitter Tolerance is the ability of the CRU to track timing variation in the received data stream. The Bellcore and ITU specifications allow the received optical data to contain jitter. The amount that must be tolerated is a function of the frequency of the jitter. At high frequencies, the specifications do not require the CRU to tolerate large amounts, whereas at low frequencies many unit intervals (bit times) of jitter have to be tolerated. The CRU is designed to tolerate this jitter with margin over the specification limits, see Figure 7. The CRU obtains and maintains lock based on the data transition information. When there is no transition on the data stream, the recovered clock frequency can drift. The VSC8117 can maintain lock over 100 bits of no switching on the data stream.

Figure 7: Jitter Tolerance



AC Timing Characteristics

Figure 8: Receive High-Speed Data Input Timing Diagram

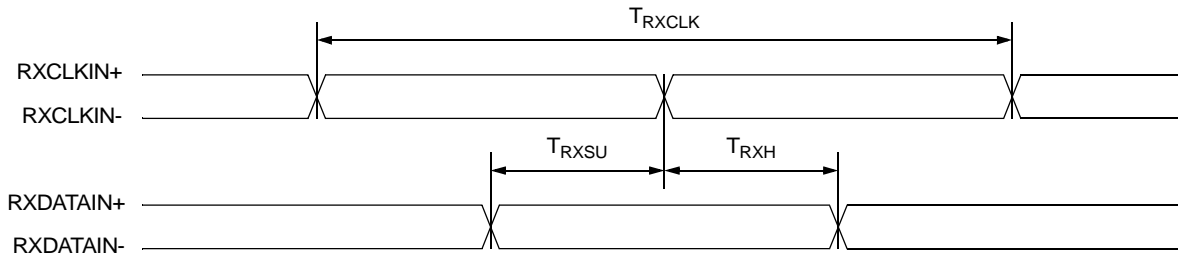


Table 2: Receive High-Speed Data Input Timing (STS-12 Operation)

Parameter	Description	Min	Typ	Max	Units
T_{RXCLK}	Receive clock period	—	1.608	—	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	400	—	—	ps
T_{RXH}	Serial data hold time with respect to RXCLKIN	100	—	—	ps

Table 3: Receive High-Speed Data Input Timing (STS-3 Operation)

Parameter	Description	Min	Typ	Max	Units
T_{RXCLK}	Receive clock period	—	6.43	—	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	1.5	—	—	ns
T_{RXH}	Serial data hold time with respect to RXCLKIN	1.5	—	—	ns

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Figure 9: Transmit Data Input Timing Diagram

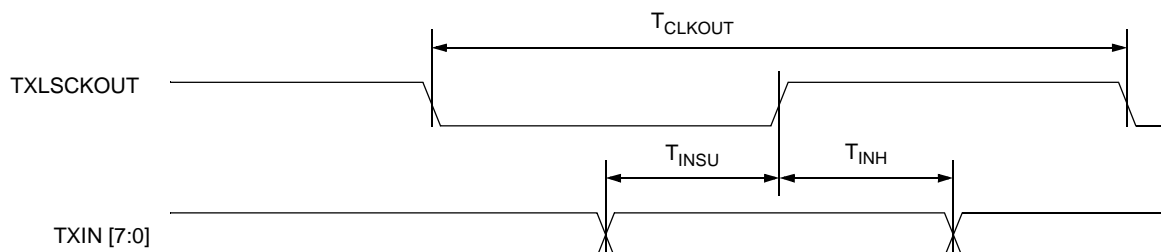


Table 4: Transmit Data Input Timing (STS-12 Operation)

Parameter	Description	Min	Typ	Max	Units
T _{CLKOUT}	Transmit data output byte clock period	—	12.86	—	ns
T _{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0	—	—	ns
T _{INH}	Transmit data hold time with respect to TXLSCKOUT ⁽¹⁾	1.0	—	—	ns

Table 5: Transmit Data Input Timing (STS-3 Operation)

Parameter	Description	Min	Typ	Max	Units
T _{CLKOUT}	Transmit data output byte clock period	—	51.44	—	ns
T _{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0	—	—	ns
T _{INH}	Transmit data hold time with respect to TXLSCKOUT ⁽¹⁾	1.0	—	—	ns

NOTE: (1) Duty cycle for TXLSCKOUT is 50% ±10% worst case

Figure 10: Receive Data Output Timing Diagram

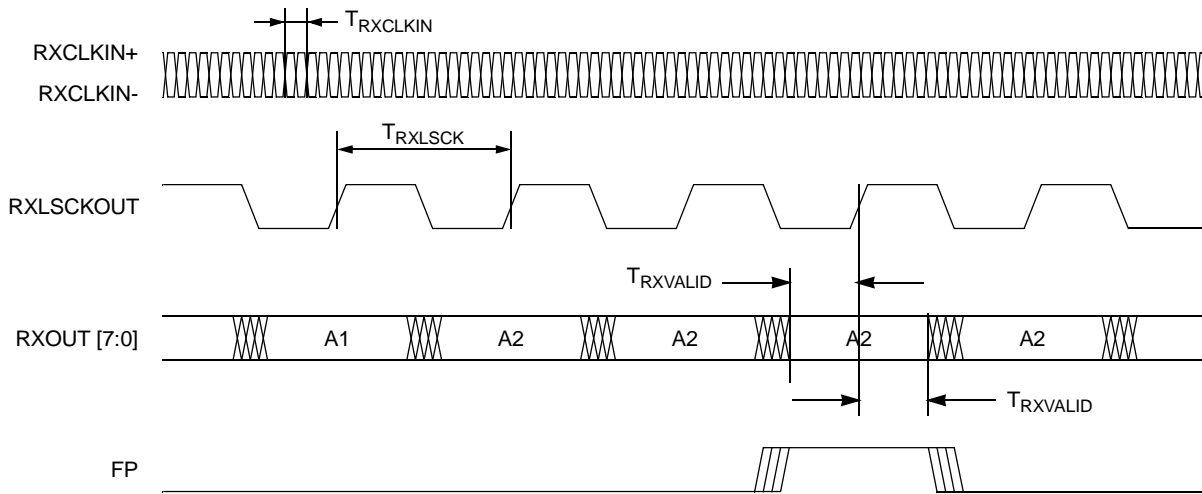


Table 6: Receive Data Output Timing (STS-12 Operation)

Parameter	Description	Min	Typ	Max	Units
$T_{RXCLKIN}$	Receive clock period	—	1.608	—	ns
T_{RXLSCK}	Receive data output byte clock period	—	12.86	—	ns
$T_{RXVALID}$	Time data on RXOUT[7:0] and FP is valid before and after the rising edge of RXLSCKOUT	4.0	—	—	ns
T_{PW}	Pulse width of frame detection pulse FP	—	12.86	—	ns

Table 7: Receive Data Output Timing (STS-3 Operation)

Parameter	Description	Min	Typ	Max	Units
$T_{RXCLKIN}$	Receive clock period	—	6.43	—	ns
$T_{RXLSCKT}$	Receive data output byte clock period	—	51.44	—	ns
$T_{RXVALID}$	Time data on RXOUT [7:0] and FP is valid before and after the rising edge of RXLSCKOUT	22	—	—	ns
T_{PW}	Pulse width of frame detection pulse FP	—	51.44	—	ns

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Data Latency

The VSC8117 contains several operating modes, each of which exercise different logic paths through the part. Table 8 bounds the data latency through each path with an associated clock signal.

Table 8: Data Latency

<i>Circuit Mode</i>	<i>Description</i>	<i>Clock Reference</i>	<i>Range of Clock Cycles</i>
Receive	MSB at RXDATAIN to data on RXOUT [7:0]	RXCLKIN	25-35
Facilities Loopback	MSB at RXDATAIN to MSB at TXDATAOUT	RXCLKIN	2-4

Clock Recovery Unit

Table 9: Reference Frequency for the CRU

<i>CRUREFSEL</i>	<i>STS12</i>	<i>CRUREFCLK Frequency (MHz)</i>	<i>Output Frequency (MHz)</i>
1	1	77.76 \pm 500ppm	622.08
1	0	77.76 \pm 500ppm	155.52
0	Uses CMU's Reference Clock (see Table 10)		

Clock Multiplier Unit

Table 10: Reference Frequency Selection and Output Frequency Control

<i>STS12</i>	<i>CMUFREQSEL</i>	<i>Reference Frequency (MHz)</i>	<i>Output Frequency (MHz)</i>
1	1	19.44	622.08
1	0	77.76	622.08
0	1	19.44	155.52
0	0	77.76	155.52

Table 11: Clock Multiplier Unit Performance

<i>Name</i>	<i>Description</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
RCd	Reference clock duty cycle	40	—	60	%
RCj	Reference clock jitter (RMS) at 77.76 MHz ref ⁽¹⁾	—	—	13	ps
RCj	Reference clock jitter (RMS) at 19.44 MHz ref ⁽¹⁾	—	—	5	ps
RC _f	Reference clock frequency tolerance ⁽²⁾	-20	—	+20	ppm

NOTES: Jitter specification is defined utilizing a 12kHz to 5MHz LP-HP single pole filter.

(1) These Reference Clock Jitter limits are required for the outputs to meet SONET system level jitter requirements (<10mUIrms).

(2) Required to meet SONET output frequency stability requirements.

AC Characteristics

Table 12: PECL and TTL Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
$T_{R,TTL}$	TTL Output Rise Time	—	2	—	ns	10-90%
$T_{F,TTL}$	TTL Output Fall Time	—	1.5	—	ns	10-90%
$T_{R,PECL}$	PECL Output Rise Time	—	350	—	ps	20-80%
$T_{F,PECL}$	PECL Output Fall Time	—	350	—	ps	20-80%

DC Characteristics

Table 13: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (PECL)	—	—	$V_{DDP} - 0.9V$	V	—
V_{OL}	Output LOW voltage (PECL)	0.7	—	—	V	—
V_{OCM}	Output common-mode range (PECL)	1.1	—	$V_{DDP} - 1.3V$	V	—
ΔV_{OUT75}	Differential output voltage (PECL)	600	—	1300	mV	75Ω to $V_{DDP} - 2.0V$
ΔV_{OUT50}	Differential output voltage (PECL)	600	—	1300	mV	50Ω to $V_{DDP} - 2.0V$
V_{IH}	Input HIGH voltage (PECL)	$V_{DDP} - 0.9V$	—	$V_{DDP} - 0.3V$	V	For single-ended
V_{IL}	Input LOW voltage (PECL)	0	—	$V_{DDP} - 1.72V$	V	For single-ended
ΔV_{IN}	Differential input voltage (PECL)	400	—	1600	mV	—
V_{ICM}	Input common-mode range (PECL)	$1.5 - \Delta V_{IN}/2$	—	$V_{DDP} - 1.0 - \Delta V_{IN}/2$	V	—
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	$I_{OH} = -1.0mA$
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	$I_{OL} = +1.0mA$
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	μA	$2.0V < V_{IN} < 5.5V$, Typical at 2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	μA	$-0.5V < V_{IN} < 0.8V$

Table 14: Power Supply Currents

Parameters	Description	Min	Typ	Max	Units	Conditions
I_{DD}	Power supply current from V_{DD}	—	—	480	mA	—
P_D	Power dissipation (worst case)	—	—	1.6	W	—

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Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{DD}) Potential to GND	-0.5V to +4V
PECL I/O Supply Voltage (V_{DDP}) Potential to GND	-0.5V to +6V
DC Input Voltage (PECL inputs).....	-0.5V to $V_{DDP} + 0.5V$
DC Input Voltage (TTL inputs)	-0.5V to 5.5V
DC Output Voltage (TTL Outputs).....	-0.5V to $V_{DD} + 0.5V$
Output Current (TTL Outputs)	$\pm 50mA$
Output Current (PECL Outputs).....	$\pm 50mA$
Case Temperature Under Bias	-55° to +125°C
Storage Temperature.....	-65°C to +150°C
Maximum Input ESD (Human Body Model)	1500 V

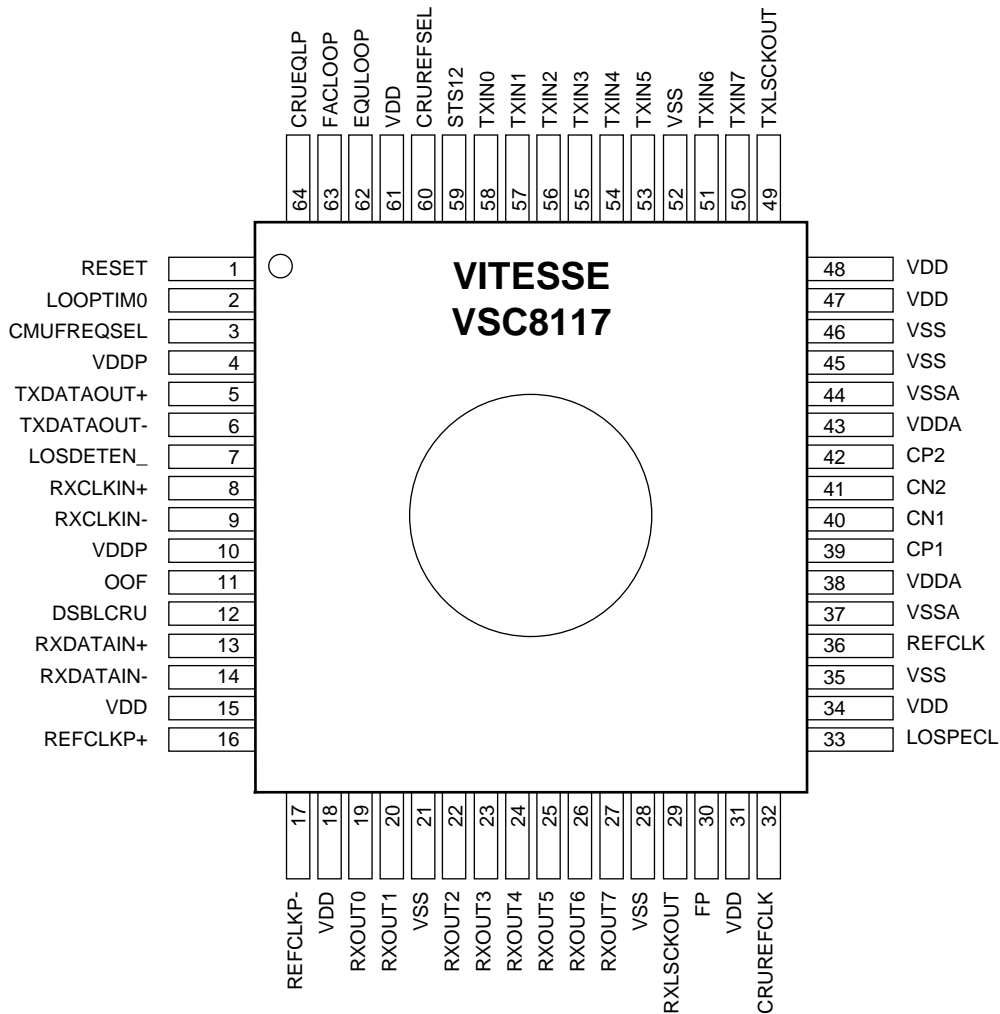
NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}).....	+3.3V $\pm 5\%$
PECL I/O Supply Voltage (V_{DDP})	+3.3V or +5.0V $\pm 5\%$
Commercial Operating Temperature Range	0°C Ambient to +70°C Case
Extended Operating Temperature Range.....	0°C to +85°C Ambient Equivalent to 0°C Ambient to +115°C Case
Industrial Operating Temperature Range	-40° ambient to +85°C Case

Package Pin Descriptions

Figure 11: Pin Diagram



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Table 15: Pin Identifications

<i>Pin</i>	<i>Signal</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
1	RESET	I	TTL	Resets frame detection, dividers, controls, active HIGH.
2	LOOPTIM0	I	TTL	Enable loop timing operation, active HIGH.
3	CMUFREQSEL	I	TTL	Reference clock frequency select, refer to Table 10.
4	VDDP	—	+3.3/+5V	+3.3V or +5V power supply for PECL I/Os
5	TXDATAOUT+	O	PECL	Transmit output, high-speed differential data, true
6	TXDATAOUT-	O	PECL	Transmit output, high-speed differential data, complement
7	LOSDETEN_	I	TTL	Enables internal LOS detection (active LOW).
8	RXCLKIN+	I	PECL	Receive high-speed differential clock input+
9	RXCLKIN-	I	PECL	Receive high-speed differential clock input-
10	VDDP	—	+3.3/+5V	+3.3V or +5V Power Supply for PECL I/Os
11	OOF	I	TTL	Out Of Frame; Frame detection initiated with high level.
12	DSBLCRU	I	TTL	Disable on-chip clock recovery unit, active HIGH.
13	RXDATAIN+	I	PECL	Receive high-speed differential data input, true
14	RXDATAIN-	I	PECL	Receive high-speed differential data input, complement
15	VDD	—	+3.3V	Power supply
16	REFCLKP+	I	PECL	PECL reference clock input, true
17	REFCLKP-	I	PECL	PECL reference clock input, complement
18	VDD	—	+3.3V	Power supply
19	RXOUT0	O	TTL	Receive output data bit 0
20	RXOUT1	O	TTL	Receive output data bit 1
21	VSS	—	GND	Ground
22	RXOUT2	O	TTL	Receive output data bit 2
23	RXOUT3	O	TTL	Receive output data bit 3
24	RXOUT4	O	TTL	Receive output data bit 4
25	RXOUT5	O	TTL	Receive output data bit 5
26	RXOUT6	O	TTL	Receive output data bit 6
27	RXOUT7	O	TTL	Receive output data bit 7
28	VSS	—	GND	Ground
29	RXLCKOUT	O	TTL	Receive byte clock output
30	FP	O	TTL	Frame detection pulse
31	VDD	—	+3.3V	Power supply
32	CRUREFCLK	I	TTL	Optional external CRU reference clock at 77.76MHz
33	LOSPECL	I	PECL	Loss of Signal Control. Single-ended PECL input, active LOW.

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<i>Pin</i>	<i>Signal</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
34	VDD	—	+3.3V	Power supply
35	VSS	—	GND	Ground
36	REFCLK	I	TTL	Reference clock input. Refer to Table 10.
37	VSSA	—	GND	Analog ground (CMU)
38	VDDA	—	+3.3V	Analog power supply (CMU)
39	CP1	—	Analog	CMU external capacitor (see Figure 6, and Table 1).
40	CN1	—	Analog	CMU external capacitor (see Figure 6, and Table 1).
41	CN2	—	Analog	CMU external capacitor (see Figure 6, and Table 1).
42	CP2	—	Analog	CMU external capacitor (see Figure 6, and Table 1).
43	VDDA	—	+3.3V	Analog power supply (CRU)
44	VSSA	—	GND	Analog ground (CRU)
45	VSS	—	GND	Ground
46	VSS	—	GND	Ground
47	VDD	—	+3.3V	Power supply
48	VDD	—	+3.3V	Power supply
49	TXLSCKOUT	O	TTL	Transmit byte clock out
50	TXIN7	I	TTL	Transmit input data bit7
51	TXIN6	I	TTL	Transmit input data bit6
52	VSS	—	GND	Ground
53	TXIN5	I	TTL	Transmit input data bit5
54	TXIN4	I	TTL	Transmit input data bit4
55	TXIN3	I	TTL	Transmit input data bit3
56	TXIN2	I	TTL	Transmit input data bit2
57	TXIN1	I	TTL	Transmit input data bit1
58	TXIN0	I	TTL	Transmit input data bit0
59	STS12	I	TTL	155Mb/s or 622Mb/s mode select. Refer to Table 10
60	CRUREFSEL	I	TTL	Selects between CMU's or CRU's REFCLK
61	VDD	—	+3.3V	Power Supply
62	EQULoop	I	TTL	Equipment Loopback. Loops low-speed byte wide transmit input data to receive output bus.
63	FACLoop	I	TTL	Facility Loopback. loops high-speed receive data and clock directly to transmit outputs.
64	CRUEQLP	I	TTL	Loops TXDATAOUT to the CRU replacing RXDATAIN+/-.

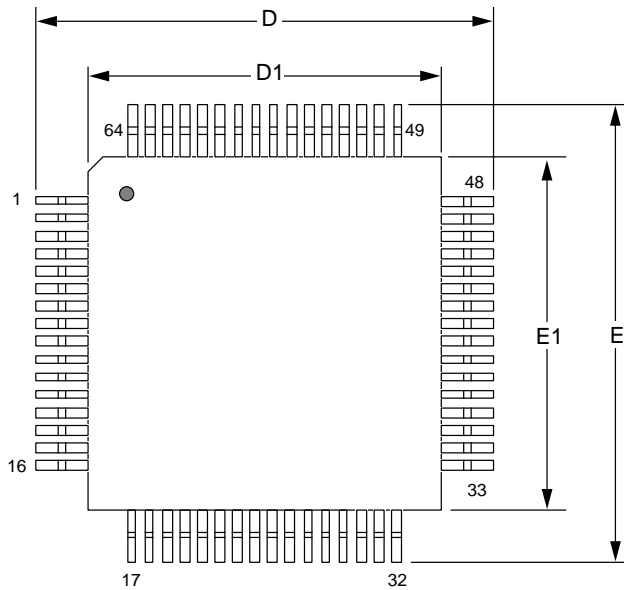
Data Sheet

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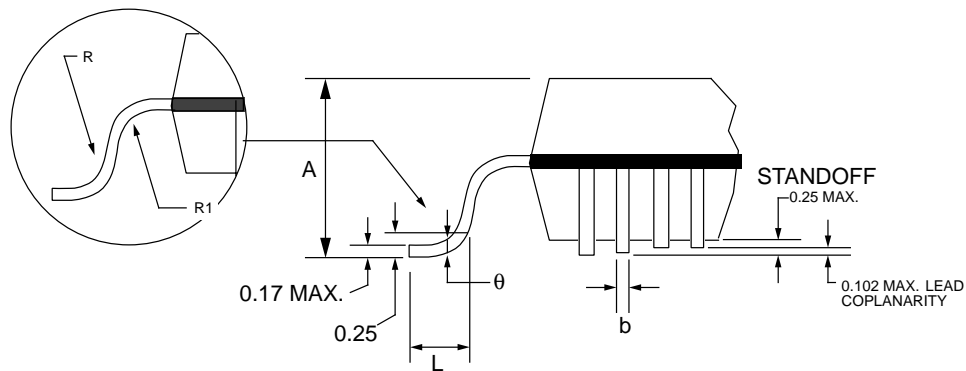
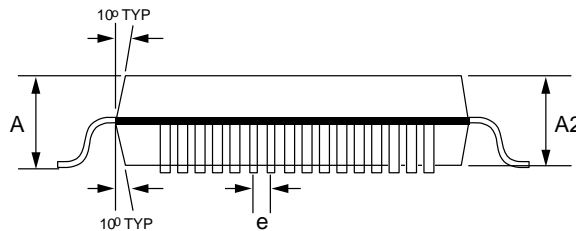
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Package Information

64-Pin PQFP Package Drawing



Item	mm	Tol.
A	2.45	MAX
A2	2.00	+.10/-.05
D	13.20	±.25
D1	10.00	±.10
E	13.20	±.25
E1	10.00	±.10
L	0.88	±.15/-.10
e	0.50	BASIC
b	0.22	±.05
θ	0° - 7°	
R	.30	TYP
R1	.20	TYP



NOTES:

All drawings not to scale
All units in mm unless otherwise noted.
10 x 10 mm Package # 101-266-1
14 x 14 mm Package # 101-262-1

Package Thermal Characteristics

The VSC8117 is packaged into a thermally-enhanced plastic quad flatpack (PQFP). This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed Copper Heat Spreader. The package construction is as shown in Figure 11.

The thermal resistance for the VSC8117 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the lead frame through the heat spreader overlap of the lead frame.

Figure 12: Package Cross Section

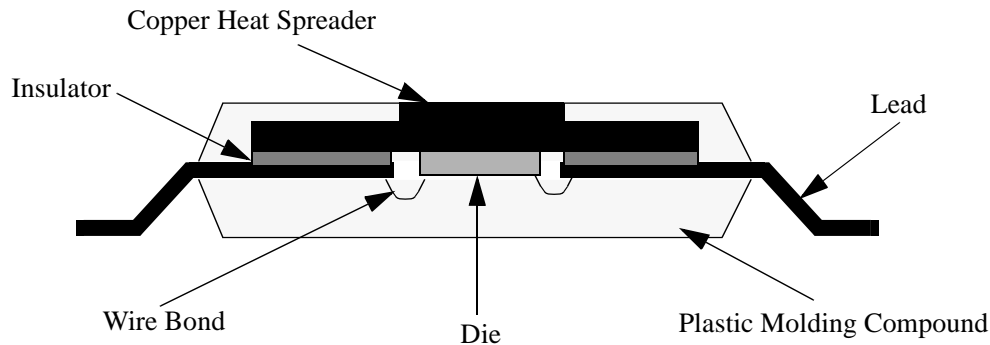


Table 16: 64-Pin PQFP Thermal Resistance

<i>Symbol</i>	<i>Description</i>	<i>Value (°C/W)</i>
θ_{JC}	Thermal resistance from junction-to-case	2.5
θ_{CA}	Thermal resistance from case-to-ambient in still air including conduction through the leads for a non-thermally saturated board.	37
θ_{CA-100}	Thermal resistance from case-to-ambient in 100 LPFM air	31
θ_{CA-200}	Thermal resistance from case-to-ambient in 200 LPFM air	28
θ_{CA-400}	Thermal resistance from case-to-ambient in 400 LPFM air	24
θ_{CA-600}	Thermal resistance from case-to-ambient in 600 LPFM air	22

The VSC8117QP1 is designed to operate at a maximum case temperature of up to 115°C. The user must guarantee that the maximum case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC8117QP1 in still air if the ambient temperature does not exceed 55°C (55°C = 115°C - 1.6W * 37°C/W). If operation above this ambient temperature is required, then an appropriate heatsink must be used with the part or adequate airflow must be provided.

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Ordering Information

The order number for this product is formed by a combination of the device number and package type.

	VSC8117	xx
Device Type		Package
622Mb/s MUX/DEMUX with CMU and CRU		QP: 64-Pin PQFP Commerical Temperature: 0°C ambient to +70°C case
		QP1: 64-Pin PQFP Extended Temperature: 0°C ambient to +115°C case
		QP2: 64-Pin PQFP Industrial Temperature: -40°C ambient to +85°C case

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Application Notes

DC-Coupling and Terminating High-Speed PECL I/Os

The high-speed signals on the VSC8117 (RXDATAIN, RXCLKIN, TXDATAOUT, REFCLKP, LOSPECL) use 3.3/5V programmable PECL I/Os which can be direct coupled to either +3.3V PECL or +5V PECL signals from the optics. These PECL levels are essentially ECL levels shifted positive by 3.3V or 5V. These PECL I/Os are referenced to the V_{DDP} supply (VDDP) and are terminated to ground. To program these I/Os for either 3.3V or 5V interface, the V_{DDP} pin (pins 4 and 10) is required to connect to 3.3V or 5V supplies accordingly.

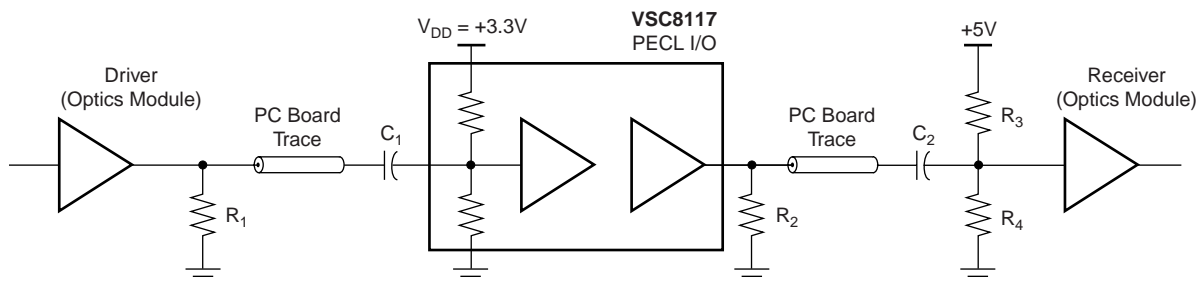
AC-Coupling and Terminating High-Speed PECL I/Os

If the optics modules provide ECL-level interface, the high-speed signals can be AC-coupled to the VSC8117 as well. The PECL receiver inputs of the VSC8117 are internally biased at $V_{DD}/2$. Therefore, AC-coupling to the VSC8117 inputs is accomplished by providing the pull-down resistor for the open-source PECL output and an AC-coupling capacitor used to eliminate the DC component of the output signal. This capacitor allows the PECL receivers of the VSC8117 to self-bias via its internal resistor divider network (see Figure 13).

The PECL output drivers are capable of sourcing current but not sinking it. To establish a LOW output level, a pull-down resistor, traditionally connected to $V_{DD}-2.0V$, is needed when the output FET is turned off. Since $V_{DD}-2.0V$ is usually not present in the system, the resistor could be terminated to ground for convenience. The VSC8117 output drivers should be either AC-coupled to the +5V PECL inputs of the optics module, or translated (DC-level shift). Appropriate biasing techniques for setting the DC-level of these inputs should be employed.

The DC biasing and 50 Ω termination requirements can easily be integrated together using a Thevenin equivalent circuit as shown in Figure 13. Figure 13 shows the appropriate termination values when interfacing 3.3V PECL to +5V PECL. This network provides the equivalent 50 Ω termination for the high-speed I/Os and also provides the required DC biasing for the receivers of the optics module. Table 17 contains recommended values for each of the components.

Figure 13: AC-Coupled High-Speed I/O



NOTE: Only one state of a differential signal is shown.

Table 17: AC Coupling Component Values

Component	Value	Tolerance
R_1	270 Ω	5%
R_2	75 Ω	5%
R_3	68 Ω	1%
R_4	190 Ω	1%
C_1, C_2, C_3, C_4	0.01 μ F High Frequency	—

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TTL Input Structure

The TTL inputs of the VSC8117 are 3.3V TTL which can accept 5.0V TTL levels within a given set of tolerances (see Table 13). The input structure, shown in Figure 14, uses a current limiter to avoid overdriving the input FETs.

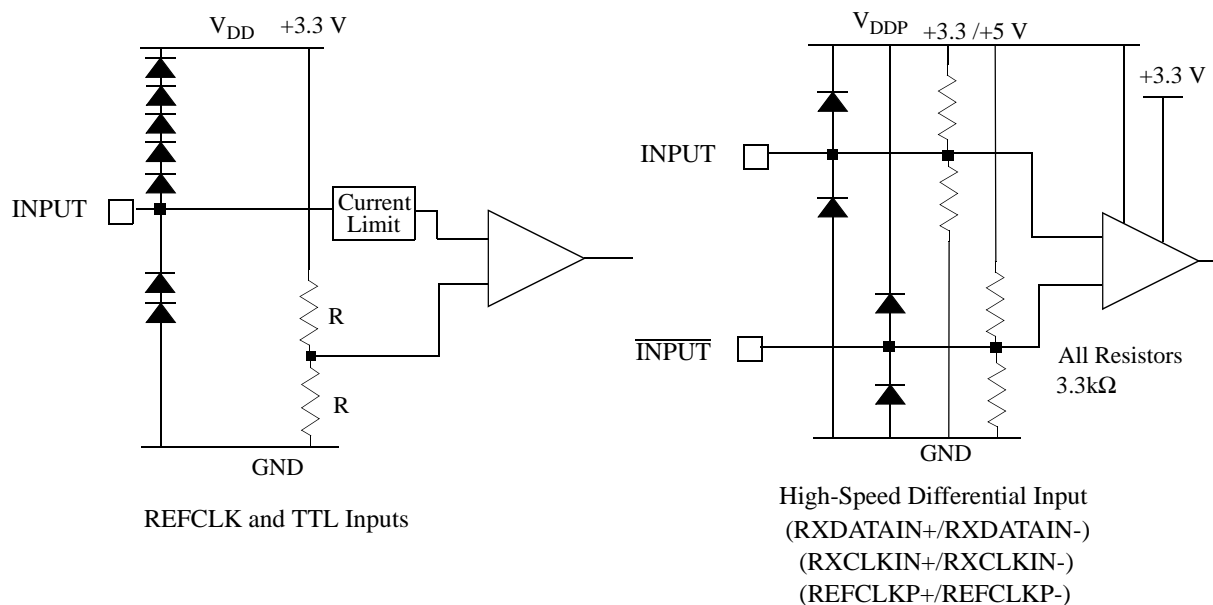
Layout of the High-Speed Signals

The routing of the high-speed signals should be done using good high-speed design practices. This would include using controlled impedance lines and keeping the distance between components to an absolute minimum. PECL signals need 50Ω traces, and TTL signals need 75Ω traces. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high-speed lines and insure the maximum eye opening. In addition, the output pull-down resistor should be placed as close to the VSC8117 pin as possible while the AC-coupling capacitor and the biasing resistors should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small out-line components and minimum pad sizes also helps in reducing discontinuities.

Ground Planes

The ground plane for the components used in the high-speed interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines. In addition, the smaller the ground planes, the less effective they are in reducing ground bounce noise and the more difficult to decouple. Sectioning of the positive supplies can provide some isolation benefits.

Figure 14: Input Structures





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