Preliminary Datasheet

VSC8109

155/622 Mhz 16 Channel PRBS Generator and Comparator.

Features

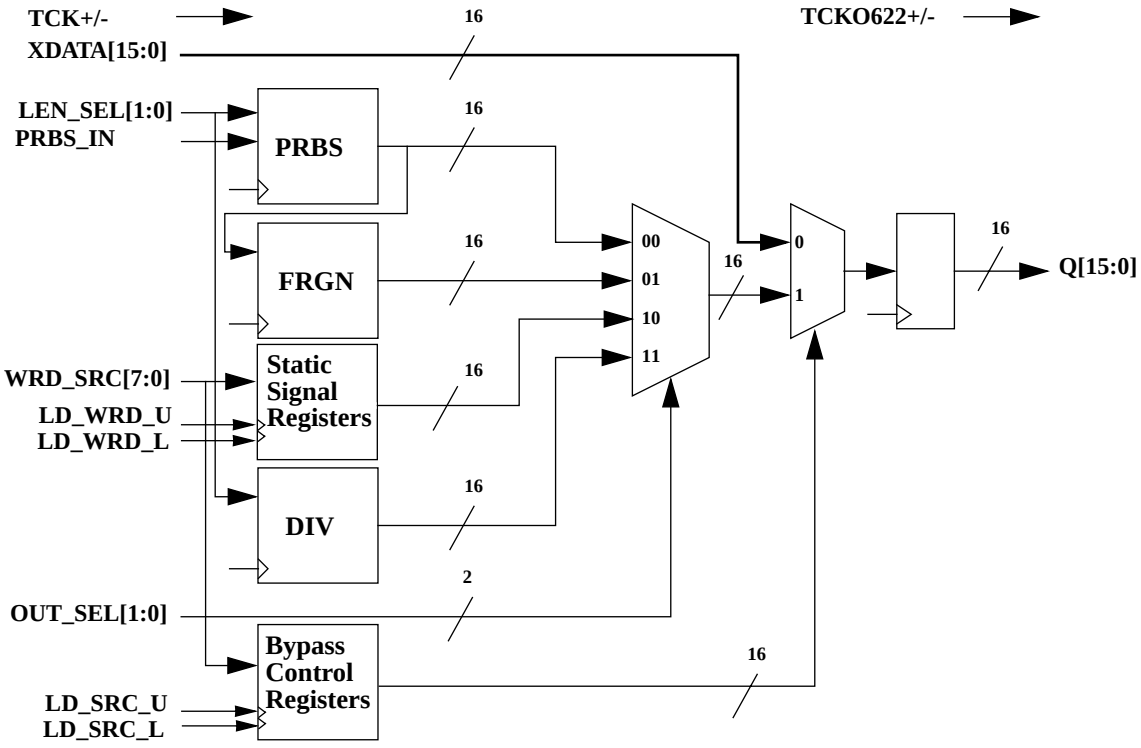
- Multiple Length PRBS Generator With Adjustable Mark Ratios
- PRBS Error Detector and 16-bit Accumulator
- 155/622 Mb/s 16 bit ECL I/O Interface
- STS-192/STM-64 Selectable Frame Insertion
- 16 Bit Static and Selectable Divider Output
- Bitwise External Data Bypass Mode

General Description

The VSC8109 incorporates a PRBS transmitter and receiver in order to construct 2.5 and 10 Gb/s test systems. The transmitter generates a 16 channel 155/622 Mbit/sec PRBS pattern and can be connected to a multiplexer to generate up to a 10 Gbit/sec serial bit pattern. The device outputs random sequence lengths from 2^7-1 to 2^{31}-1 with an adjustable mark ratio. The receiver includes a PRBS comparator and error detection circuitry that detects any errors in the demultiplexed PRBS pattern allowing the user to calculate a bit error rate.

The transmitter and receiver can be used separately, allowing testing of a transmission system with VSC8109 devices in different locations.

VSC8109 Functional Block Diagram (Transmitter)



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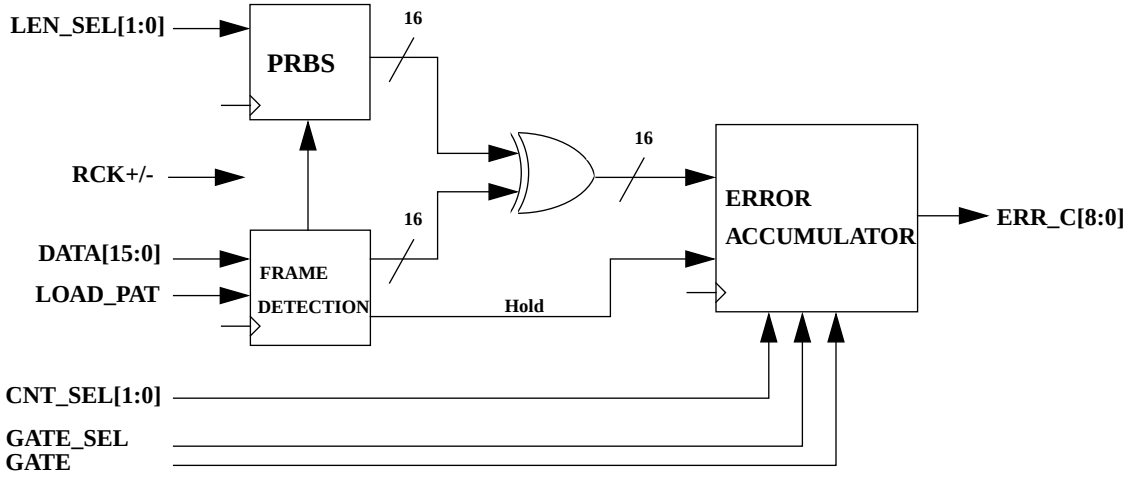
VSC8109 Functional Block Diagram (Receiver)



Transmitter Functional Description

The VSC8109 transmitter has four internal operating modes plus a bypass mode. When the bypass mode is selected, the XDATA[15:0] is pipelined 3 TCK+/- clock cycles inside the chip before it appears on the output, but is otherwise unchanged. The four internal modes are selected using OUT_SEL[1:0] (See Table 1).

Table 1: Internal Modes.

Internal Mode	*OUT_SEL[1]*	*OUT_SEL[0]*
PRBS Mode	0	0
PRBS With Frame Mode	0	1
Static Signal Mode	1	0
Square Wave Generation Mode	1	1

Each of the Q[15:0] output channels can independently select XDATA or one of the four internal modes. These settings are configured by using the bypass control register. The WRD_SRC[7:0] data bus is set to the desired functionality and latched into the registers controlling the output mux. This is done with a clock pulse on the LD_SRC_U and LD_SRC_L inputs. LD_SRC_U sets channels Q[15:8] and LD_SRC_L sets channels Q[7:0]. A logic '1' in a particular bit position forces that output to transmit pipelined XDATA, a logic '0' selects an internal transmitter signal.

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PRBS Mode

This mode generates a PRBS pattern of a selectable length determined by LEN_SEL[1:0] (See Table 2). The options are 2^7-1, 2^{15}-1, 2^{23}-1 and 2^{31}-1, indicating the number of clock cycles required for the pattern to repeat itself. The output signal PRBS_SYNC is a pulse generated in the end of each full pattern cycle.

Table 2: PRBS Options and Polynomials

Mode	*LEN_SEL[1]*	*LEN_SEL[0]*	*Generation Polynomial*
2^7-1	0	0	$1 + X^6 + X^7$
2^{15}-1	0	1	$1 + X^{14} + X^{15}$
2^{23}-1	1	0	$1 + X^{18} + X^{23}$
2^{31}-1	1	1	$1 + X^{28} + X^{31}$

PRBS_IN initializes the transmit PRBS generator. The value of PRBS_IN must always be ‘0’ except during initialization of the PRBS, when PRBS_IN must be logic ‘1’ for at least 32 TCK+/- clock cycles before it returns to ‘0’ again. The LOAD_PAT signal works in the same manner to initialize the receiver side. Other PRBS signals are described in the Signal Interface section.(See Table 5)

PRBS with Frame Mode

This mode is similar to the standard PRBS mode, with the exception that a STS-192/STM-64 frame is inserted- the A1 and A2 bytes replace an equal number of bytes in the PRBS sequence. The receiver detects these frame bits as non-PRBS, and does not treat them as bit-errors. The error counter is set to hold mode until the PRBS sequence continues.

Static Signal Mode

The VSC8109 can place a static output pattern on each of the 16 channels. The static signal register is programmed in the same way as the bypass control register. The WRD_SRC[7:0] data bus is set to the desired output word and latched into registers driving the internal mode selector. This is done with a clock pulse on the LD_WRD_U and LD_WRD_L inputs. LD_WRD_U maps to channels Q[15:8] and LD_WRD_L maps to channels Q[7:0]. This is not a bit error rate calculation mode.

Square Wave Generation Mode

This mode generates a square wave output with selectable frequency (See Table 3). The square wave signal is output simultaneously on all 16 output channels. This is not a bit error rate calculation mode.

Table 3: Square Wave Rates

Frequency	*LEN_SEL[1]*	*LEN_SEL[0]*
TCKP/2	0	0
TCKP/4	0	1
TCKP/8	1	0
TCKP/16	1	1

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Table 4: Transmitter and Common Signals.

Signal Name	*Width*	*Direction*	*Description*
FR_INV	1	Input	Inverts frame bits.
FRAME_SYNC	1	Output	Indicator for frame sync.
INV	1	Input	Inverts output.
LD_SRC_L †	1	Input	Latches WRD_SRC data to output mux select for Q[7:0].
LD_SRC_U †	1	Input	Latches WRD_SRC data to output mux select for Q[15:8].
LD_WRD_L †	1	Input	Latches WRD_SRC data to static signal registers for Q[7:0].
LD_WRD_U †	1	Input	Latches WRD_SRC data to static signal registers for q[15:8].
LEN_SEL[1:0]	2	Input	Selects PRBS length and square wave frequency.
MR	1	Input	Master Reset (Active high)
OUT_SEL[1:0]	2	Input	Selects transmit mode.
PRBS_IN	1	Input	PRBS initiating signal (Active high)
PRBS_SYNC	1	Output	Indicator that shows when full PRBS pattern cycle is performed.
Q[15:0]	16	Output	16 channel 622Mb/s output.
RAT	1	Input	Changes the mark ratio.
TCK+/-	2	Input	Transmitter differential clock input.
TCKO622+/-	2	Output	Differential clock output.
WRD_SRC[7:0]	8	Input	Data bus input for mux/static signals.
XDATA[15:0]	16	Input	External data inputs.

Note: † Data is latched on the rising edge.

Receiver Functional Description

The receiver is synchronized to the incoming PRBS signal with the signal LOAD_PAT. This signal must be held ‘1’ for at least 32 clock RCK +/- clock cycles before returning to default ‘0’. This allows the receiver to synchronize the compare PRBS generator to the incoming signal by sampling an error-free 32 bit piece. The receiver synchronization process is not affected by crossing a word boundary due to de-serialization, as long as the bit order is not changed. Following synchronization, the incoming data is compared with the contents of the receive PRBS and differences are reported as errors. The control signals INV, RAT, FR_INV etc. are shared between the transmitter and the receiver, and in applications where multiple VSC8109 devices are being used they should be set identically.

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PRBS Mode

The normal PRBS mode is initialized with LOAD_PAT as described above. Each bit is treated as one error, i.e. if three bits in one word have the wrong value, the counter will count it as three distinct errors rather than just one error per word.

PRBS with Frame Mode

If PRBS with frame mode is used, the frame detector indentifies the frame and puts the Error Accumulator on hold. The frame bits A1 and A2 are replacing the PRBS bits, the VSC8109 would normally treat these frame bits as errors in the PRBS stream. The hold signal is released as soon as the PRBS pattern returns.

Static Signal Mode and Square Wave Generation Mode

These modes are not supported by the error detection unit.

Error Detection Unit

The error detection unit counts the total number of errors in all 16 channels. The result is stored in a 16 bit counter where bit 15 is the MSB and bit 0 is the LSB.. This counter can be selected on the output ERR_C[8:0] using the control signal CNT_SEL[1:0]. The bit ERR_C[8] is an active high overflow bit that indicates error overflow in the selected 8-bit output register. There are two error counter modes:

Synchronous Counter Mode

The synchronous counter is updated every RCK +/- clock cycle.. The content of bit [15:8] or bit [7:0] can be selected to appear on the output ERR_C[8:0] using CNT_SEL[1:0]. (See table 5)

Gated Counter Mode

The outputs of the synchronous counter will change unpredictably and will make design of robust off-chip parallel read logic difficult. The contents of the synchronous counter can be sampled and stored in readout registers by use of a slower gating signal, either internally or externally provided. If internal gate mode is chosen, (GATE_SEL = ‘1’), the VSC8109 will generate the gate signal itself every 2^{30} RCK +/- clock cycle. If external gate mode is selected (GATE_SEL = ‘0’) the result from the synchronous counter is stored in the gated counter when the GATE signal is sampled by at least one RCK +/-clock cycle. (The GATE signal should always be zero otherwise) The synchronous counter is reset each time a gated counter is loaded regardless if internal or external gate mode is used. This allows the gated counter to display the number of bit errors that occurred since the previous gate sample. Note that there is a six clock cycle delay before the stored data in the B-counter is visible on the ERR_C output if external gate is used and GATE = ‘1’.

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Table 5: CNT_SEL[1:0] Functionality

ERR_C[7:0]	*CNT_SEL[1]*	*CNT_SEL[0]*
Synchronous Counter [15:8]	0	0
Synchronous Counter [7:0]	0	1
Gated Counter [15:8]	1	0
Gated Counter [7:0]	1	1

Table 6: Receiver Signals.

Signal Name	*Width*	*Direction*	*Description*
CNT_SEL[1:0]	2	Input	Counter output selection.
DATA[15:0]	16	Input	16 channel 622 Mb/s input.
ERR_C[8:0]	9	Output	Eight bit error counter output plus overflow bit.
GATE	1	Input	External counter gate input.
GATE_SEL	1	Input	Gate select signal. 0: Use internal gate signal. 1: Use external gate signal
LOAD_PAT	1	Input	PRBS receiver initiating signal.
RCK+/-	1	Input	Input differential clock for receiver side.

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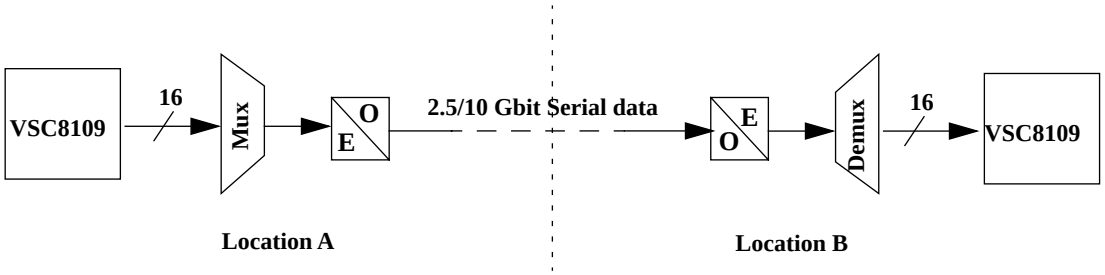
System Implementation

VSC8109 can be used in a number of different ways. Below are some suggestions of how to implement VSC8109 with the transmission system.

VSC8109 Suggested System Implementation

Suggestion 1:



Suggestion 2:

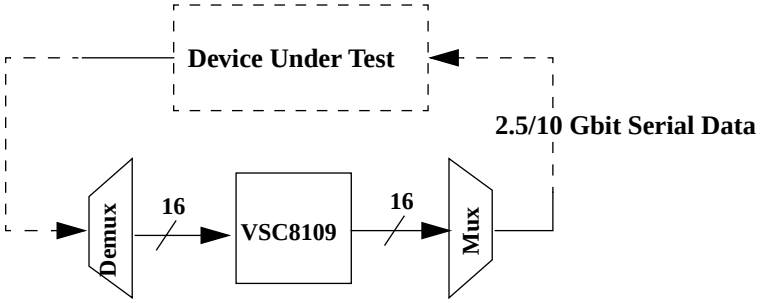


Table 7: Vitesse Part Numbers for Selected System Rates

System Frequency	*Multiplexer*	*Demultiplexer*
2.5 GHz	VSC8061	VSC8062
10 Ghz	VSC8071	VSC8072

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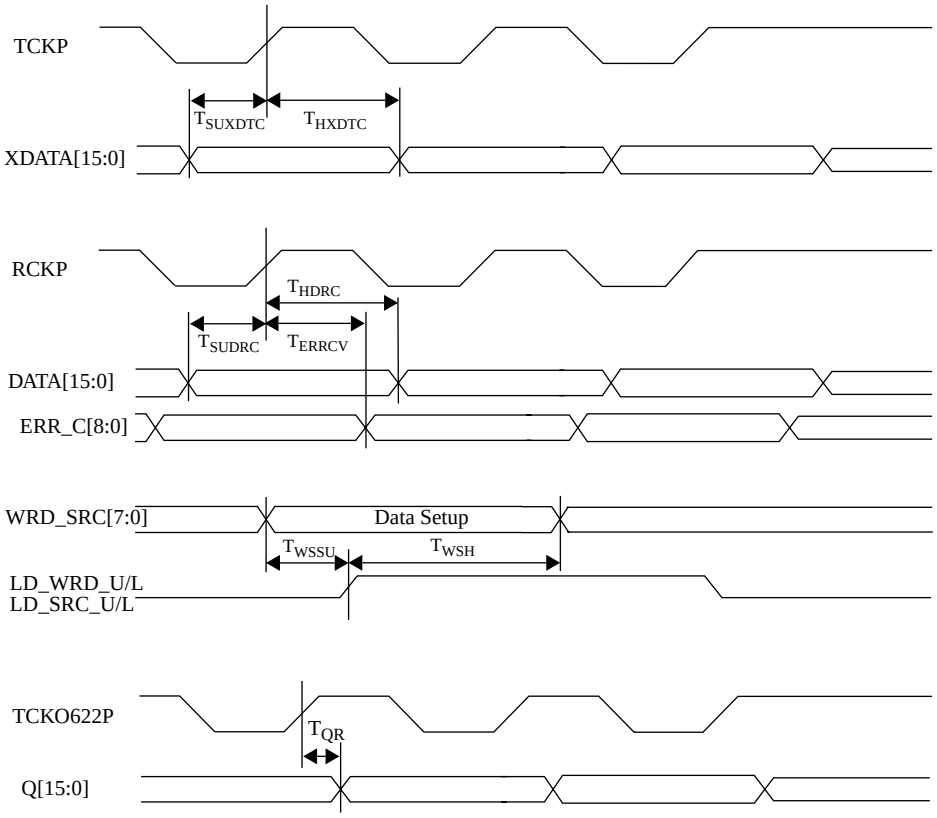
AC Timing Characteristics

Table 8: AC Timing Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{SUXDTC}	XDATA input setup time with respect to TCKP	0.55	—	—	ns
T_{HXDTC}	XDATA input hold time with respect to TCKP	0	—	—	ns
T_{SUDRC}	DATA input setup time with respect to RCKP	0.10	—	—	ns
T_{HDRC}	DATA input hold time with respect to RCKP	0.45	—	—	ns
T_{ERRCV}	ERR_C output delay with respect to RCKP	1.47	—	—	ns
T_{WSSU}	WRD_SRC input setup time with respect to LD_WRD_U/L and LD_SRC_U/L	0.25	—	—	ns
T_{WSH}	WRD_SRC input hold time with respect to LD_WRD_U/L and LD_SRC_U/L	0.5	—	—	ns
T_{QR}	Q[15:0] output delay with respect to TCKOP622 +/-	0.04	—	0.28	ns

Note: Generated Waveforms are synchronous and assume a 155.5 or 622MHz TCKP/N signal.

Figure 1: Signals Setup and Hold Time



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DC Characteristics

Table 9: Single Ended ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	
V_{IH}	Input HIGH voltage	-1165	-	-700	mV	
V_{IL}	Input LOW voltage	-2000	-	-1475	mV	
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN} = V_{IL}$ (min)

Table 10: Differential ECL Input and Output Ratings

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{DIFFIN}	Input Voltage Differential	200	-	-	mV	Required for full output swing
$V_{DIFFOUT}$	Output Voltage Differential	600		1300	mV	
V_{CM}	Common mode voltage	-1500	-	-500	mV	Common mode range required for full output swing with V_{DIFFIN} applied.
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-		uA	$V_{IN} = V_{IL}$ (min)

Table 11: Power Supply Currents (-2.1V Supply, Outputs Open)

Parameter	Description	(Max)	Units
I_{TT}	Power supply current from V_{TT}	2950	mA
P_D	Power dissipation	6.2	W

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Absolute Maximum Ratings

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltages (V_{TT}) ..... -2.0V ±5 %
Commercial Operating Temperature Range (T) ..... 0° to 70°C

Notes: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.
(2) Customer must use air cooled/heatsink environment to meet thermal requirements of the package.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8109 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Description

Table 12: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
VCC	1	PWR	GND	
TEST	2	O	N/C	Test Output
TEST	3	O	N/C	Test Output
VCC	4	PWR	GND	
VCC	5	PWR	GND	
IO	6	N/C	N/C	
IO	7	N/C	N/C	
VCC	8	PWR	GND	
IO	9	N/C	N/C	
IO	10	N/C	N/C	
VTT	11	PWR	-2V	
DATA15	12	I	ECL	Data Input Bus
DATA14	13	I	ECL	Data Input Bus
VCC	14	PWR	GND	
DATA13	15	I	ECL	Data Input Bus
DATA12	16	I	ECL	Data Input Bus
VCC	17	PWR	GND	
DATA11	18	I	ECL	Data Input Bus
DATA10	19	I	ECL	Data Input Bus
VTT	20	PWR	-2V	
DATA9	21	I	ECL	Data Input Bus
DATA8	22	I	ECL	Data Input Bus
VCC	23	PWR	GND	
DATA7	24	I	ECL	Data Input Bus
DATA6	25	I	ECL	Data Input Bus
VCC	26	PWR	GND	
VCC	27	PWR	GND	
DATA5	28	I	ECL	Data Input Bus
DATA4	29	I	ECL	Data Input Bus
VCC	30	PWR	GND	
DATA3	31	I	ECL	Data Input Bus
DATA2	32	I	ECL	Data Input Bus
VTT	33	PWR	-2V	
DATA1	34	I	ECL	Data Input Bus
DATA0	35	I	ECL	Data Input Bus
VCC	36	PWR	GND	

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Table 12: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
IO	37	N/C	N/C	
IO	38	N/C	N/C	
VCC	39	PWR	GND	
RCKN	40	I	ECL	Receiver Clock Input
RCKP	41	I	ECL	Receiver Clock Input
VTT	42	PWR	-2V	
IO	43	N/C	N/C	
IO	44	N/C	N/C	
VCC	45	PWR	GND	
IO	46	N/C	N/C	
IO	47	N/C	N/C	
VCC	48	PWR	GND	
VCC	49	PWR	GND	
IO	50	N/C	N/C	
ERR_C8	51	O	ECL	Error Counter Output Bus
VCC	52	PWR	GND	
IS	53	N/C	N/C	
IS	54	N/C	N/C	
IS	55	N/C	N/C	
IS	56	N/C	N/C	
IS	57	N/C	N/C	
IS	58	N/C	N/C	
VCC	59	PWR	GND	
VSCIPNC	60	I	ECL	
VSCOPNC	61	O	ECL	
VTT	62	PWR	-2V	
ERR_C7	63	O	ECL	Error Counter Output Bus
ERR_C6	64	O	ECL	Error Counter Output Bus
VCC	65	PWR	GND	
ERR_C5	66	O	ECL	Error Counter Output Bus
ERR_C4	67	O	ECL	Error Counter Output Bus
VCC	68	PWR	GND	
VCC	69	PWR	GND	
ERR_C3	70	O	ECL	Error Counter Output Bus
ERR_C2	71	O	ECL	Error Counter Output Bus
VTT	72	PWR	-2V	
ERR_C1	73	O	ECL	Error Counter Output Bus
ERR_C0	74	O	ECL	Error Counter Output Bus

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Table 12: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	75	PWR	GND	
I	76	N/C	N/C	
I	77	N/C	N/C	
VCC	78	PWR	GND	
VCC	79	PWR	GND	
I	80	N/C	N/C	
I	81	N/C	N/C	
VCC	82	PWR	GND	
XDATA0	83	I	ECL	External Data Input Bus
XDATA1	84	I	ECL	External Data Input Bus
VTT	85	PWR	-2V	
XDATA2	86	I	ECL	External Data Input Bus
XDATA3	87	I	ECL	External Data Input Bus
VCC	88	PWR	GND	
VCC	89	PWR	GND	
XDATA4	90	I	ECL	External Data Input Bus
XDATA5	91	I	ECL	External Data Input Bus
VCC	92	PWR	GND	
XDATA6	93	I	ECL	External Data Input Bus
XDATA7	94	I	ECL	External Data Input Bus
VTT	95	PWR	-2V	
XDATA8	96	I	ECL	External Data Input Bus
XDATA9	97	I	ECL	External Data Input Bus
VCC	98	PWR	GND	
XDATA10	99	I	ECL	External Data Input Bus
XDATA11	100	I	ECL	External Data Input Bus
XDATA12	101	I	ECL	External Data Input Bus
XDATA13	102	I	ECL	External Data Input Bus
XDATA14	103	I	ECL	External Data Input Bus
XDATA15	104	I	ECL	External Data Input Bus
VCC	105	PWR	GND	
IO	106	N/C	N/C	
IO	107	N/C	N/C	
VCC	108	PWR	GND	
VCC	109	PWR	GND	
IO	110	N/C	N/C	
IO	111	N/C	N/C	
VCC	112	PWR	GND	

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Table 12: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
TCKO622N	113	O	ECL	Transmitter Clock Output
TCKO622P	114	O	ECL	Transmitter Clock Output
VTT	115	PWR	-2V	
IO	116	N/C	N/C	
IO	117	N/C	N/C	
VCC	118	PWR	GND	
Q0	119	O	ECL	Data Output Bus
Q1	120	O	ECL	Data Output Bus
VCC	121	PWR	GND	
Q2	122	O	ECL	Data Output Bus
Q3	123	O	ECL	Data Output Bus
VTT	124	PWR	-2V	
Q4	125	O	ECL	Data Output Bus
Q5	126	O	ECL	Data Output Bus
VCC	127	PWR	GND	
Q6	128	O	ECL	Data Output Bus
Q7	129	O	ECL	Data Output Bus
VCC	130	PWR	GND	
VCC	131	PWR	GND	
Q8	132	O	ECL	Data Output Bus
Q9	133	O	ECL	Data Output Bus
VCC	134	PWR	GND	
Q10	135	O	ECL	Data Output Bus
Q11	136	O	ECL	Data Output Bus
VTT	137	PWR	-2V	
Q12	138	O	ECL	Data Output Bus
Q13	139	O	ECL	Data Output Bus
VCC	140	PWR	GND	
Q14	141	O	ECL	Data Output Bus
Q15	142	O	ECL	Data Output Bus
VCC	143	PWR	GND	
IO	144	N/C	N/C	
IO	145	N/C	N/C	
VTT	146	PWR	-2V	
TCKN	147	I	ECL	Transmitter Clock Input
TCKP	148	I	ECL	Transmitter Clock Input
VCC	149	PWR	GND	
IO	150	N/C	N/C	

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Table 12: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
IO	151	N/C	N/C	
VCC	152	PWR	GND	
VCC	153	PWR	GND	
FR_SYNC	154	O	ECL	Frame Sync Output Signal
PRBS_SYNC	155	O	ECL	PRBS Sync Output Signal
VCC	156	PWR	GND	
WRD_SRC0	157	I	ECL	Outmux/Static signal Bus
WRD_SRC1	158	I	ECL	Outmux/Static signal Bus
WRD_SRC2	159	I	ECL	Outmux/Static signal Bus
WRD_SRC3	160	I	ECL	Outmux/Static signal Bus
WRD_SRC4	161	I	ECL	Outmux/Static signal Bus
WRD_SRC5	162	I	ECL	Outmux/Static signal Bus
VCC	163	PWR	GND	
WRD_SRC6	164	I	ECL	Outmux/Static signal Bus
WRD_SRC7	165	I	ECL	Outmux/Static signal Bus
VTT	166	PWR	-2V	
LD_WRD_L	167	I	ECL	
LD_WRD_U	168	I	ECL	
VCC	169	PWR	GND	
LD_SRC_L	170	I	ECL	
LD_SRC_U	171	I	ECL	
VCC	172	PWR	GND	
VCC	173	PWR	GND	
OUT_SEL0	174	I	ECL	Output Select Signal
OUT_SEL1	175	I	ECL	Output Select Signal
VTT	176	PWR	-2V	
TEST	177	I	GND	Test Input
TEST	178	I	GND	Test Input
VCC	179	PWR	GND	
I	180	N/C	N/C	
I	181	N/C	N/C	
VCC	182	PWR	GND	
VCC	183	PWR	GND	
VREF	184	REFPWR	-1.32V	
I	185	N/C	N/C	
VCC	186	PWR	GND	
VSCTE	187	I	-2.0	
IO	188	N/C	N/C	

Table 12: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VTT	189	PWR	-2V	
PRBS_IN	190	I	ECL	PRBS Transmitter Init
RAT	191	I	ECL	1/0 Ratio selector
VCC	192	PWR	GND	
VCC	193	PWR	GND	
LEN_SEL0	194	I	ECL	Length Select Signal
LEN_SEL1	195	I	ECL	Length Select Signal
VCC	196	PWR	GND	
MR	197	I	ECL	Master Reset
FR_INV	198	I	ECL	Frame Invert Signal
VTT	199	PWR	-2V	
INV	200	I	ECL	Output Invert Signal
IS	201	N/C	N/C	
VCC	202	PWR	GND	
LOAD_PAT	203	I	ECL	PRBS Receiver Init
TEST	204	I	VTT	Test Input
GATE	205	I	ECL	External Gate Signal
GATE_SEL	206	I	ECL	External/Internal Gate
CNT_SEL0	207	I	ECL	Error Counter Output Sel.
CNT_SEL1	208	I	ECL	Error Counter Output Sel.

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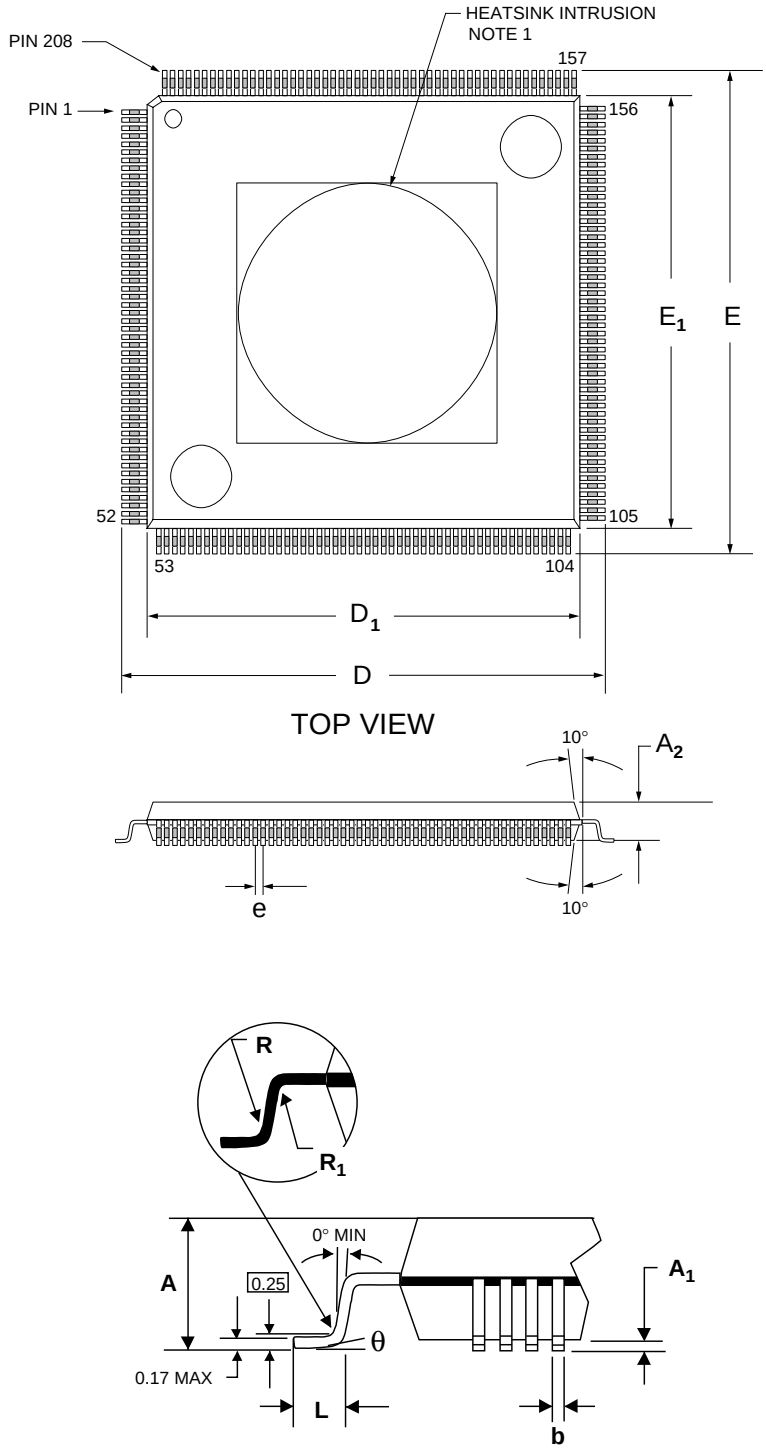
Package Information



208 PQFP Package Dimensions

Key	*mm*	*Tolerance*
A	4.10	MAX
A1	0.25	MIN
A2	3.49	±0.10
D	30.60	±0.20
D1	28,00	±0.10
E	30.60	±0.20
E1	28.00	±0.10
L	0.60	+.15/–.10
e	0.50	BASIC
b	0.22	±0.05
θ	0-7°	
R	.15	TYP
R1	.25	MAX

Notes:
(1) Exposed Heatspreader will be either 20.32 ± .50 round or 12.0 ± .50 square
(2) Drawing not to scale
Package #101-228-6, Issue #1

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Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8109 **QG**

Device Type
VSC8109:
155/622 16-bit PRBS Generator and Comparator

Package
QG: 208 PQFP, 28mm Body

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

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