## Advance Product Information

# VSC6280/81/82

*125MHz Octal Deskew*

## Features

- Eight Adjustable Delay Lines in One Package
- Independent Delay Adjustments for Positive and Negative Going Transitions
- Fanout Mode and Edge Mode Features Through Mask Programming
- Up to 8ns of Delay with <10 psec LSB Resolution
- 750 ps Minimum Pulse Width
- 125 MHz Bandwidth
- Fully Digital. No Off-chip DACs Required
- No Sensitive Analog Reference Voltages for Improved Crosstalk Performance.
- Dual Supply Operation -2, +3.3V
- 128 PQFP Package

## Functional Description

The VSC6280, VSC6281, and VSC6282 are adjustable digital delay lines designed for high-precision delay adjustment of high frequency ECL signals. They are designed specifically for de-skewing multiple drive side channels on a shared resource ATE system. They integrate fully digital delay lines eliminating the requirement for off-chip components such as DAC's, trim resistors and compensation capacitors. The three devices use a novel design to provide maximum timing stability and minimum part-to-part delay variation resulting in maximum usable range in the de-skew of multiple timing paths.

Two delay adjustments are available for each channel, Delay_R and Delay_F. These delay values independently adjust the rising-edge and falling edge of a pulse, respectively. Delay values are serially loaded into a Calibration Register via the Serial Data Input during system calibration. In addition there are 16 11-bit Data Latches for the 16 Delay Elements. ADR[3:0] determines which of the 16 Data latches is loaded from the Calibration Register. The Delay Registers hold an 11-bit word. This Delay value determines the $TPD_{SPAN}$ of the Variable Delay Element. The resolution of the Delay Element is 10ps.

### Configurational Description

The VSC6280, VSC6281, and VSC6282 configurations are mask programmable as selected by the user, and described in the block diagrams, shown as Figure 1, 2, and 3. Table 1 below provides further specifications and operability for each part number.

**Table 1: VSC6280/81/82 Configurations**

| *Part No.* | *Description* | *Edge/Pulse Mode* |
|---|---|---|
| VSC6280 | Standard Configuration: 8 Input and 8 Output | Pulse |
| VSC6281 | Edge Configuration: 16 Input and 16 Output | Edge |
| VSC6282 | Fanout Configuration: 1 Input and 8 Output | Pulse |

*Note: Edge mode delays rising or falling edges. Pulse mode delays both rising and falling pulse edges independently.*




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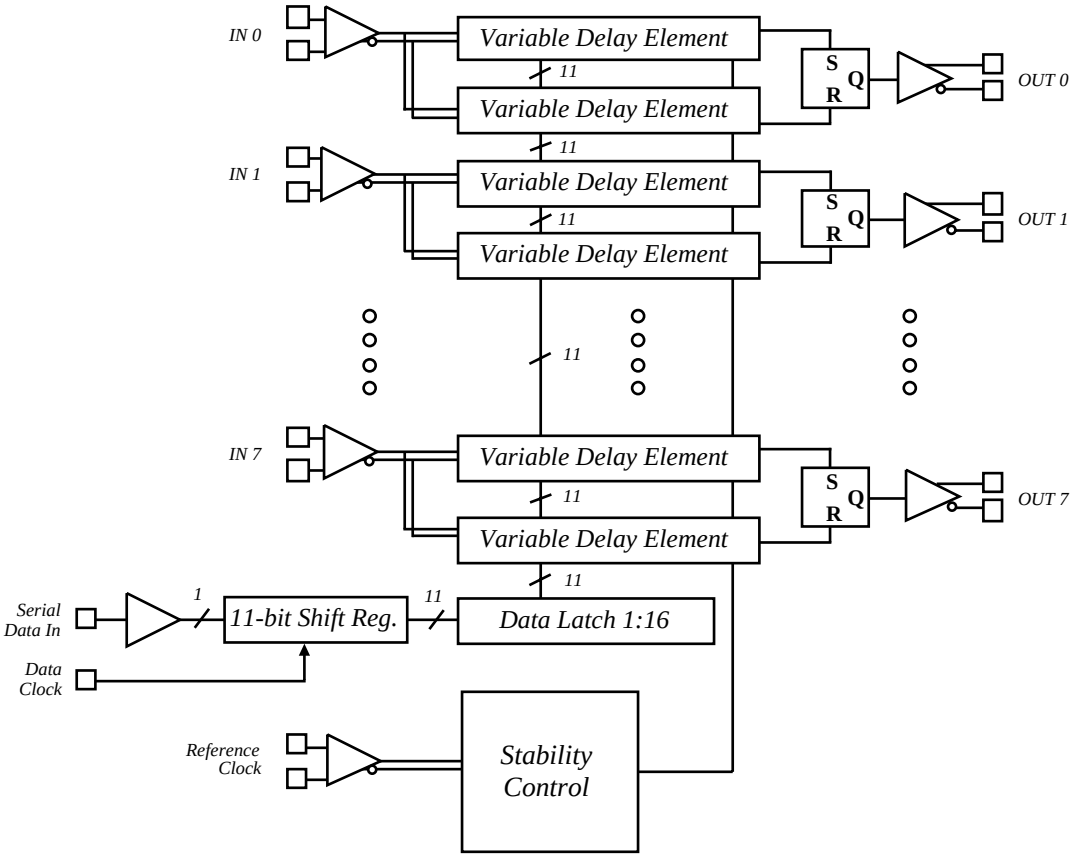
**Figure 1: VSC6280 Block Diagram - 8 In and 8 Out: Pulse Mode**




***Eight Channels: Delays both edges of a pulse. Delay adjustment of edges is independent.***



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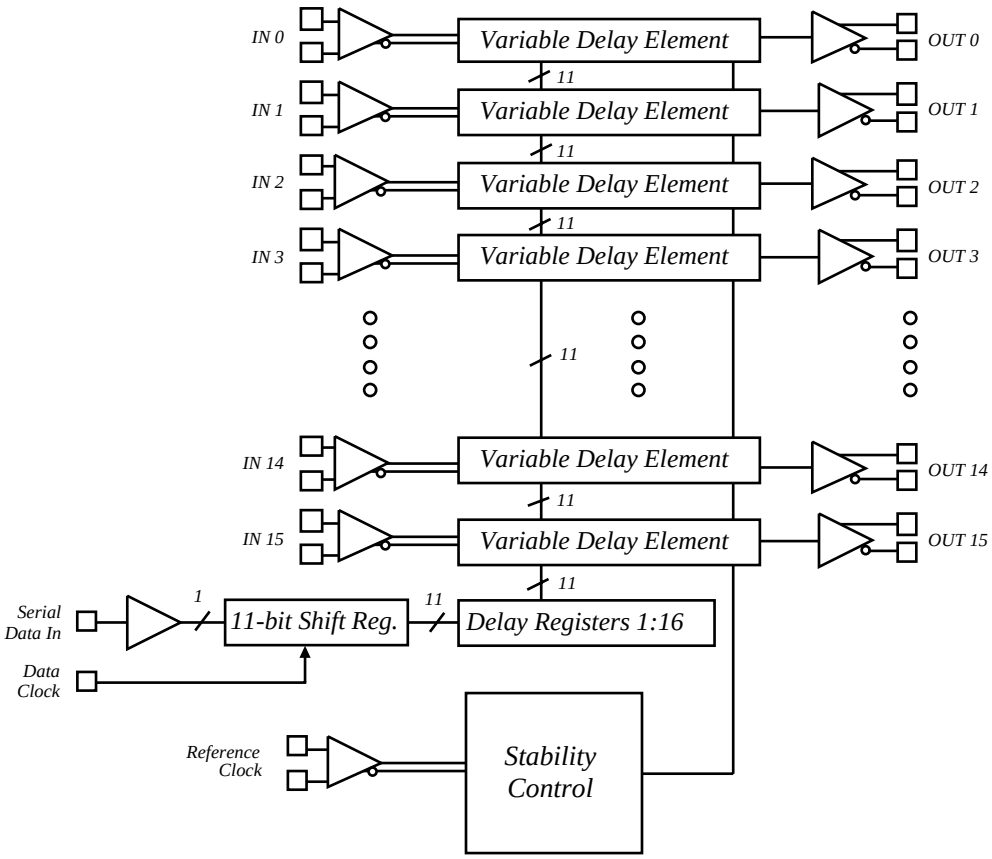
**Figure 2: VSC6281 Block Diagram - 16 In and 16 Out: Edge Mode**




***Sixteen channels (rise or fall). Each channel is delayed independently.***




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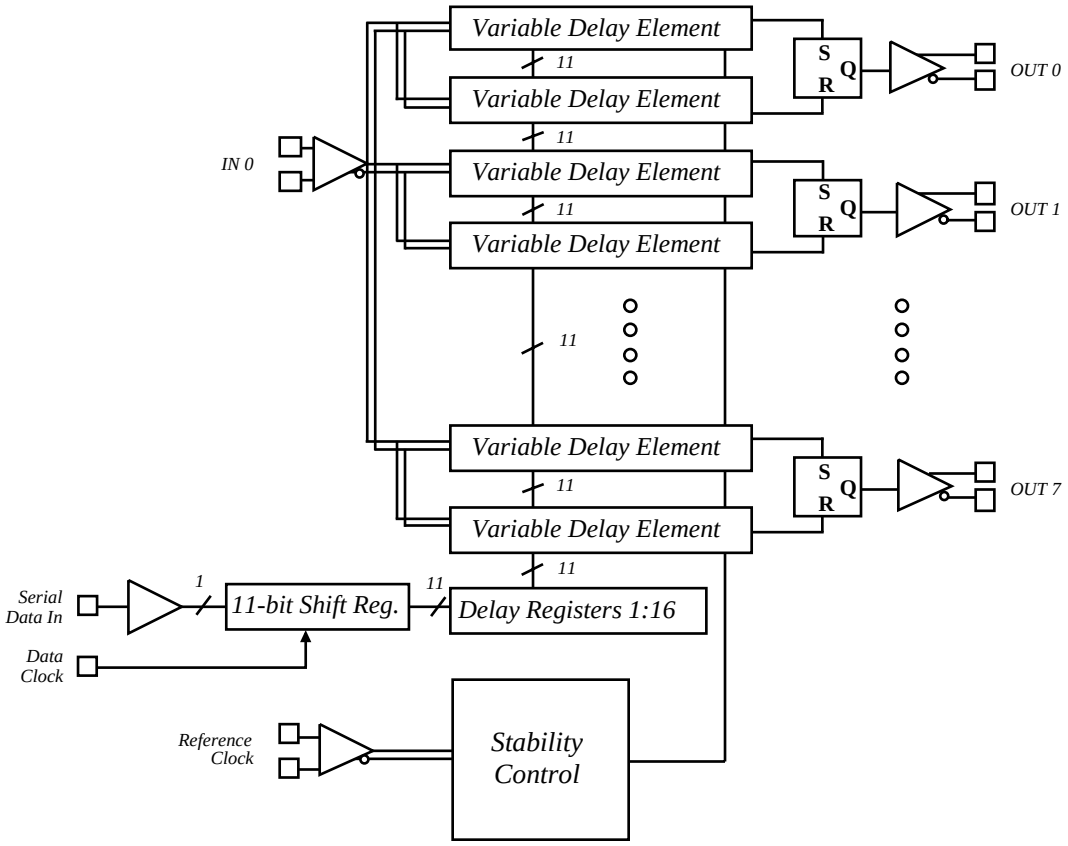
**Figure 3: VSC6282 Block Diagram - 1 In and 8 Out: Fan Out Mode**




***One input channel fanned out to eight output channels. Delays both edges of a pulse. Delay adjustment of edges is independent.***



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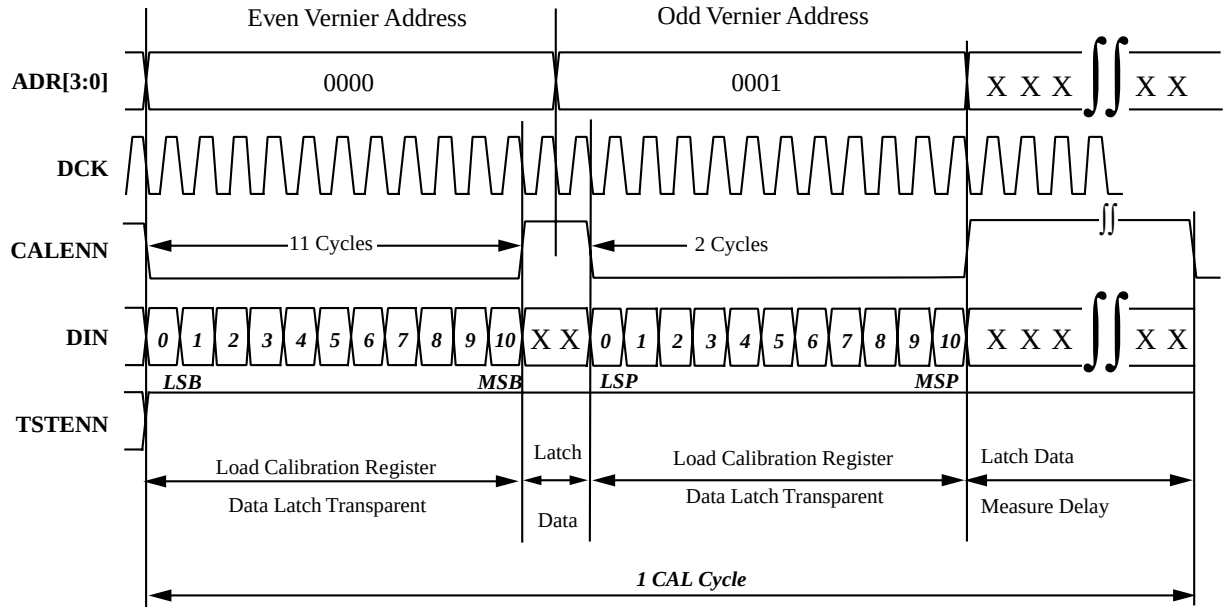
## Operational Mode Truth Table

| Mode No | Mode Name | TSTENN | CALENN | Mode Description |
|---|---|---|---|---|
| 1 | Test Mode T | 0 | 0 | Measure vernier delays. Write data to data latches - Transparent Mode. (Ring Oscillator Test) |
| 2 | Test Mode L | 0 | 1 | Measure vernier delay using latched data - Latched Mode. (Ring Oscillator Test) |
| 3 | Cal. Mode | 1 | 0 | Set timing delays with each vernier selected with ADR [3:0] Serial Data Input. |
| 4 | User Mode | 1 | 1 | Generate timing delays as set by data in Cal Mode. |

**Figure 4: CAL Mode Timing Diagram**




*Note:*

*TEST Mode Timing: Use CAL Mode Timing Diagram with TSTENN LO during CAL cycle. The TEST Mode places the verniers in ring oscillator operation.*



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**Figure 5: CAL Mode. Pre-Calibration Delay Range**
**7 Coarse Vernier Steps + 31 Fine Vernier Steps**

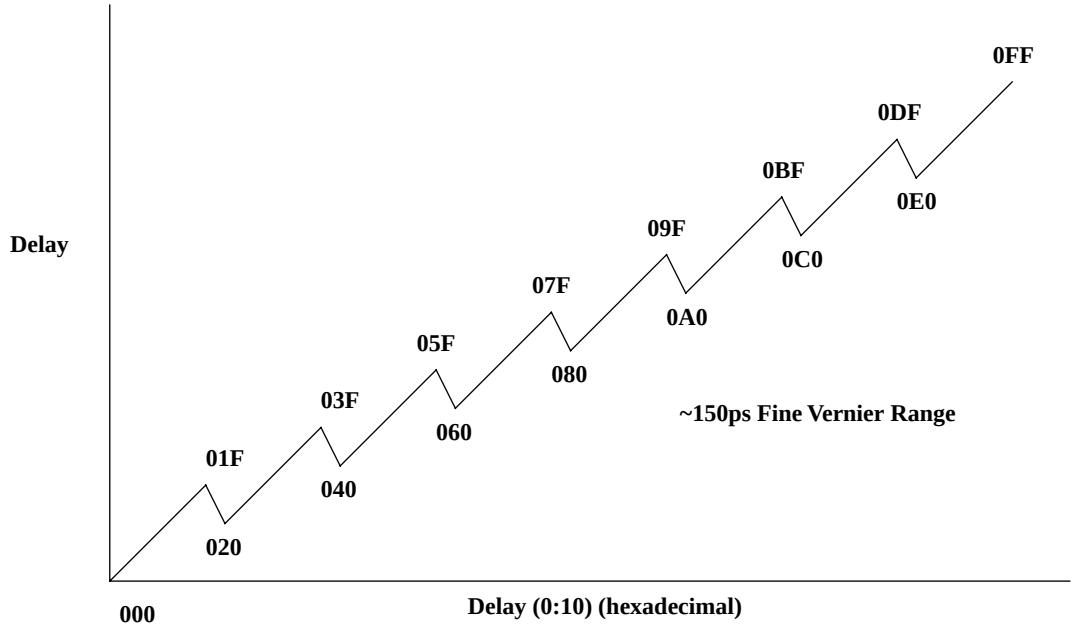
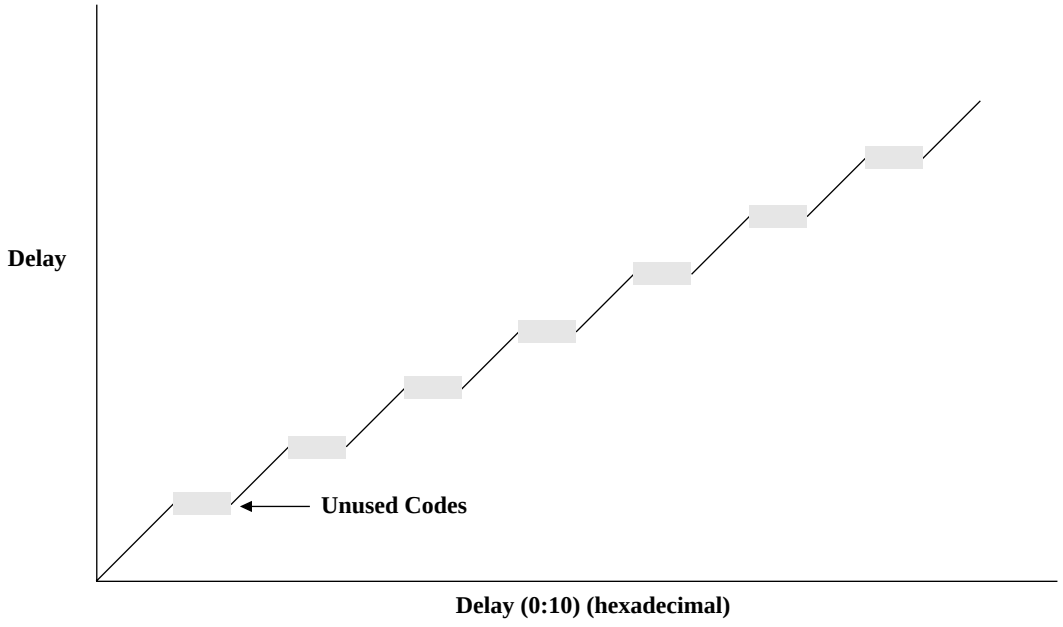



**Figure 6: CAL Mode. Post-Calibration Delay Range**
**7 Coarse Vernier Steps + 31 Fine Vernier Steps**



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## AC Timing Characteristics

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* |
|---|---|---|---|---|---|
| $TPD_{MIN}$ | Propagation Delays<br>Zero Delay (00000000000)<br>See Figure 7 | 2.5 | | 3.7 | ns |
| $TPDR_{SPAN}$(1) | Propagation Delays<br>Max Delay (11111111111)<br>See Figure 7 | 7.7 | | 8.3 | ns |
| $TPDF_{SPAN}$(1) | Propagation Delays<br>Max Delay (11111111111)<br>See Figure 7 | 7.7 | | 8.3 | ns |
| $T_{RES}$ | Variable Delay Element Resolution LSB | | 6 | 10 | ps |
| DNL | Variable Delay Element Differential Nonlinearity (Maximum Hole Size) | | | 20 | ps |
| TPWI | Input Pulse Width | 750 | | | ps |
| TPWO | Output Pulse Width | 750 | | | ps |
| $f_{RCK}$ | Reference Clock Frequency | | 62.5 | | MHz |
| $D_{TPD}$ | Variation in Delay Versus Pulse Width (TPW > 750 ps) | | ±20 | | ps |
| DCV | Variation in Delay Versus Duty Cycle and Frequency | | | ±40 | ps |
| $D_{TCO}$ | Variation in Delay vs Temperature | 6 | | 10 | ps/C° |
| $P_{SRR}$ | Power Supply Rejection Ratio | 9 | | 15 | ps/100mV |
| $T_R/T_F$ | Output Rise Fall Times (20% to 80%) | 200 | | 400 | ps |
| $T_{REFIRE}$ | Adjacent Edge Spacing. See Figure 8. | $TPD_{SPAN}$ +2ns | | | ns |

*Note: 1) $TPD_{SPAN} \leq T_{REFIRE}$ - 2ns. See Figure 8*

.

**Figure 7: AC Timing Diagram**

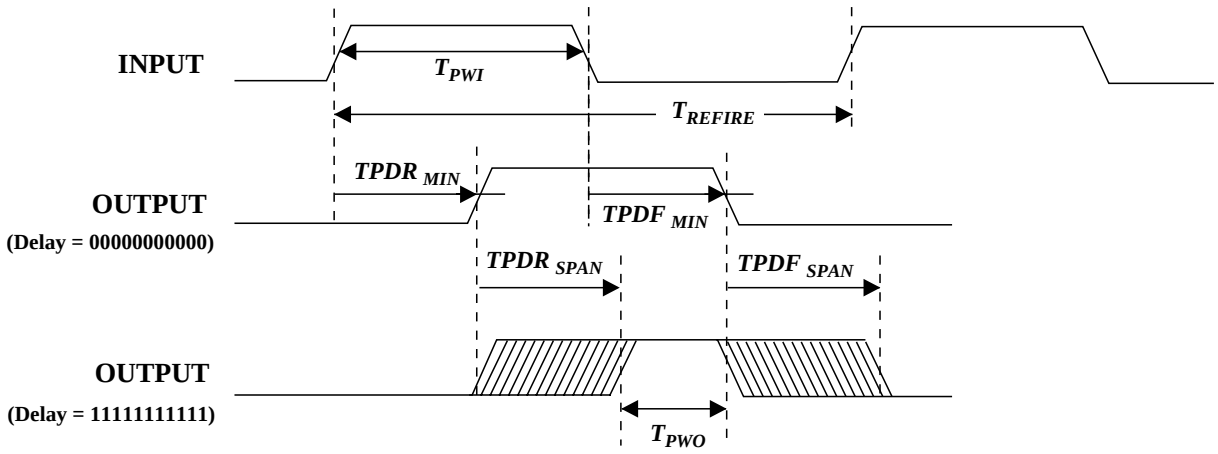





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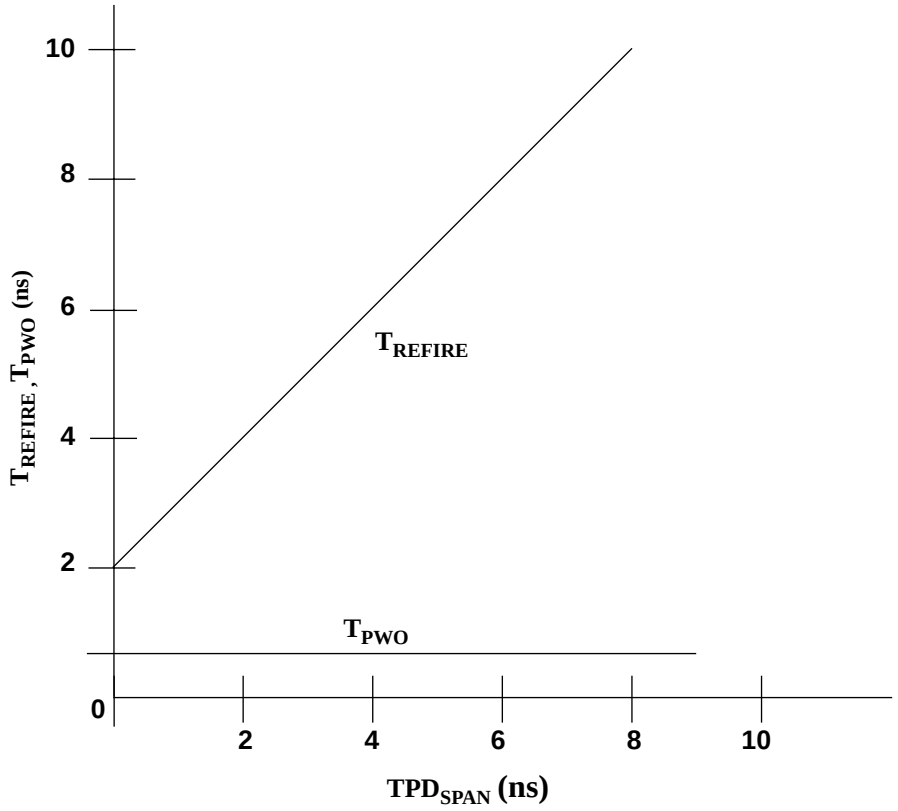
**Figure 8: Refire Rate and Pulse Width vs. Span**




## *DC Characteristics*

**Table 2: Single Ended ECL Inputs and Outputs**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | -1020 | - | -700 | mV | |
| $V_{OL}$ | Output LOW voltage | -2000 | - | -1620 | mV | |
| $V_{IH}$ | Input HIGH voltage | -1165 | - | -700 | mV | |
| $V_{IL}$ | Input LOW voltage | -2000 | - | -1475 | mV | |
| $I_{IH}$ | Input HIGH current | - | - | 200 | uA | $V_{IN} = V_{IH}$ (max) |
| $I_{IL}$ | Input LOW current | -50 | - | - | uA | $V_{IN} = V_{IL}$ (min) |

*Note: $V_{TT}$ = -2.0V ± 5%, $V_{CC} = V_{CCA}$ = GND, Load = 50 to -2.0V, External Reference ($V_{REF}$) = -1.32V ± 25 mV.*



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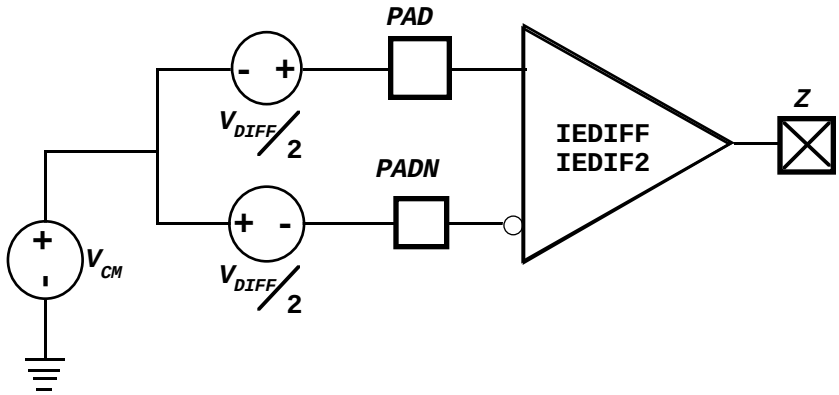
### Table 3: Differential ECL Inputs and Outputs

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{DIFF}$ | Input Voltage Differential | 200[1] | - | - | mV | Required for full output swing |
| $V_{CM}$ | Common Mode Voltage | -1.5 | - | -0.5 | V | Common mode range required for full output swing with $V_{DIFF}$ applied |

*Note (1): For input signals >500 MHz $V_{DIFF}$ must be 600mV.*

### Figure 9: Differential ECL Input Voltages




### Table 4: TTL Inputs and Outputs

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | 2.4 | - | - | V | $I_{OH}$ = -2.4mA |
| $V_{OL}$ | Output LOW voltage | 0 | - | 0.4 | V | $I_{OL}$ = 16 mA |
| $V_{IH}$ | Input HIGH voltage | 2.0 | - | $V_{TTL}$+1.0V | V | - |
| $V_{IL}$ | Input LOW voltage | 0 | - | 0.8 | V | - |
| $I_{IH}$ | Input HIGH current | - | - | 50 | uA | $V_{IN}$ = 2.4V |
| $I_{IL}$ | Input LOW current | -500 | - | - | uA | $V_{IN}$ = 0.4V |
| $I_{OZH}$ | 3-State Output OFF current HIGH | - | - | 200 | uA | $V_{OUT}$ = 2.4V |
| $I_{OZL}$ | 3-State Output OFF current LOW | -100 | - | - | uA | $V_{OUT}$ = 0.4V |
| $I_{OZLB}$ | 3-State Output OFF Current Low for Bi-directs | -600 | - | - | uA | $V_{OUT}$ = 0.4V |
| $I_{OCZ}$ | Open Collector Output Leakage Current | - | - | 200 | uA | $V_{OUT}$ = 2.4V |

*Note: All Specifications are over recommended commercial operating conditions, TTL/GND = GND*

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## Power Dissipation

**Table 5: Power Supply Currents**

| Device Configuration | Supply Current | Description | (Max) | Units |
|---|---|---|---|---|
| VSC6280 | $I_{TT}$ | Power supply current from $V_{TT}$ | 1500 | mA |
| | $I_{DD}$ | Power supply current from $V_{DD}$ | 1160 | mA |
| | $I_{TTL}$ | Power supply current from $V_{TTL}$ | 10 | mA |
| VSC6281 | $I_{TT}$ | Power supply current from $V_{TT}$ | 1800 | mA |
| | $I_{DD}$ | Power supply current from $V_{DD}$ | 1160 | mA |
| | $I_{TTL}$ | Power supply current from $V_{TTL}$ | 10 | mA |
| VSC6282 | $I_{TT}$ | Power supply current from $V_{TT}$ | 1400 | mA |
| | $I_{DD}$ | Power supply current from $V_{DD}$ | 1160 | mA |
| | $I_{TTL}$ | Power supply current from $V_{TTL}$ | 10 | mA |

**Table 6: Power Dissipation**

| Device Configuration | Supply Current | Description | (Max) | Units |
|---|---|---|---|---|
| VSC6280 | $P_D$ | Power dissipation | 7.5 | Watt |
| VSC6281 | $P_D$ | Power dissipation | 7.5 | Watt |
| VSC6282 | $P_D$ | Power dissipation | 7.5 | Watt |



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## Package Pin Description

**Table 7: Pin Identification**

| *Pin #* | *Signal* | *Signal Type* | *I/O Type* | *Comments* | *Pin Description* |
|---|---|---|---|---|---|
| 1 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 2 | VCC | Ground | --- | 0V | Ground |
| 3 | IN3N | I | ECL | | |
| 4 | IN3 | I | ECL | | Input Channel #3 |
| 5 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 6 | IN4N | I | ECL | | |
| 7 | IN4 | I | ECL | | Input Channel #4 |
| 8 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 9 | IN5N | I | ECL | | |
| 10 | IN5 | I | ECL | | Input Channel #5 |
| 11 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 12 | IN6N | I | ECL | | |
| 13 | IN6 | I | ECL | | Input Channel #6 |
| 14 | VCC | Ground | --- | 0V | Ground |
| 15 | IN7N | I | ECL | | |
| 16 | IN7 | I | ECL | | Input Channel #7 |
| 17 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 18 | IN8N | I | ECL | | |
| 19 | IN8 | I | ECL | | Input Channel #8 |
| 20 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 21 | IN9N | I | ECL | | |
| 22 | IN9 | I | ECL | | Input Channel #9 |
| 23 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 24 | IN10N | I | ECL | | |
| 25 | IN10 | I | ECL | | Input Channel #10 |
| 26 | VCC | Ground | --- | 0V | Ground |
| 27 | IN11N | I | ECL | | |
| 28 | IN11 | I | ECL | | Input Channel #11 |
| 29 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 30 | IN12N | I | ECL | | |
| 31 | IN12 | I | ECL | | Input Channel #12 |
| 32 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 33 | IN13 | I | ECL | | |
| 34 | IN13N | I | ECL | | Input Channel #13 |
| 35 | VCC | Ground | --- | 0V | Ground |
| 36 | IN14 | I | ECL | | |




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| *Pin #* | *Signal* | *Signal Type* | *I/O Type* | *Comments* | *Pin Description* |
|---|---|---|---|---|---|
| 37 | IN14N | I | ECL | | Input Channel #14 |
| 38 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 39 | IN15 | I | ECL | | |
| 40 | IN15N | I | ECL | | Input Channel #15 |
| 41 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 42 | ADR3 | I | TTL | | Address Bit 3 for Vernier Selection |
| 43 | ADR2 | I | TTL | | Address Bit 2 for Vernier Selection |
| 44 | ADR1 | I | TTL | | Address Bit 1 for Vernier Selection |
| 45 | ADR0 | I | TTL | | Address Bit 0 for Vernier Selection |
| 46 | CALENN | I | TTL | | Cal Mode Enable -- Active Low |
| 47 | DIN | I | TTL | | Input Serial Data for Vernier Delay |
| 48 | DCK | I | TTL | | Input Serial Data Clock |
| 49 | VTTL | Power | --- | 3.3V | TTL IO Power |
| 50 | RCK | I | ECL | | PLL Reference Clock Input |
| 51 | RCKN | I | ECL | | |
| 52 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 53 | VCC | Ground | --- | 0V | Ground |
| 54 | OUT8N | O | ECL | | |
| 55 | OUT8 | O | ECL | | Delayed Output Channel #8 |
| 56 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 57 | OUT9N | O | ECL | | |
| 58 | OUT9 | O | ECL | | Delayed Output Channel #9 |
| 59 | VCC | Ground | --- | 0V | Ground |
| 60 | OUT10N | O | ECL | | |
| 61 | OUT10 | O | ECL | | Delayed Output Channel #10 |
| 62 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 63 | OUT11N | O | ECL | | |
| 64 | OUT11 | O | ECL | | Delayed Output Channel #11 |
| 65 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 66 | NC | --- | --- | | |
| 67 | VPLL | Power | --- | 3.3V | PLL Power |
| 68 | VAGND | Ground | --- | 0V | PLL Ground |
| 69 | VCC | Ground | --- | 0V | Ground |
| 70 | OUT12N | O | ECL | | |
| 71 | OUT12 | O | ECL | | Delayed Output Channel #12 |
| 72 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 73 | OUT13N | O | ECL | | |
| 74 | OUT13 | O | ECL | | Delayed Output Channel #13 |
| 75 | VCC | Ground | --- | 0V | Ground |



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| Pin # | Signal | Signal Type | I/O Type | Comments | Pin Description |
|---|---|---|---|---|---|
| 76 | OUT14N | O | ECL | | |
| 77 | OUT14 | O | ECL | | Delayed Output Channel #14 |
| 78 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 79 | OUT15N | O | ECL | | |
| 80 | OUT15 | O | ECL | | Delayed Output Channel #15 |
| 81 | VCC | Ground | --- | 0V | Ground |
| 82 | OUT0N | O | ECL | | |
| 83 | OUT0 | O | ECL | | Delayed Output Channel #0 |
| 84 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 85 | OUT1N | O | ECL | | |
| 86 | OUT1 | O | ECL | | Delayed Output Channel #1 |
| 87 | VCC | Ground | --- | 0V | Ground |
| 88 | OUT2N | O | ECL | | |
| 89 | OUT2 | O | ECL | | Delayed Output Channel #2 |
| 90 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 91 | OUT3N | O | ECL | | |
| 92 | OUT3 | O | ECL | | Delayed Output Channel #3 |
| 93 | VCC | Ground | --- | 0V | Ground |
| 94 | NC | --- | --- | | |
| 95 | NC | --- | --- | | |
| 96 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 97 | VCC | Ground | --- | 0V | Ground |
| 98 | OUT4N | O | ECL | | |
| 99 | OUT4 | O | ECL | | Delayed Output Channel #4 |
| 100 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 101 | OUT5N | O | ECL | | |
| 102 | OUT5 | O | ECL | | Delayed Output Channel #5 |
| 103 | VCC | Ground | --- | 0V | Ground |
| 104 | OUT6N | O | ECL | | |
| 105 | OUT6 | O | ECL | | Delayed Output Channel #6 |
| 106 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 107 | OUT7N | O | ECL | | |
| 108 | OUT7 | O | ECL | | Delayed Output Channel #7 |
| 109 | TSTOUT | O | ECL | | Test Output |
| 110 | VCC | Ground | --- | 0V | Ground |
| 111 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 112 | VTTL | Power | --- | 3.3V | TTL IO Power |
| 113 | NC | --- | --- | | |
| 114 | NC | --- | --- | | |




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| Pin # | Signal | Signal Type | I/O Type | Comments | Pin Description |
|---|---|---|---|---|---|
| 115 | PTENN | I | TTL | | PLL Test Enable -- Active Low |
| 116 | TSTRST | I | TTL | | Test Mode Reset Input |
| 117 | TSTSEL | I | TTL | | Selects between Coarse/Fine Vernier |
| 118 | TSTENN | I | TTL | | Test Mode Enable -- Active Low |
| 119 | VCC | Ground | --- | 0V | Ground |
| 120 | IN0N | I | ECL | | |
| 121 | IN0 | I | ECL | | Input Channel #0 |
| 122 | VTT | Power | --- | -2V | ECL/DCFL Power |
| 123 | IN1N | I | ECL | | |
| 124 | IN1 | I | ECL | | Input Channel #1 |
| 125 | VDD | Power | --- | 3.3V | SCFL Logic Power |
| 126 | IN2N | I | ECL | | |
| 127 | IN2 | I | ECL | | Input Channel #2 |
| 128 | VCC | Ground | --- | 0V | Ground |

*Notes:*

1. *Above Pad/Pin Table is for VSC6281 which has 16 inputs and 16 outputs.*
2. *For VSC6280 only inputs IN0, IN2, IN4,IN6, IN8, IN10, IN12, IN14 and outputs OUT0, OUT2, OUT4, OUT6, OUT8, OUT10, OUT12 and OUT14 are used.*
3. *For VSC6282 only one input IN0 and outputs OUT0, OUT2, OUT4, OUT6, OUT8, OUT10, OUT12 and OUT14 are used.*
4. *In the user mode the following test inputs should be connected on the board as descri bed:*
   *TSTENN = TTL High*
   *TSTRST = TTL Low*
   *PTENN = TTL High*
   *TSTSEL = TTL Low*



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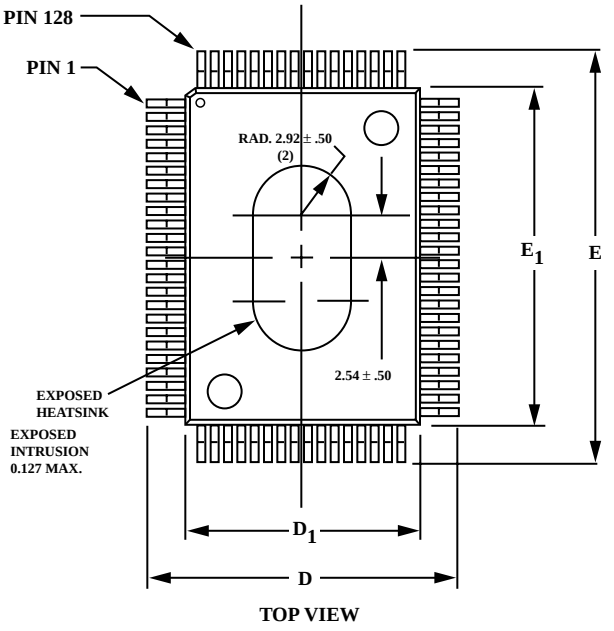
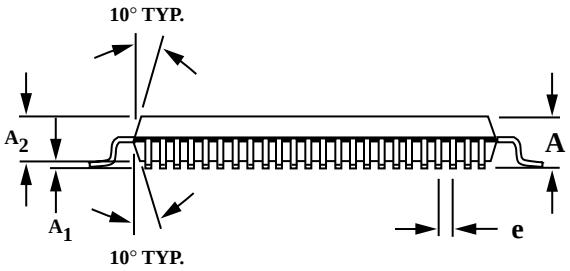
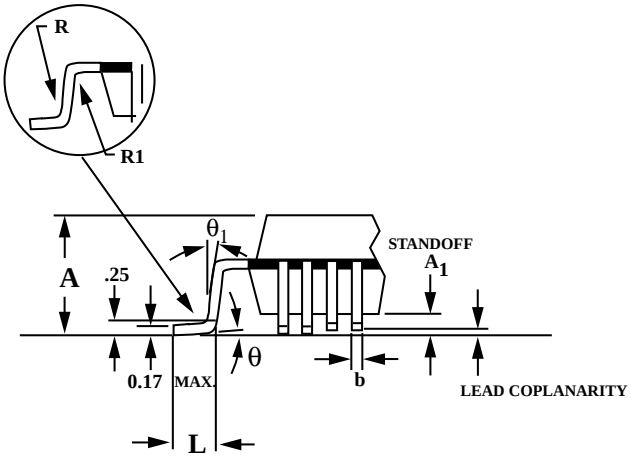
## Package Information

### 128 PQFP Package Drawings




| Key | mm | Tolerance |
|---|---|---|
| A | 3.40 | MAX |
| A1 | 0.25 | MIN |
| A2 | 2.70 | +.10 |
| D | 17.20 | ±.20 |
| D1 | 14.00 | ±.10 |
| E | 23.20 | ±.20 |
| E1 | 20.00 | ±.10 |
| L | .88 | +.15/-.10 |
| e | .50 | BASIC |
| b | .22 | ±.05 |
| θ | 0°-7° | |
| R | .30 | TYP |
| R1 | .20 | TYP |




Notes:
1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

*Package #: 101-267-7*
*Issue #: 1*

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## Absolute Maximum Ratings(1)

Power Supply Voltage ($V_{TT}$) ..... -2.5V to +0.5V
Power Supply Voltage ($V_{DD}$) ..... -0.5V to +4.3V
Power Supply Voltage ($V_{TTL}$) ..... -0.5V to +4.3V
ECL Input Voltage Applied, ($V_{IN\ ECL}$) ..... +0.5V to $V_{TT}$ + -0.5V
TTL Input Voltage Applied, ($V_{IN\ TTL}$) ..... -0.5V to $V_{TTL}$ + 1.0V
Output Current ($I_{OUT}$) ..... 50mA
Case Temperature Under Bias ($T_C$) ..... -55°C to + 125°C
Storage Temperature ($T_{STG}$) ..... -65°C to + 150°C

*Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

## Recommended Operating Conditions

Power Supply Voltage ($V_{TT}$) ..... -2.0V ± 5%
Power Supply Voltage ($V_{DD}$) ..... +3.3V ± 5%
Power Supply Voltage ($V_{TTL}$) ..... +3.3V ± 5%
Commercial Operating Temperature Range(2) ($T$) ..... 0°C to 70°C

*1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
*2) Lower limit of specification is ambient temperature and upper limit is case temperature.*

## ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC6280, VSC6281 and VSC6282 are rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

## Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

## Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.



741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896