

Table 1: Electrical Specifications

All min and max values are tested at $V_{SS} = -4.5$ and -5.5 volts unless otherwise noted. All min and max values are guaranteed from $T_{case} = 0^{\circ}\text{C}$ to 85°C unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{+/-in}^1$	Input Voltage Swing	---	---	800	mV _{p-p}	Single ended source
$V_{+in-V-in}^1$	Input Voltage Swing	---	---	1600	mV _{p-p}	Differential source
$V_{+ref.} - V_{-ref.}$	Input Offset Voltage Swing	---	10	25	mV	$V_{in} = 0$
$(V_{out+}) - (V_{out-})$	Output Voltage Swing	320	500	1200	mV _{p-p}	Differential Output Swing. $V_{in} = 8\text{mV}$, Differential Input Peak to Peak
$V_{+/- offset}$	Output DC Offset Voltage	---	-0.5	---	V	Measured to ground
PW%	Output Pulse Width	90	100	110	%	
t_r, t_f	Rise and Fall Time	---	100	---	ps	20-80%, 25°C , $V_{in} = 50\text{mV}$
G	Small Signal Gain	26	30	45	dB	$V_{in} = 4\text{mV}_{p-p}$ single ended
f_{max}^1	Small Signal -3 dB Bandwidth	---	3	---	GHz	25°C , $V_{in} = 4\text{mV}_{p-p}$
f_{min}^1	Low Frequency -3dB Cutoff	---	30	--	KHz	25°C , $V_{in} = 4\text{mV}_{p-p}$
S_{11}^1	Input Return Loss Reference to 50 ohm	---	15	--	dB	@ 1.5GHz
S_{22}^1	Output Return Loss Reference to 50 ohm	---	15	--	dB	@ 1.5GHz
I_{SS}	Supply Current	---	80	100	mA	
NF ¹	Noise Figure	---	15	--	dB	8KHz to 18 GHz
V_{nr}^1	Input Referred Wide Band Noise	---	170	--	μV_{rms}	Total single-ended output noise voltage divided by small signal gain. 8KHz to 18 GHz
R_{jc}	Thermal Resistance	---	30	--	$^{\circ}\text{C}/\text{W}$	Junction to case

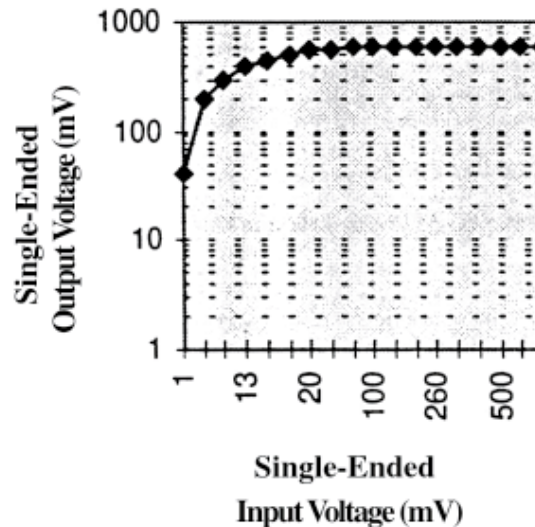
Note: (1) These values are not measured during production test. These values are results of engineering characterization

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2.5Gb/s High Speed Limiting Post Amplifier
for OC-48/SDH-16 Applications

Figure 1: Typical Output Voltage vs. Input Voltage of Limiting Amplifier



Absolute Maximum Ratings ⁽¹⁾ (at Ta = 25°C unless otherwise specified)

Power Supply Voltage, (V _{SS}):	-7V to -0.5V
Power Dissipation:	1W
All Pins:	V _{SS} to +0.5V
V + ref. -V +in:	±2V
V - ref. -V -in:	±2V
Storage Temperature Range:	-40 to 125°C
Operating Temperature Range:	0 to 100°C

Recommended Operating Conditions

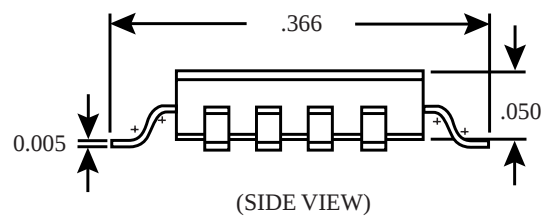
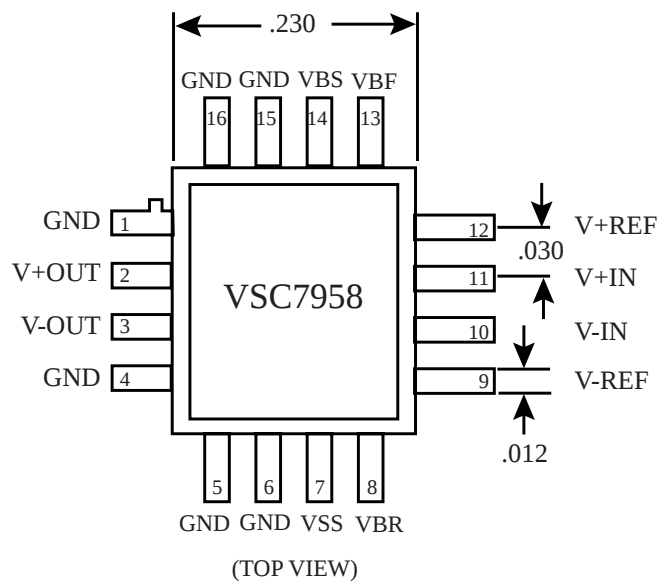
T _{case} :	0 to 85°C
V _{BR} :	-1.5V
V _{ss} :	-5.5 to -4.7V
Bit Rate = 2.488Gb/s NRZ and data pattern = 2 ²³ -1 PRBS, unless otherwise indicated	

Notes:

- (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Package Pin Descriptions

Figure 2: Pin Configuration



*All values are typical in inches

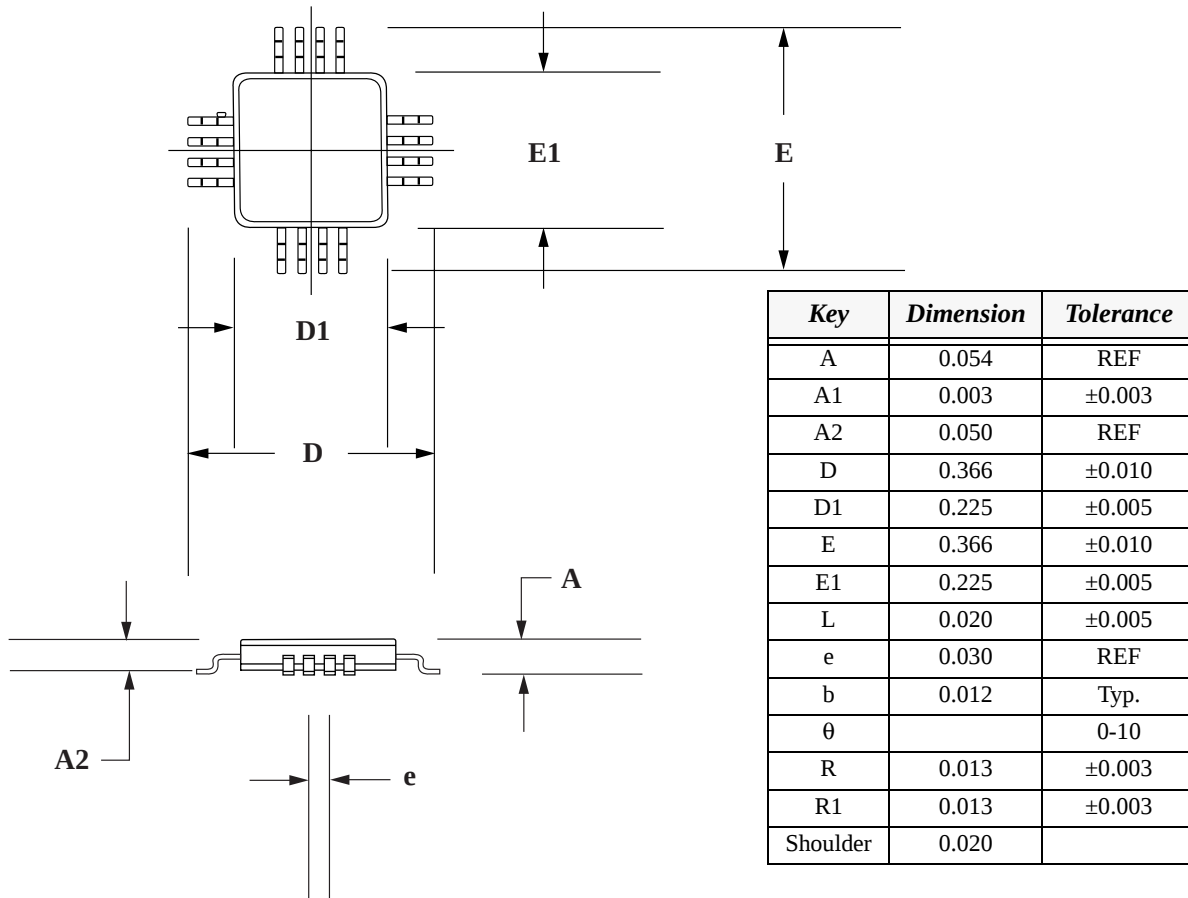
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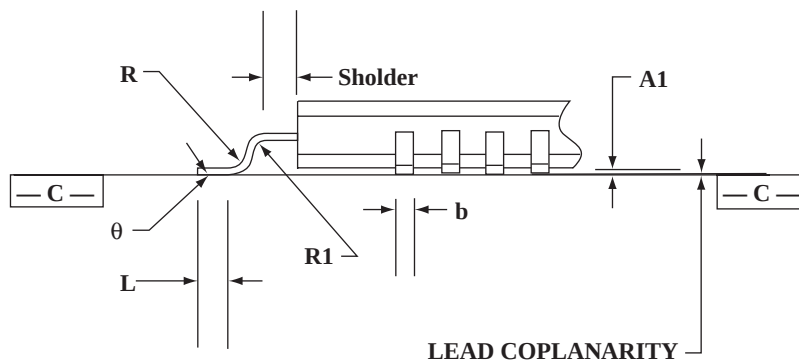
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Package Information

Figure 3: Package Dimensions



All Dimensions in inches



Die Information

Figure 4: Die Pad Information

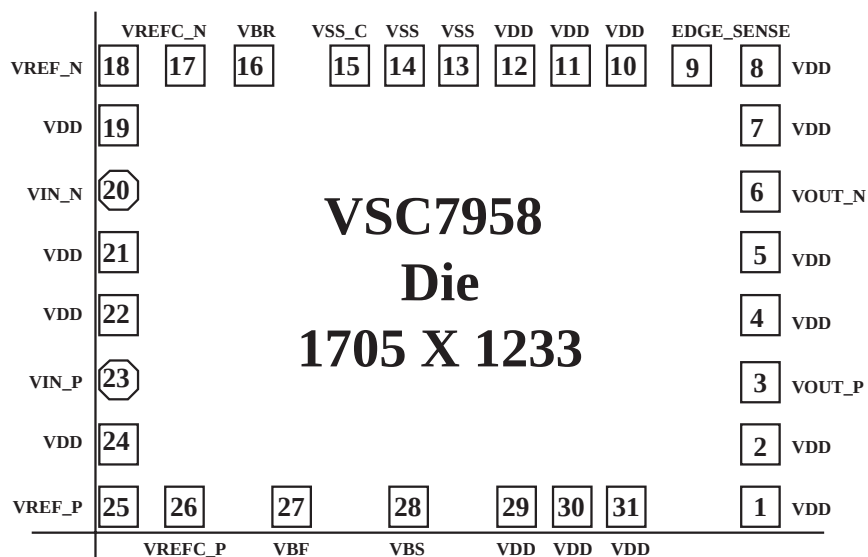


Table 2: Package Pin Identification

Pin #	Name	Function
1,4,5,6,15, 16, and bottom heat spreader	GND	DEVICE GROUND The package bottom heat spreader should be connected to ground for the optimum thermal and electrical performance.
2	V+OUT	POSITIVE DATA OUTPUT
3	V-OUT	NEGATIVE DATA OUTPUT
7	VSS	NEGATIVE DC SUPPLY
8	VBR	DEVICE REFERENCE VOLTAGE This pin can either float or be set to an external -1.5 volt supply.
9	V-REF	NEGATIVE DATA INPUT REFERENCE This pin should be bypassed to ground with a 0.1μf cap and a 5Ω series resistor.
10	V-IN	NEGATIVE DATA INPUT
11	V+IN	POSITIVE DATA INPUT

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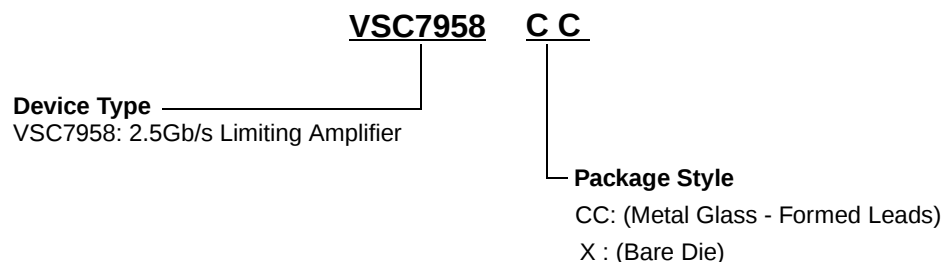
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Table 2: Package Pin Identification

Pin #	Name	Function
12	V+REF	POSITIVE DATA INPUT REFERENCE This pin should be bypassed to ground with a 0.1 μ f cap and a 5 Ω series resistor.
13	VBF	INTERNAL TEST POINT Do not connect.
14	VBS	INTERNAL TEST POINT Do not connect.

Ordering Information

The order number for this product is formed by a combination of the device number, and package style.



Notice

This document contains information about a proposed product during its design phase of development and is subject to change without notice at any time. All features and specifications are design goals only. Please contact Vitesse Semiconductor to obtain the latest product status and most recent version of this specification.

Warning

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