

Advance Product Information

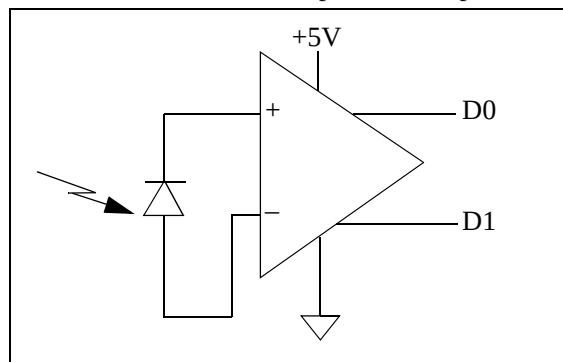
VSC7710

Photodetector/Transimpedance Amplifier
Family for Optical Communication

Features

- Integrated Photodetector/Transimpedance Amplifier Family optimized for high speed optical communications applications
- Integrated AGC
- Fibre Channel and Gigabit Ethernet
- High Bandwidth
- Low Input Noise Equivalent Power
- Single 5V Supply

Block Diagram:
Photodetector/Transimpedance Amplifier



Part Number	Data Rate (Gb/s)	Bandwidth (MHz)	Input Noise (μW rms)	Optically Active Area (μm diameter)
VSC7710	1.25	1300	.22	75

General Description

The VSC7710 integrated *p-i-n* Photodetector/Transimpedance Amplifiers provides a highly integrated solution for converting 1300 nm light from a fiber optic communications channel into a differential output voltage. The benefits of Vitesse Semiconductor's Gallium Arsenide H-GaAs-III process are fully utilized to provide a very high bandwidth and low noise amplifier. The *p-i-n* detector is 75 μm in diameter. The detector bias is supplied internally eliminating the need for a separate bias connection. The sensitivity, duty cycle distortion and jitter meet or exceed all Fibre Channel and Gigabit Ethernet application requirements. Parts are available in flat-windowed or lensed packages.

The use of a photodetector and transimpedance amplifier hybrid, reduces the input capacitance, resulting in higher sensitivity and bandwidth and improved speed of response. These parts can easily be used in developing Fibre Channel and Gigabit Ethernet electro-optic Receivers for the 900-1600 nm spectral range which exhibit very high performance and ease of use.

Table 1: Electro-Optic Specifications

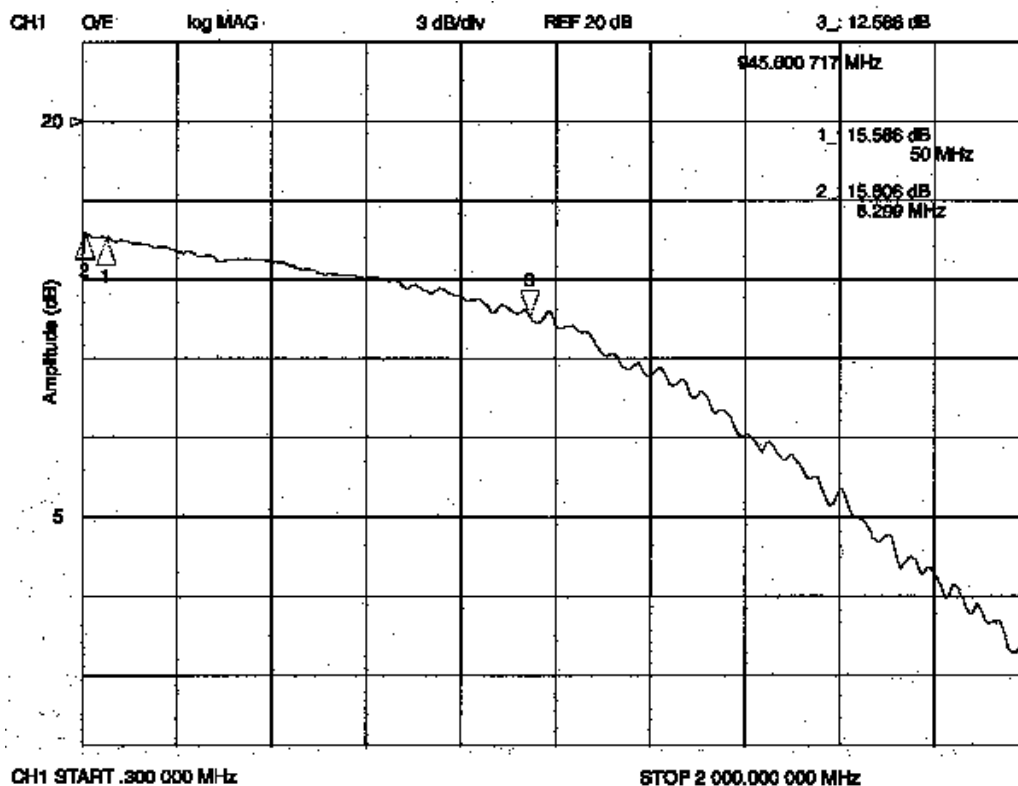
Symbol	Parameter	Min.	Max.	Units	Conditions
V _{DD}	Supply Voltage	4.5	5.5	V	
λ	Wavelength	1270	1355	nm	
f _c	Low Frequency Cutoff		1.4	MHz	-3dB P = -22dBm f _r = 50MHz
T _r T _f	Rise/Fall Time		300	ps	20% to 80% P = -3 dBm
S	Sensitivity	-28		dBm	BER 10 ⁻¹² B = 1063Mb/s
D _r	Dynamic Range	25		dB	
R _O	Single Ended Output Impedance	25	90	Ω	
V _d	Differential Output Voltage	0.25	1.2	V	P = -3 dBm, R = 100Ω
PSRR	Power Supply Rejection Ratio	35		dB	f = 0.3MHz - 40MHz Hybrid Differential
I _s	Supply Current		62	mA	P = -28 to -3 dBm
BW	Optical Modulation Bandwidth	700	1300	MHz	-3dB P = -22dBm f _r = 50MHz
R _d	Differential Responsivity	2.5		mV/μW	R _L = 100Ω P = -22dBm f _r = 50MHz
V _n	Output Noise Voltage		1.2	mV _{RMS}	BW = 1500MHz P = 0mW
NEP _O	Input Noise Equivalent Optical Power		0.22	μW RMS	BW = 1500MHz P = 0mW
PDJ	Pattern Dependent Jitter		60	ps	P = -3 dBm ± 10% Voltage Window
DCD	Duty Cycle Distortion		5	%	P = -3 dBm
ȳV	Bias Offset Voltage		200	mV	P = -3 dBm

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Figure 1: Amplitude vs. Frequency



Frequency response of VSC7710WB (Upper 3db frequency is measured with respect to response at 50 MHz)

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Limits
V _{DD}	Power Supply	6V
T _{stg}	Storage Temperature	-55°C to 125°C (case temperature under bias)
P _{inc}	Incident Optical Power	+3 dBm

Table 3: Recommended Operating Conditions

Symbol	Parameter	Limits
V _{DD}	Power Supply	4.5-5.5V (5.0V nominal)
T _{op}	Operating Temperature	0°C (ambient) to 70°C case

Table 4: Pin Table Specifications for TO-46(ball lens), TO-56 (flat window) Packages and Bare Die

Symbol	Description
D ⁺ OUT	Data output normal (with reference to incident light)
D ⁻ OUT	Data output complement (inverting) (with reference to incident light)
VDD	Power supply
GND	Ground (package case)

Note: Pin Diagram is identical for both TO-46 and TO-56 package styles.

Figure 2: Pin Diagram

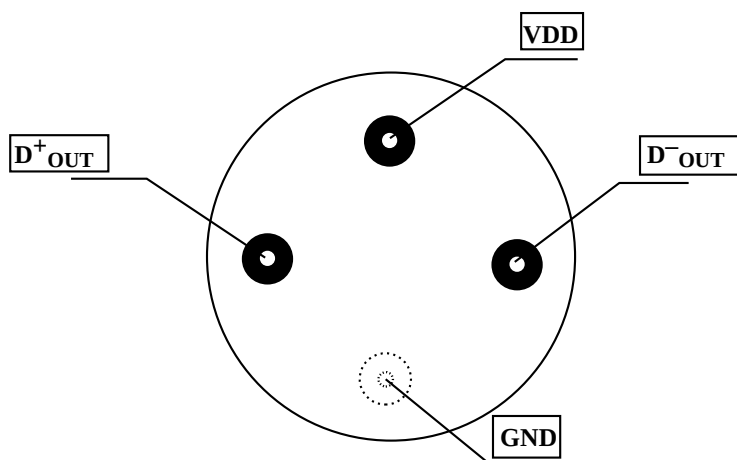
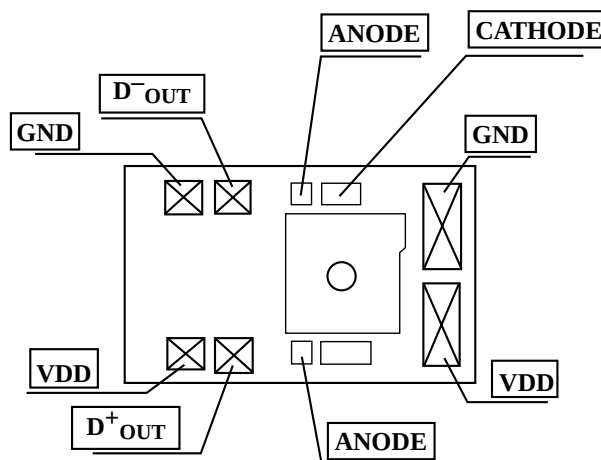


Figure 3: Schematic View of Bare Die Pad Assignments



Notes: 1) Refer to Figures 6-8 for mechanical assembly drawings for both ball lens and flat-window packages.
2) Refer to Figure 5 for die layout detail.

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Thermal Resistance Calculation

In order to relate the junction temperature to an equivalent case temperature, the following thermal characteristics of the package are provided (note that the thermal conductivity is identical for TO-46 and TO-56 package styles).

Table 5: Thermal Resistance Calculation for TO-56 and TO-46 Packages.

Chip Size	0.168cm x 0.104cm	Thermal Path Tj <

$$\theta_{\text{GaAs}} = \frac{T_{\text{die}}}{K_{\text{GaAs}}A} = \frac{0.066}{0.55 \times 0.015} = 8 \text{ }^{\circ}\text{C/W}$$

$$\theta_{\text{epoxy}} = \frac{T_{\text{epoxy}}}{K_{\text{epoxy}}A} = \frac{0.0076}{0.0186 \times 0.015} = 27.24 \text{ }^{\circ}\text{C/W}$$

$$\theta_{\text{kovar}} = \frac{T_{\text{kovar}}}{K_{\text{kovar}}A} = \frac{0.12}{0.17 \times 0.015} = 47 \text{ }^{\circ}\text{C/W}$$

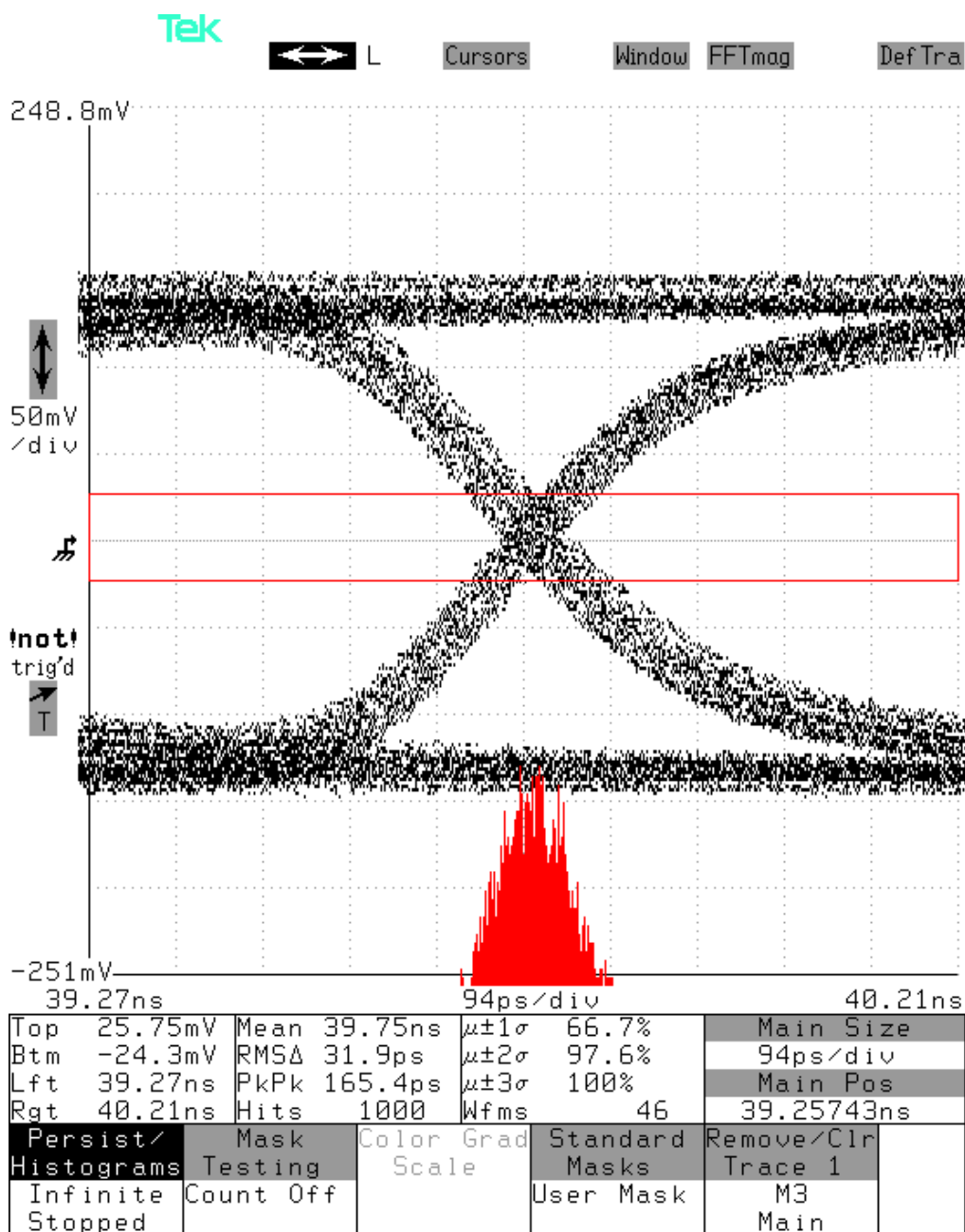
$$\theta_{\text{JC}} = \text{Thermal Resistance from Junction to Case} = (8 + 27.24 + 47) = 82.24 \text{ }^{\circ}\text{C/W}$$

Example:

For VSC7710 at nominal supply current of 25mA and V_{DD} = 5V

Temperature rise from junction to case = 0.025A x 5V x 82.24 °C/W = 10.28 °C

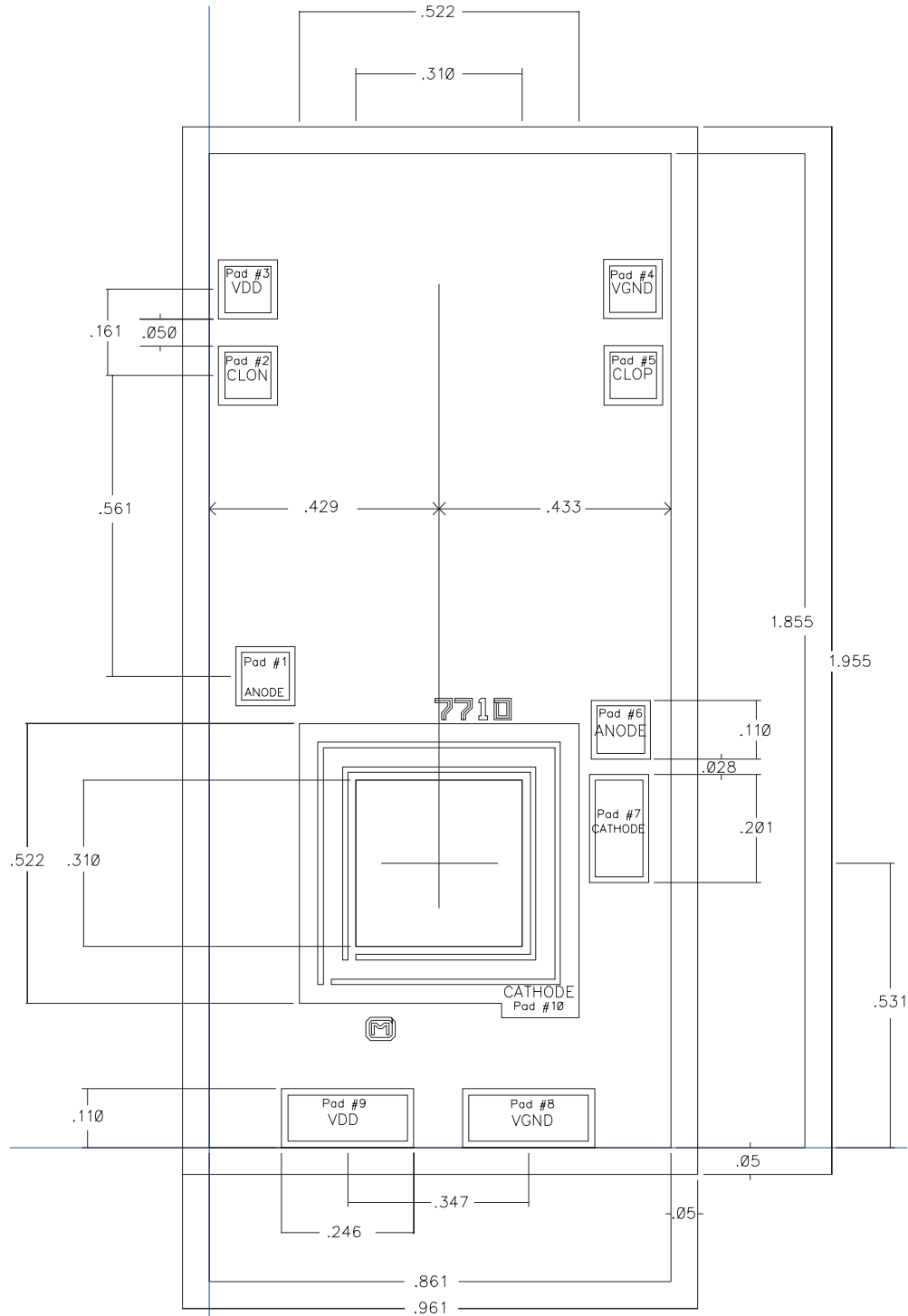
Figure 4: Eye Diagram



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Figure 5: Mechanical Specifications (Hybrid Die)



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Table 6: Die Pad Descriptions

Pad Number	Pad Name	Pad Locations		Pad Size	Pass Opening	Pad Finish	Finish Thickness
		X	Y				
1	ANODE	104.5	880	110 x 110	89 x 89	Gold	1500 Å
2	CLON	71.7	1440.6	110 x 110	89 x 89	Gold	1500 Å
3	VDD	71.7	1601.2	110 x 110	89 x 89	Gold	1500 Å
4	VGND	790	1602.1	110 x 110	89 x 89	Gold	1500 Å
5	CLOP	790	1441.1	110 x 110	89 x 89	Gold	1500 Å
6	ANODE	765.9	781.2	110 x 110	89 x 89	Gold	1500 Å
7	CATHODE	764.3	595.8	110 x 201	89 x 180	Gold	1500 Å
8	VGND	595.4	55	246 x 110	223 x 86	Gold	1500 Å
9	VDD	258	55	246 x 110	223 x 86	Gold	1500 Å
10	CATHODE	428.5	530.5	522 x 522	310 x 310	Gold	1500 Å

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Figure 6: Mechanical Package Specifications (5.6 mm Package)

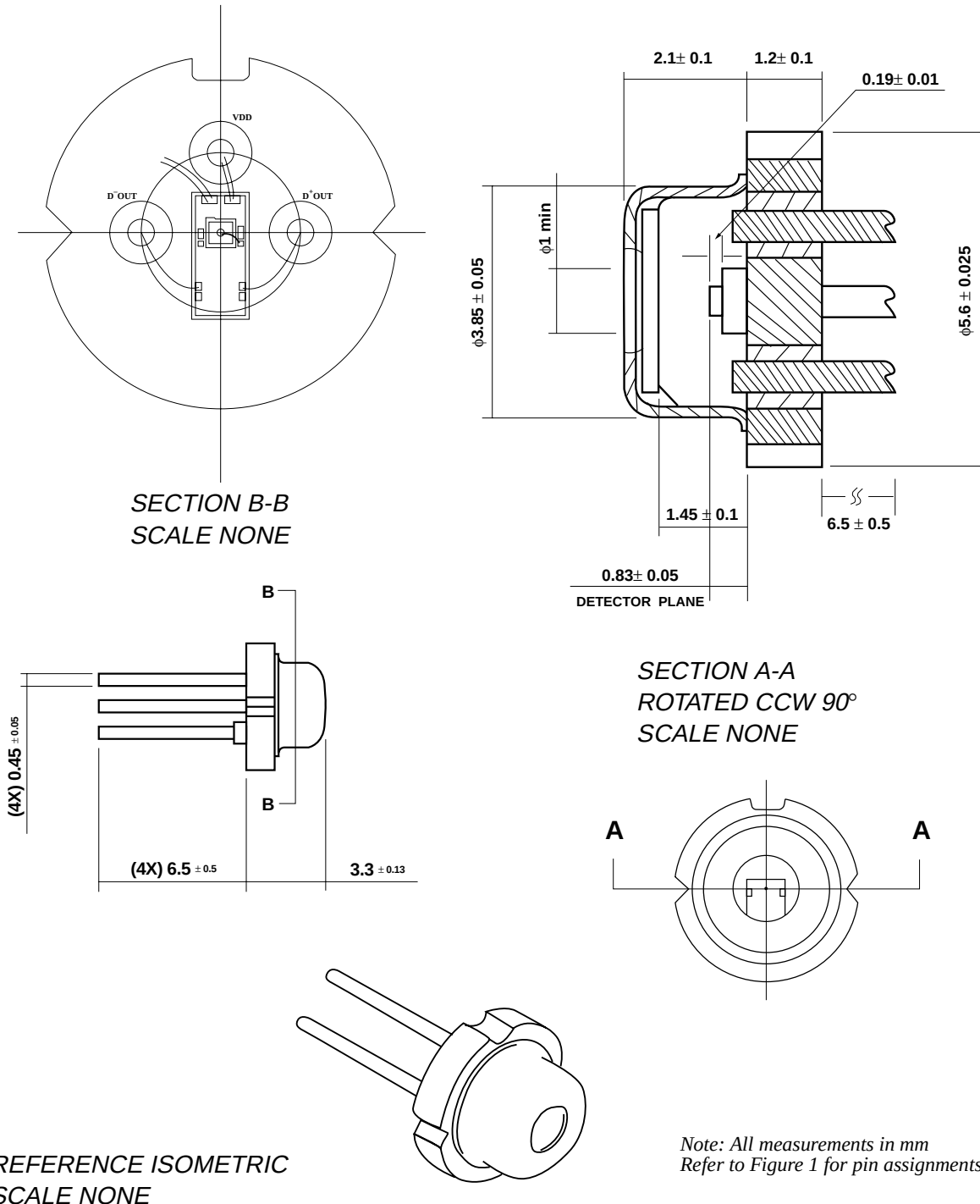
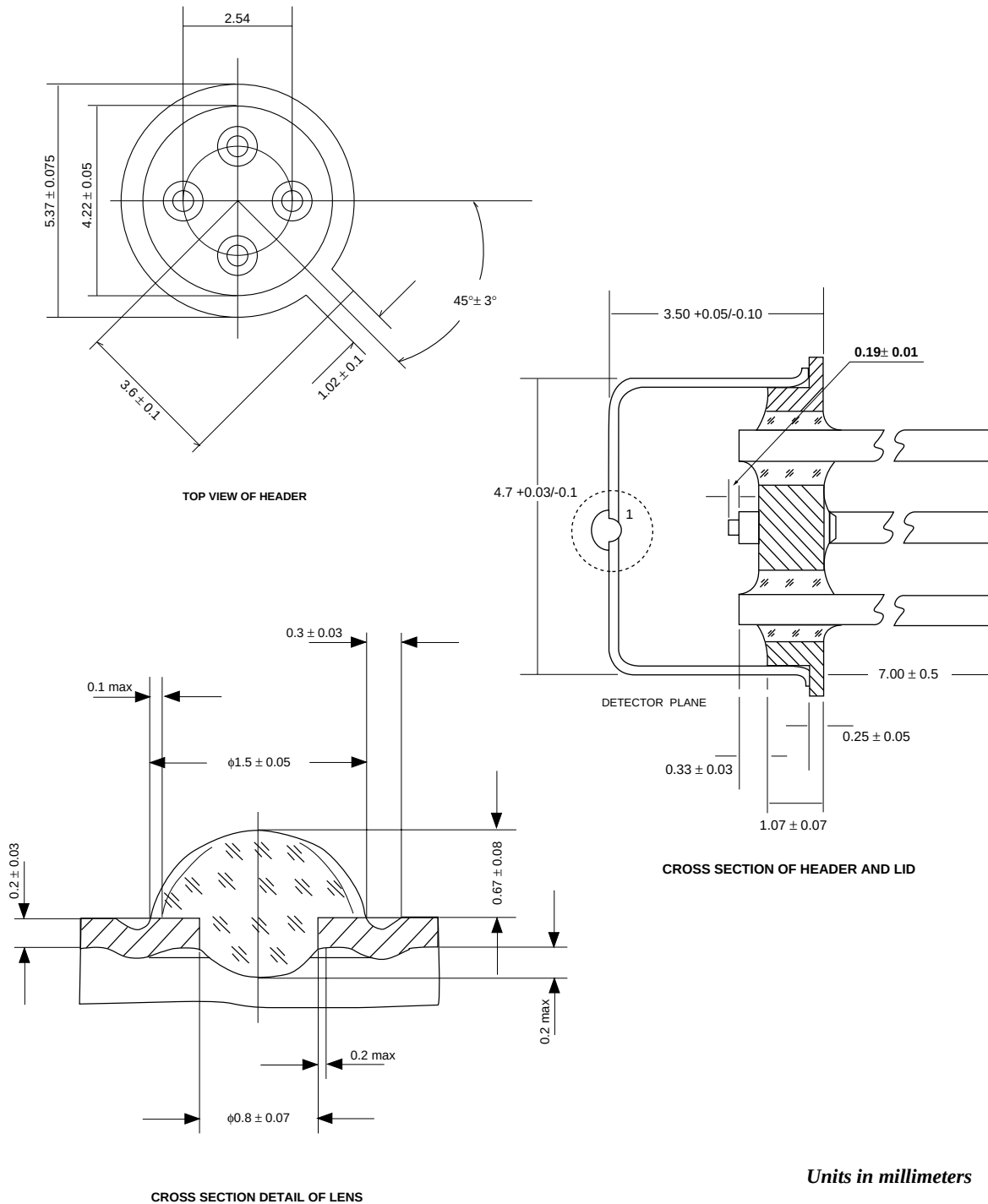


Figure 7: Mechanical Package Specifications (TO-46 Ball Lens Package with 7mm lead length)



Ordering Information

Part Numbering Scheme:

VSC77XXYY

XX =	Speed Grade
10	1.0625 Gbit/sec

YY =	Package Style
WB	5.6mm Package
WC	TO-46 Package with Ball Lens and 7mm lead length
WD	TO-46 Package with Ball Lens and 13mm lead length

Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

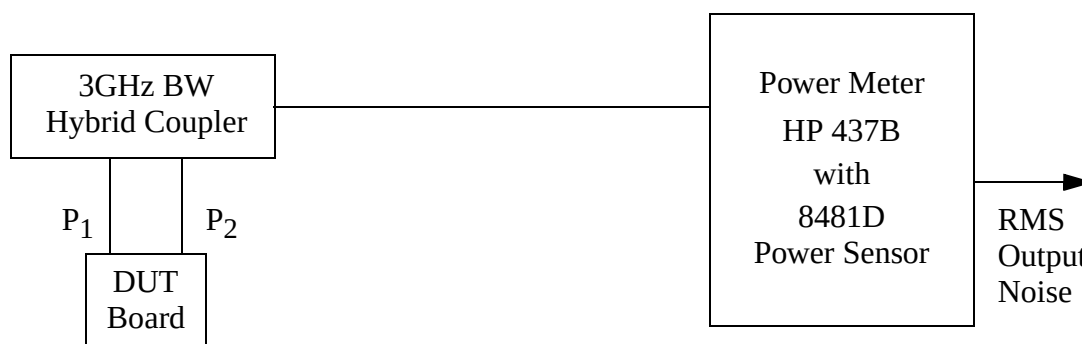
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Notes on Measurement Conditions & Applications

Note 1: Noise Measurement Method



The noise voltage, (V_n), is calculated from the Output Noise Power, (P_n), into 50 ohm.

$$V_n = \sqrt{P_n \cdot 50}$$

The noise voltage, V_n , at the output is referred back to the noise power at the input through the responsivity R (with R in volts/watts)

$$NEP = \frac{V_n}{R}$$

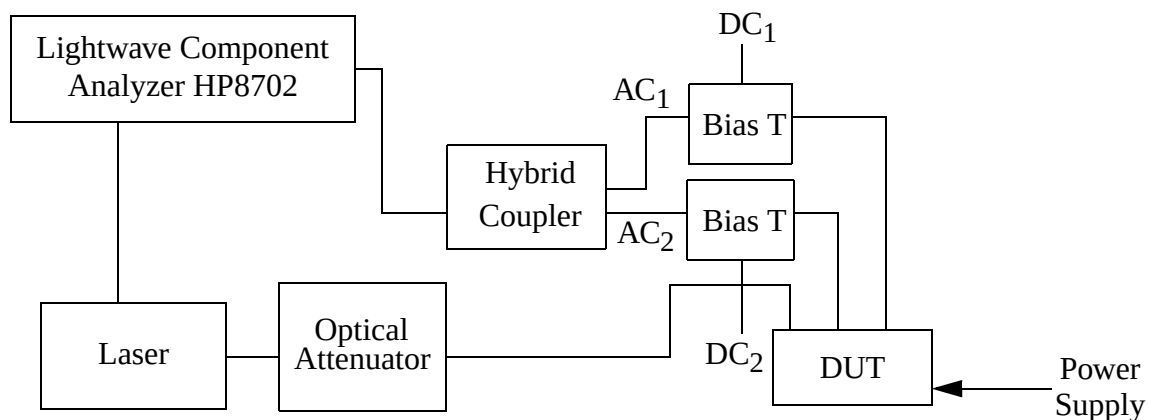
The bit error rate can be expressed as

For a $BER = 1 \times 10^{-12}$ the parameter $Q = 7$.

The sensitivity(s) at a bit error rate of 1×10^{-12} is calculated as follows:

where the NEP is in units of milliwatts and S is in dBm, respectively.

Note 2: Measurement Setup for Frequency Response



Note 3: Bias T Schematic

