Advance Product Information

VSC7130

Dual Repeater/Retimer
for Fibre Channel and Gigabit Ethernet

Features

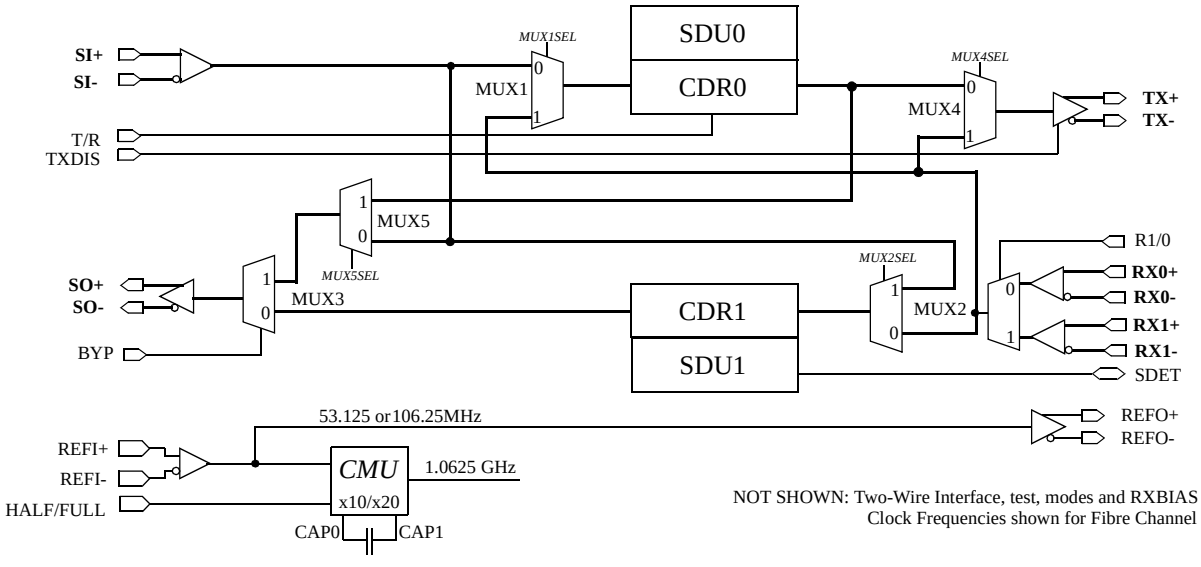
- Used in Switches, Hubs, GBICs, MIAs and JBODs
- ANSI T11 Fibre Channel Compliant at 1.0625 Gb/s
- IEEE 802.3z Gigabit Ethernet Compliant at 1.25 Gb/s
- Dual Clock and Data Recovery Units configurable as Repeaters or Retimers
- Two-Wire Serial Communications Port for control and status
- Combined Analog/Digital Signal Detect Units
- $1/10^{th}$ or $1/20^{th}$ Baud Rate TTL/PECL Reference Clock Input and PECL Output
- Bidirectional Analog/Digital Signal Detect
- 3.3V, 750mW Max Power
- 64-pin, 10x10x1.0 mm TQFP package
- Cost effective 0.35um CMOS Technology

General Description

The VSC7130 is used in Fibre Channel (1.0625 Gb/s) and Gigabit Ethernet (1.25 Gb/s) systems to provide bidirectional Clock and Data Recovery (CDR) to ensure standards compliance at critical systems interfaces. As protocol ASICs integrate multiple SerDes functions, the ASICs tend to be located far from interface connectors which results in signal degradation and difficulty in meeting industry standard signal quality specifications. The VSC7130 provides a low-cost, easy-to-use solution to this problem by ensuring standards-compliant signal quality at system interfaces. Additional circuitry implements an FC-AL Hub node.

The VSC7130 provides a pair of bidirectional CDRs which can be configured as either repeaters or retimers or bypassed altogether. Internal system data is recovered and retransmitted with standards-compliant signal quality at the connector. External receive data from the connector is recovered and retransmitted to the internal system with increased amplitude and attenuated jitter. An optional Two-Wire Interface allows robust configuration control and status monitoring of the device in order to enhance operation.

VSC7130 Block Diagram



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Applications

Several Fibre Channel and Gigabit Ethernet applications can use the VSC7130. Configuration changes between different applications are accomplished with mode pins and the Two-Wire Interface. **SI+/-** and **SO+/-** are normally connected to the duplex interface from the system while **TX+/-** and **RX0+/-** or **RX1+/-** are connected to the external link through a connector or optical transceiver. Redundant receive inputs are provided in order to optimize layouts with copper connectors or optical modules. CDR0 improves the signal quality of **SI** and retransmits the data on **TX**. CDR1 improves signal quality of **RX0** or **RX1** and retransmits recovered data to **SO**.

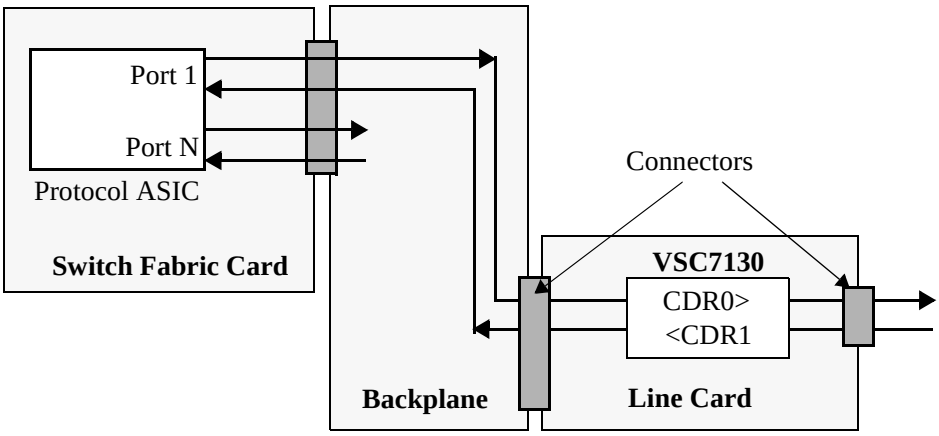
In this document, the term "Repeater" will be used for a clock and data recovery function (CDR) where the recovered serial data is retransmitted synchronously to the recovered clock. Unlike standard PLL-based CDRs, this circuit is all-digital which results in good jitter tolerance, excellent jitter transfer and low latency in a circuit which performs identically across process, voltage and temperature.

The term "Retimer" is used for a CDR which retransmits the recovered serial data synchronously to the local reference clock. This complex CDR function eliminates jitter transfer at the expense of latency. Due to the potential mismatch between the baud rate of the incoming data and the local reference clock (i.e. +/- 100ppm), an add/drop elasticity buffer is needed to insert/delete Ordered Sets to match this rate difference. The data which is added/dropped must meet Fibre Channel protocol specifications. By eliminating jitter transfer, standards compliance is ensured. The retimer function is not available for Gigabit Ethernet.

Multi-node Switch

One application for the VSC7130 is in high port-count Fibre Channel and Gigabit Ethernet systems such as switches. The following figure shows a switch with a CMOS protocol ASIC with integrated Serializer/Deserializers located on the Switch Fabric card. Serial data from the protocol ASIC passes through multiple connectors and long traces on the PCB before reaching the connector. Without the VSC7130, the signal quality at the connectors would result in poor system performance. However, by using the VSC7130, signal quality is improved to meet the specifications of Fibre Channel and Gigabit Ethernet at the system interface connectors.

Figure 1: Fibre Channel or Gigabit Ethernet Switch



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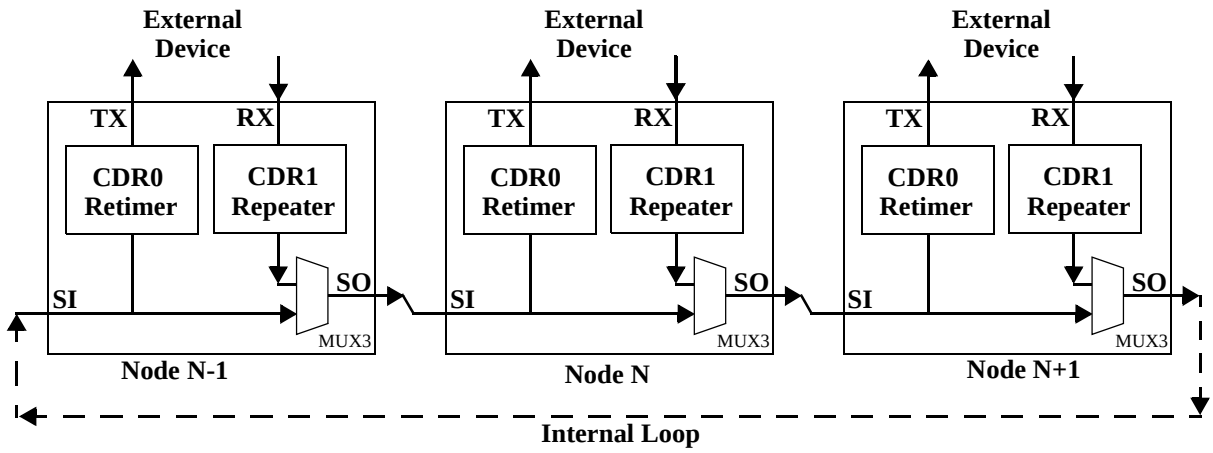
Fibre Channel Hub

The VSC7130 may be used as a single node in a Fibre Channel Arbitrated Loop Hub. In this application, incoming data on **RX** goes through a repeater (CDR1) which reduces jitter. The data is then output on **SO** to the next hub node. Incoming data from the previous hub node on **SI** goes through CDR0 which is configured as a retimer to eliminate any jitter generated inside the Hub. A bypass multiplexer (MUX3) is used to bypass nodes which do not have active devices connected. The signal detection circuitry identifies valid data at **RX** in order to control the configuration of MUX3. The **BYP** pin may be connected directly to **SDET**, **BYP** may be controlled externally or MUX3 may be controlled via the Two-Wire Interface.

Access to internal registers through the Two-Wire Interfaces allows numerous features requires by sophisticated managed Hubs such as Ordered Set Recognition, Ordered Set Generation and simple traffic monitoring.

Figure 2: Fibre Channel Arbitrated Loop Hub



Optical/Electrical Transceiver (GBIC)

As a dual repeater, the VSC7130 may provide the functions required on an Optical/Electrical transceiver such as an Optical or an a active copper Gigabit Interface Converter (GBIC). In this application, outgoing data from a system goes through CDR0 which can be configured as either a repeater or a retimer. Incoming data passing through repeater CDR1 is transferred to the system. This function implements the critical circuits in an active GBIC including RX_LOS.

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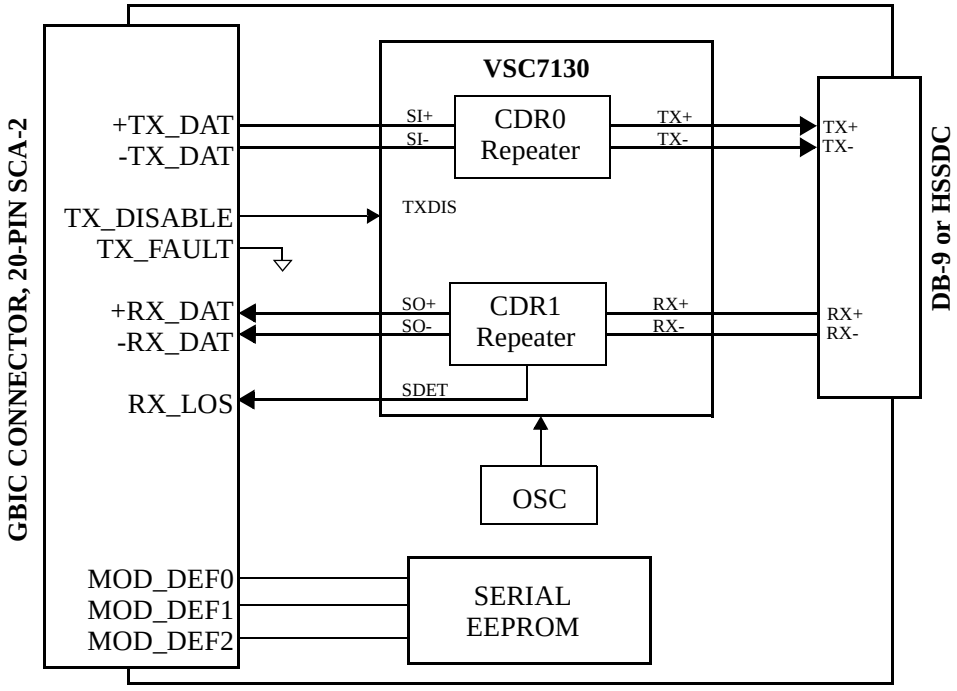
Figure 3: Active Copper GBIC Module



Functionality

Please note that this datasheet does not completely describe the VSC7130. A companion document, the "VSC7130 User's Manual" describes additional applications issues and goes into great depth regarding the Two-Wire Interface and internal register operation.

Clock Multiplier Unit and Reference Clock

A reference clock is needed for the clock multiplier unit (CMU) in order to generate the internal baud rate clock. The VSC7130 is used for both Fibre Channel (1.0625 Gb/s) and Gigabit Ethernet (1.25 Gb/s) applications. The **HALF/FULL** signal indicates whether the reference clock is $1/20^{th}$ of the baud rate (HIGH) or $1/10^{th}$ of the baud rate (LOW). The table below indicates the valid combinations of the **HALF/FULL** signal and reference clock frequency. Combinations not listed in the table will result in abnormal functionality.

Table 1: Reference Clock Frequency Selection

HALF / FULL	*Frequency*	*Application*
HIGH	53.125	Fibre Channel @ 1.0625 Gb/s
LOW	106.25	Fibre Channel @ 1.0625 Gb/s
HIGH	62.5	Gigabit Ethernet @ 1.25 Gb/s
LOW	125	Gigabit Ethernet @ 1.25 Gb/s
All Other Combinations		Not Allowed.

Implementing reference clock distribution in multi-node systems can be difficult and expensive if optimal signal quality is to be achieved. In order to reduce this burden, the VSC7130 has a flexible reference input buffer which can be either single-ended TTL, differential PECL or LVDS. If single-ended, **REFI+** should be connected to the clock source and **REFI-** should be left unconnected. **REFI-** is biased to VDD/2 for TTL thresholds. If a PECL or LVDS source is used, connect the positive side to **REFI+** and the negative side to **REFI-**. In order to provide the reference clock to multiple devices, a reference clock output, **REFO+/-**, is provided which is just an LVDS buffered version of **REFI+/-**. In this way, multiple VSC7130s may be daisy chained together with the **REFO** driving the **REFI** of the next device. When **REFO** is driving **REFI**, a 100 ohm resistor should be connected between **REFI+** and **REFI-**.

The reference clock is used by the clock multiplier unit (CMU) in order to generate the internal baud rate clock. In order to maximize signal quality of the **TX** and **SO** outputs, the **REFI** input should be of the highest quality possible with sharp edges and low jitter. Duty cycle distortion is not very important since only the rising edge of **REFI** is used. The CMU is a high performance analog PLL which multiplies the reference clock frequency by 20 or 10 depending on **HALF/FULL**. A single external 0.1uF capacitor must be connected between the CAP0 and CAP1 pins in order to control the loop bandwidth of the CMU. Separate power (**VDDA**) and ground (**VSSA**) are provided in order to allow a separately filtered power supply to reduce noise.

Input and Output Buffers, Analog Signal Detection, Cable Equalization

The **RX0+/-**, **RX1+/-** and **SI+/-** differential inputs are high performance input buffers which amplify the incoming signal. Furthermore, a cable equalization circuit is included in the input buffer which accentuates high frequency signals in order to compensate for the high frequency loss found in copper cables and traces. This cable equalization circuit enhances the ability of the VSC7130 to reliably receive serial inputs which have been degraded with jitter. The **RX1+/-** input buffer also includes an analog signal detection circuit which indicates, when HIGH, that the differential input is at least 375mV. If the input amplitude is less than 200mV the output will be LOW. If the input is between 200mV and 375mV, the output is indeterminate. The output of this signal is processed further in the Signal Detection circuitry described elsewhere.

If the Two-Wire Interface is not used, **R1/0** directly controls the **RX0** and **RX1** input buffers and Cable Equalization is enabled in **SI**, **RX0** and **RX1**. If the Two-Wire Interface is used, microcontroller control allows enabling or disabling of the cable equalization circuit.

Please refer to the “VSC7130 User’s Manual” for a more complete description of the input and output buffer controls and cable equalization controls.

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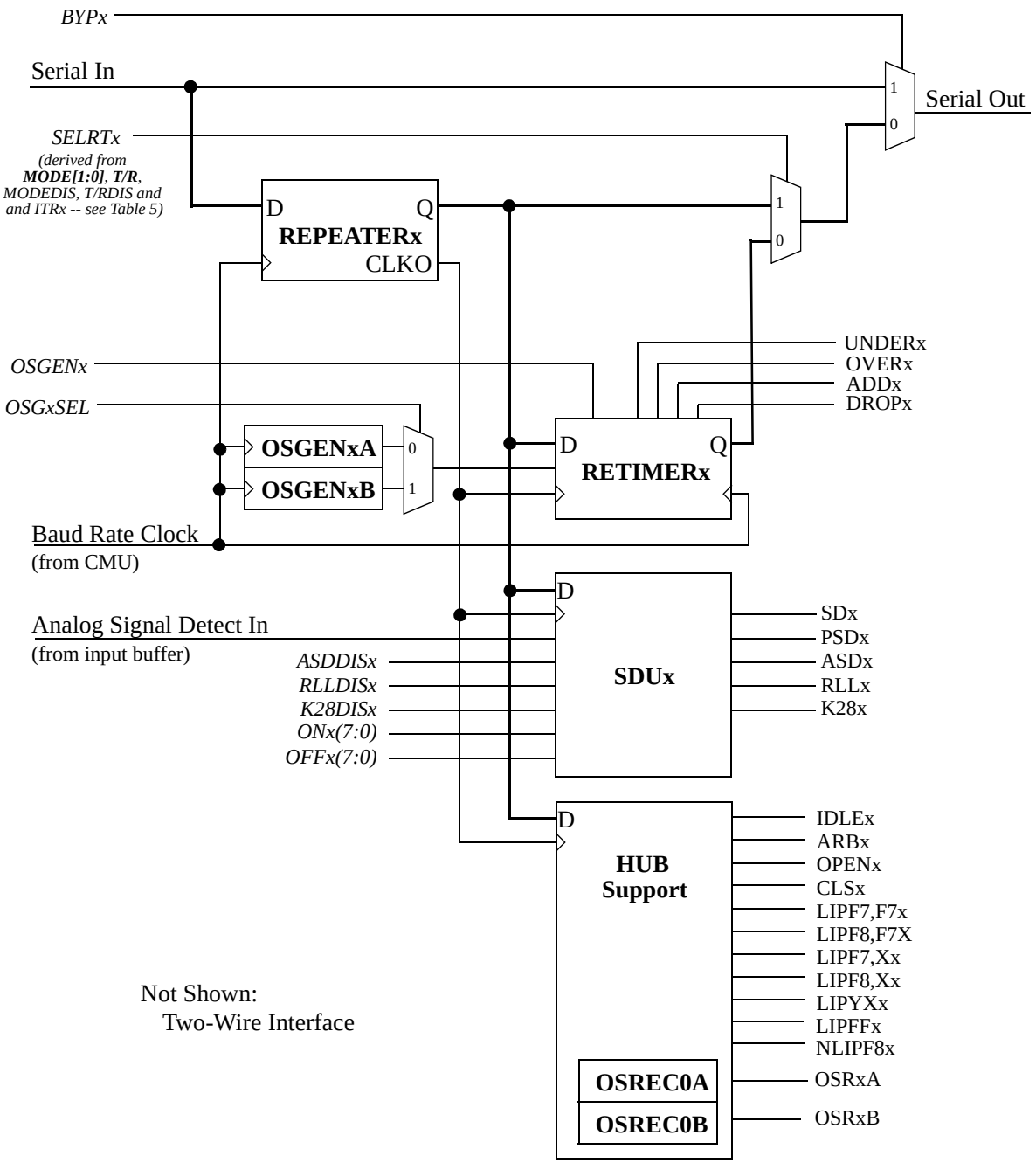
Figure 4: CDRx/SDUx Block Diagram



Clock and Data Recovery (CDR)

Two Clock and Data Recovery Units (CDR) are included in the VSC7130 in order to improve signal quality of serial data by amplification and jitter attenuation. The previous figure shows a block diagram of each with its corresponding Signal Detect Unit (SDU). Each CDR may be configured as either a repeater or a retimer using the **MODE0**, **MODE1** and **T/R** pins or via the Two-Wire Interface by programming the *MODEDIS*, *T/RDIS* and *ITRx* register bits.

Table 2: CDRx Repeater/Retimer Configuration

MODE1 pin	*MODE0 pin*	*T/R pin*	*CDR1*	*CDR0*
0	0	0	Repeater *(SELRT1=1)*	Repeater *(SELRT0=1)*
		1	Repeater *(SELRT1=1)*	reTimer *(SELRT0=0)*
0	1	0	Repeater *(SELRT1=1)*	Repeater *(SELRT0=1)*
		1	Repeater *(SELRT1=1)*	reTimer *(SELRT0=0)*
1	0	0	Repeater *(SELRT1=1)*	Repeater *(SELRT0=1)*
		1	Repeater *(SELRT1=1)*	Repeater *(SELRT0=1)*
1	1	0	reTimer *(SELRT1=0)*	Repeater *(SELRT0=1)*
		1	reTimer *(SELRT1=0)*	reTimer *(SELRT0=0)*

The $SELRT_x$ signal determines whether the repeater or retimer output is selected, as shown in Figure 6.

The *MODEDIS* register bit (CHIPCA-7) and the *T/RDIS* register bit (CHIPCA-4) can be used to disable the pin controls defined in above table for selecting repeater or retimer mode for each CDR unit. For CDR0, if the *MODEDIS* and *T/RDIS* bits are both set, the *ITR0* register bit (CDR0C-4) will control the repeater/retimer selection. For CDR1, only the *MODEDIS* register bit needs to be set in order to use *ITR1* (CDR1C-4) to control the repeater/retimer selection. A HIGH in *ITRx* selects repeater mode, and a LOW selects retimer mode.

Four sources of serial output data are selected by the BYPx signals: Serial Input (Bypass Mode), Ordered Set Generators (either A or B as selected by *OSGxSEL*, bit 5 of the CDRxC register), the output of the Repeater or the output of the Retimer.

Normally, the **SI** input passes through MUX1 to the input of CDR0 whose output is transmitted on **TX+/-** if **TXDIS** is LOW. If **TXDIS** is HIGH, **TX+** will be HIGH and **TX-** will be LOW. Similarly, the **RX** input normally passes through MUX2, CDR1 and MUX3 to the **SO** output.

The retimer has two outputs indicating whether it is adding (ADDx) or dropping (DROPx) ordered sets from the serial stream in order to perform rate matching between the incoming serial data and the local reference clock. The retimer also has an output (OVERx) indicating that an overrun condition has occurred when an order set which needed to be dropped was not able to be dropped. Similarly, underrun errors are reported when a Fill Word which needed to be added was not able to be added.

Retimer Operation

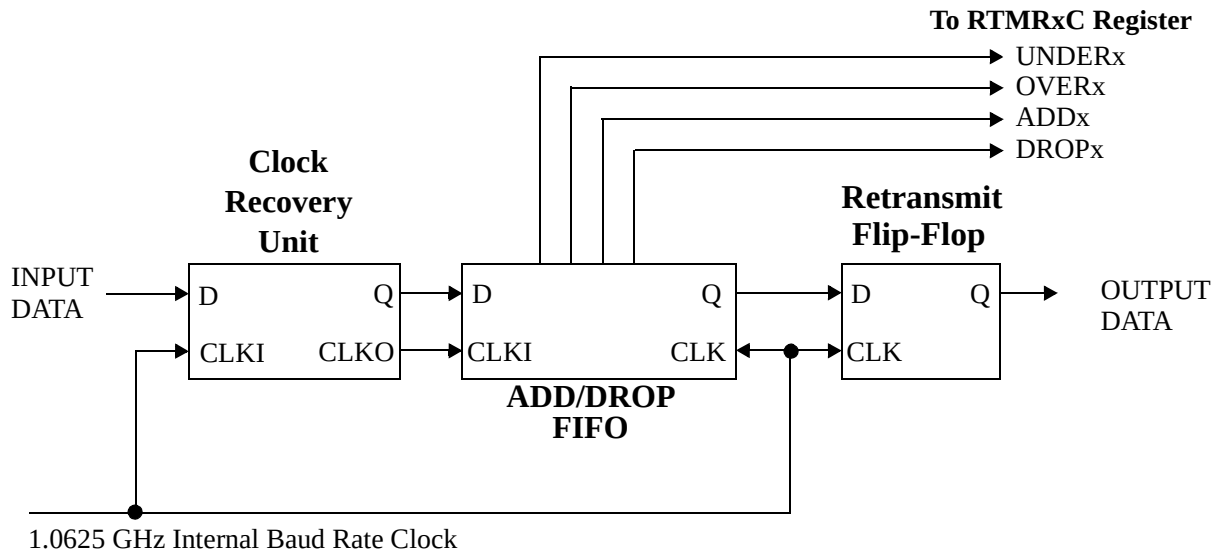
NOTE: Retimer operation is only used for Fibre Channel data at 1.0625 Gb/s. Do not use Retimer mode unless the incoming data is Fibre Channel or follows the Ordered Set structure defined by Fibre Channel. Failure to do so will result in data corruption.

When CDRx is configured as a Retimer, recovered data is resynchronized to an internally generated baud rate clock derived from the REFI. This prevents jitter at the inputs from transferring to the outputs. However,

incoming data is not necessarily at the same frequency as the internal baudrate clock, so special Fibre Channel Ordered Sets, called Fill Words, are added or dropped from the data stream in order to accommodate this speed difference. The rules for adding and dropping Fill Words are delineated in documents generated by the T11 committee: FC-PH, FC-PH2, FC-PH3, FC-AL, FC-AL2 and FC-AL3 (in progress). The VSC7130 is fully compliant with these rules.

A detailed block diagram of the Retimer is shown below. Incoming data goes into a Clock Recovery Unit (CRU) where the data is recovered and resampled. Recovered data and recovered clock are sent to the Add/Drop FIFO where the data is stored using the recovered clock. Data is removed from the Add/Drop FIFO and resynchronized by the Retransmitting Flip-Flop using the internally generated baud rate clock derived from **REFI**. The output of the Flip-Flop is recovered serial data which is synchronous to the low-jitter baud rate clock and complies with all jitter specifications for Fibre Channel.

Figure 5: Retimer Block Diagram



The internally generated baud rate clock (nominally 1.0625 GHz) is used by the Retimer for several functions. First, it provides the timing reference for the Clock Recovery Unit. Second, it clocks data out of the FIFO. Third, it retimes the retransmitted output data. The quality of the baud rate clock will impact the jitter tolerance of the Clock Recovery Unit and the jitter generation of the Retransmitter Flip-Flop. The signal quality of the internally generated baud rate clock is directly related to jitter on **REFI** and power supply noise. The user is encouraged to minimize both **REFI** jitter and power supply noise in order to maximize jitter tolerance at the input and minimize jitter generation at the output.

In the Add/Drop FIFO, a phase detector monitors the phase difference between the recovered clock and the internally generated baud rate clock to determine when to add or drop Fill Words. Fill Words can only be

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added/dropped between packets following the rules delineated by the Fibre Channel Specifications mentioned previously.

Please refer to the "VSC7130 User's Manual" for more information regarding retimer operation and associated register controls.

Signal Detection

The receiver, **RX1**, has an analog signal detect output indicating, when HIGH, that the input contains a valid Fibre Channel or Gigabit Ethernet signal level. One analog and two digital checks are used to determine if the incoming signal contains valid data, and combine to form the preliminary signal detect (PSDx) for each channel:

1.) Analog transition detection is performed on the input to verify that the signal swings are of adequate amplitude. The **RX1+/-** input buffer contains a differential voltage comparator which will go high if the differential peak-to-peak amplitude is greater than 375mV or LOW if under 200mV. If the amplitude is between 200 and 375mV, the output is indeterminate. The **RXBIAS** input may be adjusted to override these internally set levels in order to provide either different levels or tighter tolerance. If **RXBIAS** is left open, these levels are active. This check only applies to PSD1.

2.) Serial data, after the CDR, is monitored for more than five consecutive zeros or ones. Valid 8B/10B data will not have a run length greater than 5 clock periods.

3.) Serial data, after the CDR, is monitored for K28.5- (0011111010). Valid Fibre Channel or Gigabit Ethernet data will contain a K28.5- character during ~64K reference clock period. If a K28.5- is not detected during the period, SDx will be set LOW for the next period.

Please refer to the "VSC7130 User's Manual" for a more complete description of the signal detect circuitry and its associated register controls.

Hub Support

Several functions are provided in the CDRx/SDUx circuitry to support FC-AL Hubs. Two programmable 40-bit registers are available to generate data on **TX** or **SO**. This allows simple 40-bit patterns to be generated easily. Monitoring of the serial data out of the repeater provides the user with information concerning data content of packets as they are received. Many FC-AL ordered sets are detected (all ARBs, IDLE, all LIPs, all CLS and all OPENs). Furthermore, two 40-bit registers/comparators are provided to allow the user to identify when user programmable patterns occur in the data. One use of these would be to monitor for the presence of ordered sets defined after release of this product.

Please refer to the "VSC7130 User's Manual" for a more complete description of the ordered set generation and recognition capabilities and associated register controls.

Performance Monitoring

In order to determine the relative traffic on the link, a 32-bit counter is provided which increments on each occurrence of an ARB ordered set or an IDLE ordered set. By reading this counter periodically, the relative traffic on the link can be calculated.

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Please refer to the "VSC7130 User's Manual" for a more complete description of the performance monitoring capabilities and associated register controls.

Two-Wire Interface

An industry-standard Two-Wire Interface is provided to allow user access to internal control and status. Use of the interface is optional. **SCL** is the serial interface clock running at up to 400 KHz when used with readily available microcontrollers. **SDA** is a bidirectional data signal. **A4** and **A3** selects the group address of the device while **A2**-**A0** set the address. **TWI** and **TWO** are used to serially configure the address of daisy-chained devices in order to accommodate large numbers of devices on each Two-Wire Interface link. **INT#** is an open drain output used to signal an interruptible event to the microcontroller.

Please refer to the "VSC7130 User's Manual" for a more complete description of this interface, including timing diagrams.

Proprietary Interface

If higher performance than 400KHz is required, a proprietary mode may be used. In this mode, the **SCL** clock can operate at a maximum speed of 6.25 MHz. Due to the speed of this link, significant electrical limitations may be placed on the link which will restrict trace lengths, the number of daisy-chained devices and the use of multiple masters.

The Verilog code for the Master Controller in proprietary mode will be made available to customers in order to ensure compatibility. This Master Controller core is designed to use either a 25 MHz or a 50 MHz clock to generate a 6.25 MHz **SCL** clock frequency with a 25% high, 75% low duty cycle (1 clock high, 3 clocks low at 25 MHz). Slower clock frequencies are also allowable.

When using the Proprietary High-Speed mode of the Two-Wire Interface, all other interface functionality is identical to the standard Two-Wire Interface with the exception that the interface timing has changed.

Interrupt Circuitry

Interrupts are available only when the Two-Wire Interface is used otherwise **INT#** will be disabled. The **INT#** output is open-drain so an external pull-up resistor is needed to allow the output to achieve a valid TTL or CMOS HIGH level. Multiple **INT#** outputs can be wire ORed together. **INT#** is a glitchless signal which is synchronized to divide-by-32 **REFO** clock. The output of the interrupt controller prior to the output buffer is readable in *INTOUT*, CHIPS bit 2.

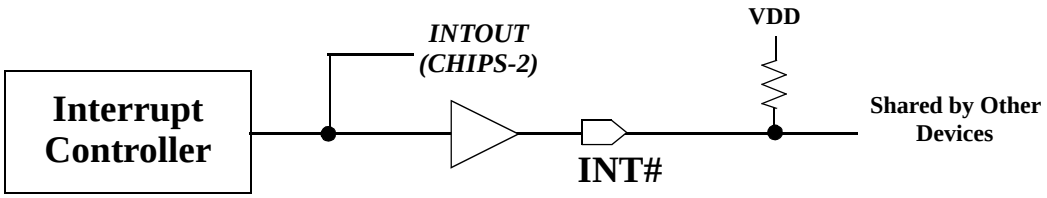
The VSC7130 is capable of managing several different kinds of internal interrupt conditions. Each interrupt source can be enabled independently using the registers accessible via the Two-Wire Interface. When an enabled interrupt event occurs, the open-drain **INT#** output will be asserted LOW and will stay LOW until the interrupt is cleared. The register address corresponding to the highest priority pending interrupt can be read from the ISR register (address F8h). This provides a relatively fast means for determining the source of the interrupt with a single register read operation.

Please refer to the "VSC7130 User's Manual" for a more complete description of the interrupt controller and its associated register controls.

Table 3: Interrupt Status Register Addresses, Priorities and Sources

Address (Hex)	*Priority*	*Label*	*Function*
22	1 (Highest)	SDU0S	SDU0 Status Register: *SDR0* (7), *SDF0* (6), *ASD0* (2), *RLL0* (1), *K280* (0)
2A	2	SDU1S	SDU1 Status Register: *SDR1* (7), *SDF1* (6), *ASD1* (2), *RLL1* (1), *K281* (0)
23	3	RTMR0C	Retimer0 Configuration Register: *UNDER0* (6), *OVER0* (4), *ADD0* (2), *DROP0* (0)
2B	4	RTMR1C	Retimer1 Configuration Register: *UNDER1* (6), *OVER1* (4), *ADD1* (2), *DROP1* (0)
6C	5	MATCHA0	Ordered Set Match Register A for CDR0: All Bits except *RES* (1)
6D	6	MATCHB0	Ordered Set Match Register B for CDR0: All Bits except *RES* (6)
7C	7	MATCHA1	Ordered Set Match Register A for CDR1: All Bits except *RES* (1)
7D	8	MATCHB1	Ordered Set Match Register B for CDR1: All Bits except *RES* (6)
F4	9 (Lowest)	TEST4	Test Register 4: TESTINT (4) for diagnostics

Table 4: Block Diagram of Interrupt Output



Programmable Registers

A list of the programmable registers accessible by the Two-Wire Interface is shown below. This list includes the address of the register, whether it is Readable and/or Writable, if it is a source of interrupts, the register's name and function. Following this table is a complete description of each register. The registers for CDR1 are identical to the CDR0 registers but only the CDR0 registers are documented.

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Table 5: Programmable Registers

Address (Hex)	*Read/Write (or Clear)*	*Interrupt Source*	*Label*	*Function*
CONFIGURATION/STATUS REGISTERS				
00	R	N	CHIPS	Chip Status Register
01	R/W	N	CHIPCA	Chip Configuration Register A
02	R/W	N	CHIPCB	Chip Configuration Register B
03	R/W	N	CHIPCC	Chip Configuration Register C
CDR0/ CDR1	CDR0 REGISTERS			
20/28	R/W	N	CDR0C	CDR0 Configuration Register
21/29	R/W	N	SDU0C	SDU0 Configuration Register
22/2A	R/C	Y	SDU0S	SDU0 Status Register
23/2B	R/W/C	Y	RTMR0C	Retimer0 Configuration Register
24/2C	R/W	N	CNTON0	ON Count Register for SDU0
25/2D	R/W	N	CNTOFF0	OFF Count Register for SDU0
60/70	R/W	N	OSGEN0A0	Ordered Set Generator A, Bits 39-32 for CDR0
61/71	R/W	N	OSGEN0A1	Ordered Set Generator A, Bits 31-24 for CDR0
62/72	R/W	N	OSGEN0A2	Ordered Set Generator A, Bits 23-16 for CDR0
63/73	R/W	N	OSGEN0A3	Ordered Set Generator A, Bits 15-8 for CDR0
64/74	R/W	N	OSGEN0A4	Ordered Set Generator A, Bits 7-0 for CDR0
65/75	R/W	N	OSGEN0B0	Ordered Set Generator B, Bits 39-32 for CDR0
66/76	R/W	N	OSGEN0B1	Ordered Set Generator B, Bits 31-24 for CDR0
67/77	R/W	N	OSGEN0B2	Ordered Set Generator B, Bits 23-16 for CDR0
68/78	R/W	N	OSGEN0B3	Ordered Set Generator B, Bits 15-8 for CDR0
69/79	R/W	N	OSGEN0B4	Ordered Set Generator B, Bits 7-0 for CDR0
6C/7C	R/C	Y	MATCHA0	Match Register A for CDR0
6D/7D	R/C	Y	MATCHB0	Match Register B for CDR0
6E/7E	R/W	N	MATIEA0	Match Interrupt Enable Register A for CDR0
6F/7F	R/W	N	MATIEB0	Match Interrupt Enable Register B for CDR0
80/90	R/W	N	OSREC0A0	Ordered Set Recognition Register A, Bits 39-32 for CDR0
81/91	R/W	N	OSREC0A1	Ordered Set Recognition Register A, Bits 32-24 for CDR0
82/92	R/W	N	OSREC0A2	Ordered Set Recognition Register A, Bits 23-16 for CDR0
83/93	R/W	N	OSREC0A3	Ordered Set Recognition Register A, Bits 15-8 for CDR0
84/94	R/W	N	OSREC0A4	Ordered Set Recognition Register A, Bits 7-0 for CDR0
85/95	R/W	N	OSMASK0A 0	Ordered Set Mask Register A, Bits 39-32 for CDR0
86/96	R/W	N	OSMASK0A 1	Ordered Set Mask Register A, Bits 31-24 for CDR0
87/97	R/W	N	OSMASK0A 2	Ordered Set Mask Register A, Bits 23-16 for CDR0

Address (Hex)	*Read/Write (or Clear)*	*Interrupt Source*	*Label*	*Function*
88/98	R/W	N	OSMASK0A 3	Ordered Set Mask Register A, Bits 15-8 for CDR0
89/99	R/W	N	OSMASK0A 4	Ordered Set Mask Register A, Bits 7-0 for CDR0
A0/B0	R/W	N	OSREC0B0	Ordered Set Recognition Register B, Bits 39-32 for CDR0
A1/B1	R/W	N	OSREC0B1	Ordered Set Recognition Register B, Bits 32-24 for CDR0
A2/B2	R/W	N	OSREC0B2	Ordered Set Recognition Register B, Bits 23-16 for CDR0
A3/B3	R/W	N	OSREC0B3	Ordered Set Recognition Register B, Bits 15-8 for CDR0
A4/B4	R/W	N	OSREC0B4	Ordered Set Recognition Register B, Bits 7-0 for CDR0
A5/B5	R/W	N	OSMASK0B 0	Ordered Set Mask Register B, Bits 39-32 for CDR0
A6/B6	R/W	N	OSMASK0B 1	Ordered Set Mask Register B, Bits 31-24 for CDR0
A7/B7	R/W	N	OSMASK0B 2	Ordered Set Mask Register B, Bits 23-16 for CDR0
A8/B8	R/W	N	OSMASK0B 3	Ordered Set Mask Register B, Bits 15-8 for CDR0
A9/B9	R/W	N	OSMASK0B 4	Ordered Set Mask Register B, Bits 7-0 for CDR0
C0/D0	R/W	N	PCNT00	Performance Counter 0, Bits 31-24 for CDR0
C1/D1	R/W	N	PCNT10	Performance Counter 0, Bits 23-16 for CDR0
C2/D2	R/W	N	PCNT20	Performance Counter 0, Bits 15-8 for CDR0
C3/D3	R/W	N	PCNT30	Performance Counter 0, Bits 7-0 for CDR0
C4/D4	R/W	N	PC0CTL	Performance Counter 0 Control Register
MISCELLANEOUS REGISTERS				
F0	-	N	TEST0	Test Register #0, For Factory Test Only, Do Not Access
F1	-	N	TEST1	Test Register #1, For Factory Test Only, Do Not Access
F2	-	N	TEST2	Test Register #2, For Factory Test Only, Do Not Access
F3	-	N	TEST3	Test Register #3, For Factory Test Only, Do Not Access
F4	R/W	Y	TEST4	Test Register #4, Soft Reset, TWOPOR & **INT#** Control Register
F5	-	N	TEST5	Test Register #5, For Factory Test Only, Do Not Access
F6	-	N	TEST6	Test Register #6, For Factory Test Only, Do Not Access
F7	R/W	N	SADDR	Soft ADDRess Register
F8	R/C	N	ISR	Interrupt Status Register (Read then Clear)
FD	R	N	MODEL1	Model Number Register (High Byte)
FE	R	N	MODEL0	Model Number Register (Low Byte)
FF	R	N	VER	Version Register

Note: Please refer to the "VSC7130 User's Manual" for a thorough description of each register and its function.

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AC Characteristics *(Over Recommended Operating Conditions).*

Figure 6: AC Timing Diagrams

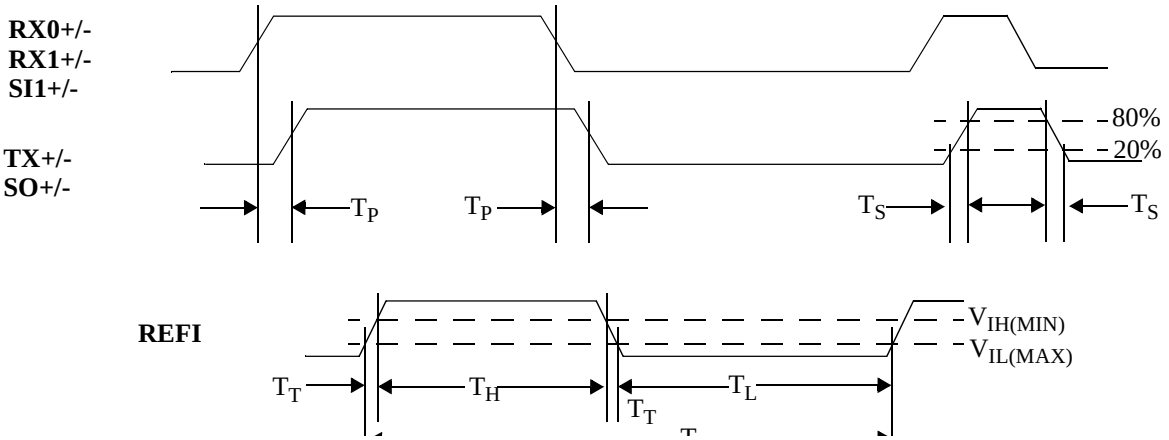

Table 6: AC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_P	Latency from any Serial Input to any Serial Output	0.25	7.0	ns	No Retimer in path
T_S	Differential Output Rise/Fall time	—	300	ps	Between 20% and 80%
$T_{J(RPTR)}$	Total data output jitter [Retimer Mode]	—	192	ps	Jitter Generation at **TX/SO** when driven by the CRU in Repeater Mode. IEEE 802.3z Clause 38.68
$T_{DJ(RPTR)}$	Serial data output deterministic jitter (p-p) [Retimer Mode]	—	80	ps	Jitter Generation at **TX/SO** when driven by the CRU in Repeater Mode. IEEE 802.3z Clause 38.68
$T_{J(RTMR)}$	Total data output jitter [Retimer Mode]	—	192	ps	Jitter Generation at **TX/SO** when driven by the CRU in Retimer Mode. IEEE 802.3z Clause 38.68
$T_{DJ(RTMR)}$	Serial data output deterministic jitter (p-p) [Retimer Mode]	—	80	ps	Jitter Generation at **TX/SO** when driven by the CRU in Retimer Mode. IEEE 802.3z Clause 38.68
T_{JTOL}	Jitter Tolerance at **RX0/RX1/SI**	0.24	—	UI	Minimum Eye Opening for proper operation as defined in MJS 8.0.
T_T	**REFI** input rise/fall times	—	1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
F	**REFI** Frequency	105 52.5	126 63	MHz	**HALF/FULL** is LOW **HALF/FULL** is HIGH
F_O	Frequency Offset between incoming data and **REFI**.	-200	+200	ppm	
DC	**REFI** Duty Cycle	30	70	%	Measured at 1.5V
T_H , T_L	**REFI** Input HIGH/LOW time	1.5	—	ns	From $V_{IH(MIN)}$ to $V_{IH(MIN)}$ or $V_{IL(MAX)}$ to $V_{IL(MAX)}$

DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0mA
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.3V ± 5%
P_D	Power Dissipation	—	500	800	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current	—	150	230	mA	Outputs open, V_{DD} = V_{DD} max
ΔV_{IN}[1]	PECL input swing: **RX0**, **RX1** or **SI** (PECL+) - (PECL-)	300	—	2200	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
ΔV_{OUT75}[1]	PECL output swing: **TX** or **SO** (PECL+) - (PECL-)	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}[1]	PECL output swing: **TX** or **SO** (PECL+) - (PECL-)	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V

[1] *NOTE: Refer to Application Note, AN-37, for differential measurement techniques.*

Absolute Maximum Ratings *(1)*

Power Supply Voltage (V_{DD}) ..... -0.5V to +4V
PECL DC Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage ..... -0.5V to 5.5V
DC Voltage Applied to TTL Outputs ..... -0.5V to V_{DD} + 0.5V
TTL Output Current ..... +/-50mA
PECL Output Current ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65° to + 150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage ..... 3.3V +/- 5%
Ambient Operating Temperature Range ..... 0°C Ambient to +95°C Case

Notes:

1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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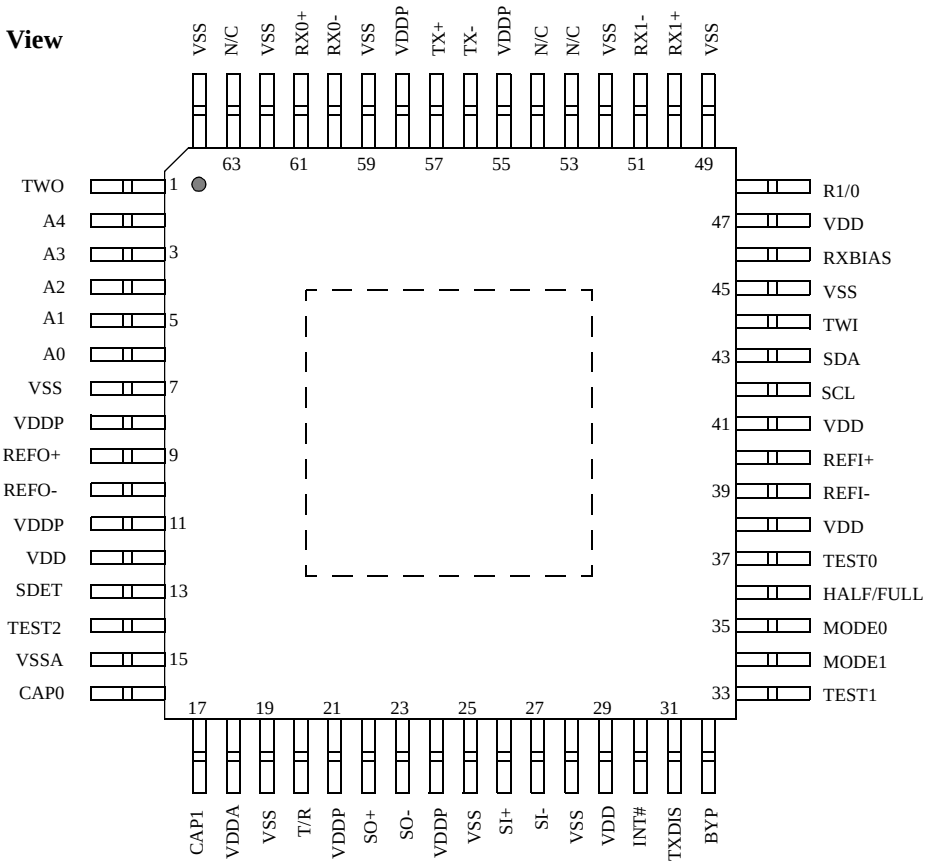
Package Pin Descriptions

Figure 7: Pin Diagram



NOTE: Exposed pad on bottom must be connected to ground.

Table 7: Pin Identification

Pin #	*Name*	*Description*
61, 60	RX0+, RX0-	INPUT - Differential. Serial input to MUX2/MUX1 from the external media.
50, 51	RX1+, RX1-	INPUT - Differential. Serial input to MUX2/MUX1 from the external media.
48	R1/0	INPUT - TTL. Selects **RX1+/-** when HIGH, **RX0+/-** when LOW.
26, 27	SI+, SI-	INPUT - Differential. Serial input to MUX1/MUX3 from the internal system.
57, 56	TX+, TX-	OUTPUT - Differential. Serial output from Repeater0 to the external media.
22, 23	SO+, SO-	OUTPUT - Differential. Serial output from Repeater1 to the internal system.
31	TXDIS	INPUT - TTL. When HIGH, **TX+**=HIGH, **TX-**=LOW. When LOW, **TX+/-** is enabled. Can be overridden by *TXDDIS*.
40 39	REFI+ REFI-	INPUT - TTL or PECL. REFerence CLocK at 1/10th or 1/20th the baud rate as determined by **HALF/FULL**. Used for the clock multiplier unit. If TTL, leave **REFI-** open. If PECL, connect both **REFI+** and **REFI-**.

Pin #	Name	Description
35 34	MODE0 MODE1	INPUT - TTL. Selects the mode. 00=Dual Repeater, 01=Hub, 10=GBIC, 11=reserved. Overridden by the *MODEDIS* register bit.
36	HALF/FULL	INPUT - TTL. When LOW, **REFI** is 1/10th the baud rate. When HIGH, **REFI** is 1/20th the baud rate
9 10	REFO+ REFO-	OUTPUT - PECL: This is a buffered version of **REFI+/-** which is intended for daisy chaining the reference clocks between multiple chips.
13	SDET	BIDIRECTIONAL - TTL: Configured by default as an input intended to be connected to the LOS from an optics module. Can be configured as an output via the Two-Wire Interface so the protocol device can determine if valid data is present.
46	RXBIAS	INPUT - ANALOG: An external resistor to ground sets the level of the analog signal detect circuits in the **RX0+/-**, **RX1+/-** and **SI+/-** inputs.
20	T/R	INPUT - TTL. When HIGH, CDR0 is configured as a Retimer, when LOW, a Repeater. Overridden by *T/RDIS*.
32	BYP	INPUT - TTL. When HIGH, MUX3 passes **SI** to **SO**. When LOW, MUX3 passes the output of CDR1 to **SO**. Overridden by *BYPDIS*.
16, 17	CAP0, CAP1	Clock Multiplier Unit PLL Loop Filter Capacitor. Nominally 0.1 uF, +/-20%, X7R
43	SDA	BIDIRECTIONAL - TTL: This is the Two-Wire Interface data pin
42	SCL	INPUT - TTL: This is the Two-Wire Interface serial clock input. For normal Two-Wire Interface usage, **SCL** may be clocked at up to 400 KHz. For Proprietary Link mode, **SCL** should be at **REFI**/8 (**HALF/FULL** is HIGH) or **REFI**/16 (**HALF/FULL** is LOW).
6, 5, 4, 3, 2	A0-A4	INPUT - TTL: **A4** is the address to select the group address for Two-Wire Interface addressing. **A0**-**A3** select the Two-Wire Interface address. **A0**-**A3** are active only if **TWI** is LOW.
44	TWI	INPUT - TTL: Two-Wire Interface Input. This input enables daisy chaining of devices on the Two-Wire Interface so that addresses can be assigned in software.
1	TWO	OUTPUT - TTL: Two-Wire Interface Output. This output enables daisy chaining of devices on the Two-Wire Interface so that addresses can be assigned in software.
30	INT#	OUTPUT - TTL (Open Drain): This output indicates that an interruptible condition occurred internally.
37 33 14	TEST0 TEST1 TEST2	INPUT - TTL. LOW for factory test, HIGH for normal operation.
12, 29, 38 41, 47	VDD	Power Supply. 3.3V Supply.
8, 11 21, 24 55, 58	VDDP	High-Speed Output Power Supply. Pins 8 and 11 are for **REFO+/-** and may be left unconnected in order to power down this output buffer. Pins 21 and 24 are for **SO+/-**. Pins 55 and 58 are for **TX+/-**
18	VDDA	Analog Power Supply. 3.3V for Clock Multiplier PLL. Bypass to **VSSA**
15	VSSA	Analog Ground
7, 19, 25 28, 45, 49, 52 59, 62, 64	VSS	Ground.
53, 54, 63	N/C	Do not connect. (These are internally connected).

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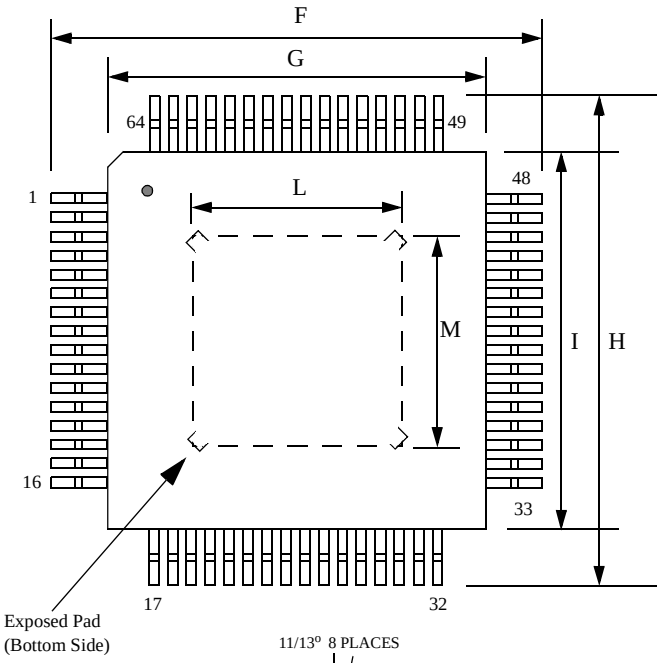
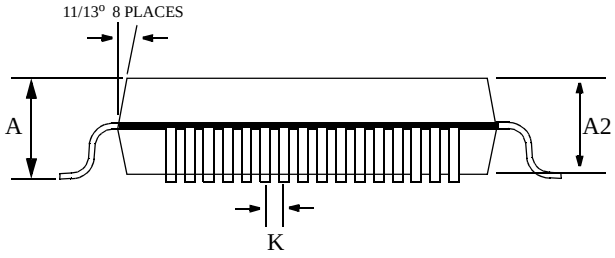
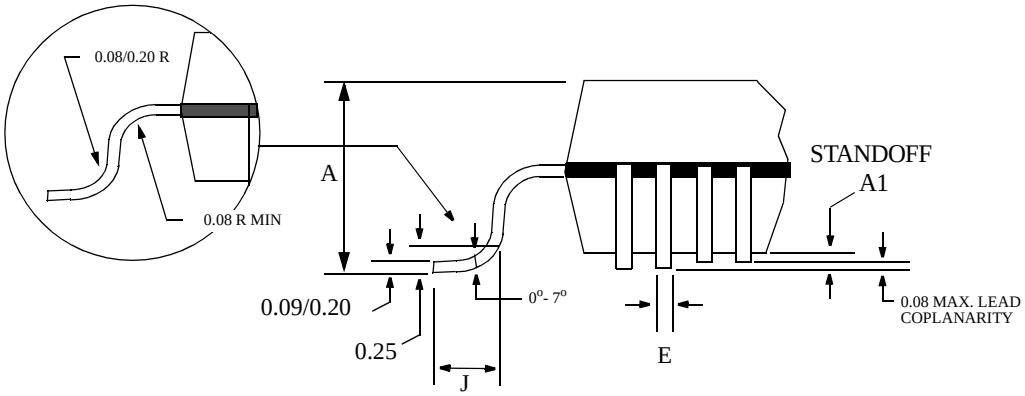
Package Information: 64-pin TQFP



Item	*10 mm*	*Tolerance*
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	12.00	BASIC
G	10.00	BASIC
H	12.00	BASIC
I	10.00	BASIC
J	0.60	±0.15
K	0.50	BASIC
L	5.00	BASIC
M	5.00	BASIC





NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.

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Package Thermal Characteristics

The VSC7130 is packaged in an exposed pad, thin quad flatpack (TQFP) which adheres to industry standard EIAJ footprints for a 10x10x1.0mm body, 64 lead TQFP. The package construction is shown below. The bottom of the leadframe is exposed so that it can be soldered to the printed circuit board and connected to the ground plane. This provides excellent thermal characteristics and reduces electrical parasitics as well.

Figure 8: Package Cross Section

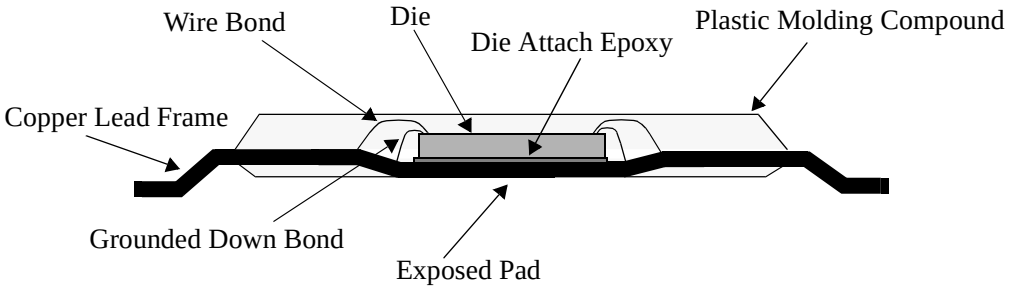


Table 8: 64-pin, Exposed Pad, TQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
$\theta_{ca\text{-}0}$	Thermal resistance from case to ambient, still air	30	^{o}C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient, 100 LFPM air	25	^{o}C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient, 200 LFPM air	23	^{o}C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient, 400 LFPM air	21	^{o}C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient, 600 LFPM air	20	^{o}C/W

The VSC7130 is designed to operate with a case temperature up to 95^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown above, the VS7130 can operate in still air ambient temperatures of 70^{o}C [~70^{o}C = 95^{o}C - 0.8W * 30]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided. Additional heat can be transferred to the printed circuit board by not using thermal reliefs on the power and ground plane vias as well as using multiple vias to the power and ground planes.

If the exposed pad is not soldered to the printed circuit board and grounded, both thermal and electrical performance will be degraded significantly.

Moisture Sensitivity Level

This device is rated at a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7130RC

Device Type:

VSC7130: Dual Repeater

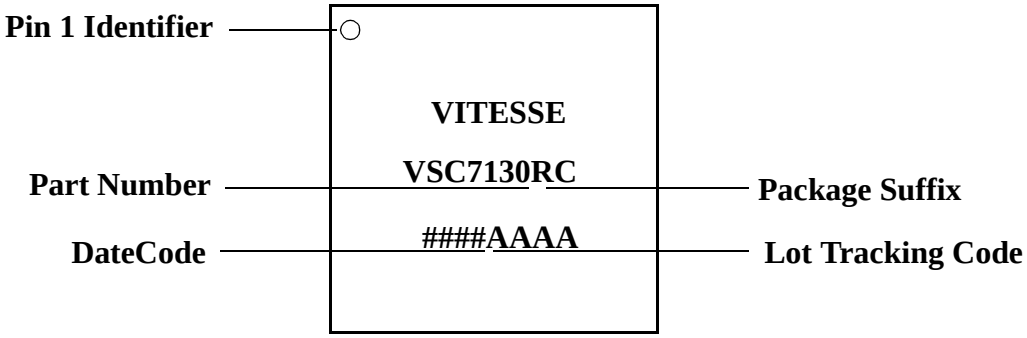
Package Style

RC: 64-pin, 10x10x1.0 mm Exposed Pad TQFP

Marking Information

The top of the package is marked as shown below.

Figure 9: Package Marking Information



Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in the document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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Revision History

P5/7 Rx1 is signal detect only
P6 f8,lip8 etc… missing
P8 64k ref clock is not active
P11 asd dis0 defaults high
P? ordered set generation only works in retimer mode
P19 test 4 is out of date
P20 *(RPTR) => repeater mode
P21 330ma is power estimate
P21 add HT i/o Spec (levels)
P21 if sig detect not fire ?
P23 pin 1 is not ground
P25 change 0.8W
P25 remove downbonds
P28 no open issues
Add high speed open loop pll
Add high speed I2C not operate

Changes between Rev 2.2 and Rev 2.3:
- All pages: Ran spellchecker and looked for extra spaces
- All pages: Attempted to make consistent use of “Two-Wire Interface” phrase.
- All pages: Attempted to make consistent use of **bold** type for pin names.
- All pages: Attempted to make consistent use of *italic* type for register control bit names.
- All pages: Updated any text section shared in the VSC7130 User’s Manual.
- All pages: Removed length sections involving register controls, these will appear in User’s Manual only.
- p18: Removed pin 1 from VSS pin list -- pin 1 is actually **TWO**.

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