Advance Product Information

VSC7123 - Extended Temperature Range

10-Bit Transceiver for Fibre Channel and Gigabit Ethernet

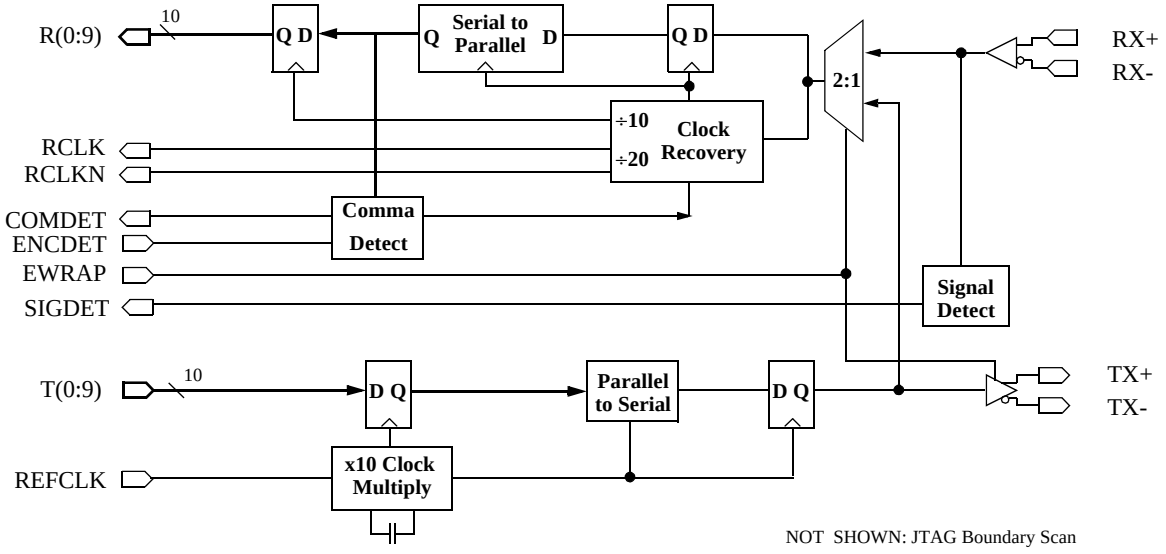
Features

- 802.3z Gigabit Ethernet Compliant 1.25 Gb/s Transceiver
- ANSI X3T11 Fibre Channel Compliant 1.0625 Gb/s Transceiver
- 0.98 Gb/s to 1.36 Gb/s Full-Duplex Operation
- 10-Bit TTL Interface for Transmit and Receive Data
- Operating Temperature Down to -40°
- RX Cable Equalization
- Analog/Digital Signal Detection
- JTAG Access Port for Testability
- 64-Pin, 10 mm TQFP Package
- Single +3.3V Supply, 650mW

General Description

The VSC7123 Extended Temperature Range (ETR) is a full-speed Fibre Channel and Gigabit Ethernet Transceiver with industry-standard pinouts, which operates down to –40°. The VSC7123 ETR accepts 10-bit 8B/10B encoded transmit data, latches it on the rising edge of REFCLK and serializes it onto the TX PECL differential outputs at a baud rate which is 10 times the REFCLK frequency. Serial data input on the RX PECL differential inputs is resampled by the Clock Recovery Unit (CRU) and deserialized onto the 10-bit receive data bus synchronously to complementary divide-by-twenty clocks. The VSC7123 ETR receiver detects “Comma” characters for frame alignment. An analog/digital signal detection circuit indicates that a valid signal is present on the RX input. A cable equalizer compensates for InterSymbol Interference (ISI) in order to increase maximum cable distances.

VSC7123 ETR Block Diagram



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Functional Description

Clock Synthesizer

The VSC7123 ETR clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock between 0.98GHz and 1.36GHz. The on-chip Phase Lock Loop (PLL) uses a single external 0.1µF capacitor to control the Loop Filter.

Serializer

The VSC7123 ETR accepts TTL input data as a parallel 10 bit character on the T(0:9) bus, which is latched into the input register on the rising edge of REFCLK. This data is serialized and transmitted on the TX PECL differential outputs at a baud rate that is 10 times the frequency of the REFCLK, with bit T0 transmitted first. User data should be encoded using 8B/10B block code or equivalent.

Transmission Character Interface

An encoded byte is 10 bits and is referred to as a transmission character. The 10-bit interface on the VSC7123 ETR corresponds to a transmission character. This mapping is shown in Figure 1.

Figure 1: Transmission Order and Mapping of an 8B/10B Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	X	X	X	1	1	1	1	1	0	0

Last Data Bit Transmitted — First Data Bit Transmitted

Clock Recovery

The VSC7123 ETR accepts differential high-speed serial inputs on the RX+/RX- pins, extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for InterSymbol Interference which may be present in the incoming data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B encoding scheme. The CRU is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within ±200ppm of 10 times the REFCLK frequency. For example, Gigabit Ethernet systems would use 125MHz oscillators with a ±100ppm accuracy resulting in ±200ppm between VSC7123 ETR pairs.

Deserializer

The recovered serial bit stream is converted into a 10-bit parallel output character. The VSC7123 ETR provides complementary TTL recovered clocks, RCLK and RCLKN, which are $1/20^{th}$ of the serial baud rate. The clocks are generated by dividing down the high-speed recovered clock which is phase-locked to the serial data. The serial data is retimed, deserialized and output on R(0:9). The parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN.

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If serial input data is not present, or does not meet the required baud rate, the VSC7123 ETR will continue to produce a recovered clock, allowing downstream logic functionalilty to continue. The RCLK/RCLKN output frequency under these circumstances will differ from its expected frequency by no more than ±1%.

Word Alignment

The VSC7123 ETR provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled by asserting ENCDET HIGH. When synchronization is enabled, the receiver examines the recovered serial data for the presence of the "Comma" character. This pattern is "0011111XXX", where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined for synchronization purposes. Improper alignment of the "Comma" character is defined as any of the following conditions:

1) The comma is not aligned within the 10-bit transmission character such that R0...R6 = "0011111".
2) The comma straddles the boundary between two 10-bit transmission characters.
3) The comma is properly aligned but occurs in the received character presented during the rising edge of RCLK rather than RCLKN.

When ENCDET is HIGH and an improperly aligned comma is encountered, the recovered clock is stretched (never slivered) so that the comma character and recovered clocks are properly aligned to R(0:9). This results in proper character and word alignment. When the parallel data alignment changes in response to an improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. Additionally, the first Comma pattern may also be lost or corrupted. Subsequent data will be output correctly and properly aligned. When ENCDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, COMDET is driven HIGH. The COMDET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COMDET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 2 and Figure 3. Figure 2 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COMDET pulse in relation to the comma character on R(0:9). Figure 3 shows the case where the K28.5 is detected, but it is misaligned so a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

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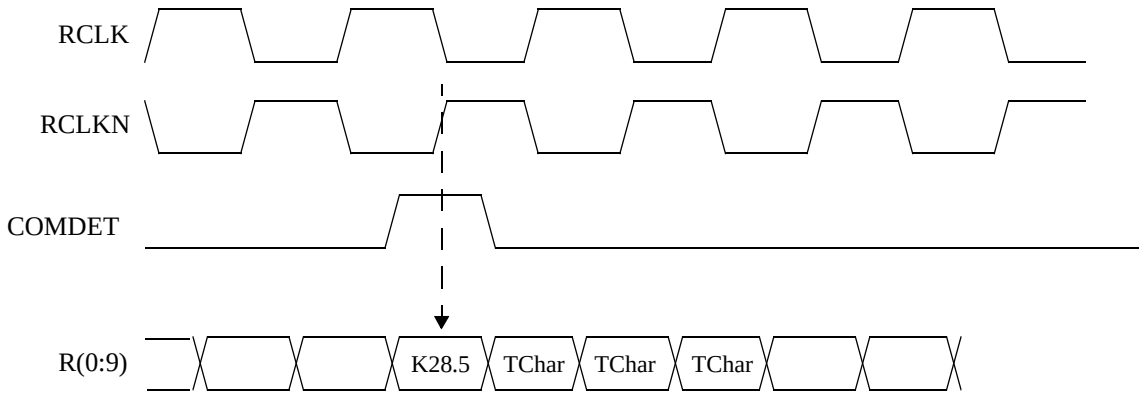
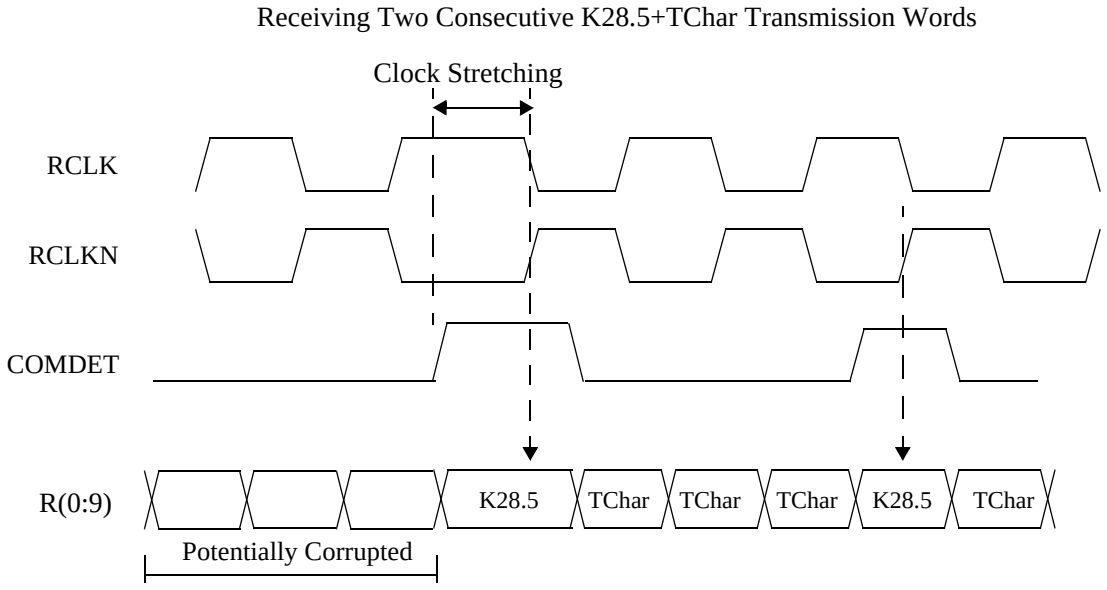
Figure 2: Detection of a Properly Aligned Comma Character



TChar: 10 bit Transmission Character

Figure 3: Detection and Resynchronization of an Improperly Aligned Comma Character



TChar: 10 bit Transmission Character

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Signal Detection

The receiver has an output, SIGDET, indicating, when HIGH, that the RX input contains a valid Fibre Channel or Gigabit Ethernet signal. A combination of one analog and three digital checks are used to determine if the incoming signal contains valid data. SIGDET is updated every four RCLKs. During the current period, if all four of the following criteria are met, SIGDET will be HIGH during the next 4-RCLK period. If any of the four criteria is not met during the current period, SIGDET will be LOW during the next 4-RCLK period.

1) Analog transition detection is performed on the input to verify that the signal swings are of adequate amplitude. The RX+/- input buffer contains a differential voltage comparator which will go high if the differential peak-to-peak amplitude is greater than 400mV or LOW if under 200mV. If the amplitude is between 200 and 400mV, the output is indeterminate.
2) Data on R(0:9) is monitored for all zeros (0000000000). If this pattern is encountered during the current RCLK interval, the SIGDET output will go LOW during the next 4-RCLK interval.
3) Data on R(0:9) is monitored for all ones (1111111111). If this pattern is encountered during the current RCLK interval, the SIGDET output will go LOW during the next 4-RCLK interval.
4) Data on R(0:9) is monitored for K28.5- (0011111010). Unlike previous patterns, the interval during which a K28.5- must occur is 64K+24 10-bit characters in length. Valid Fibre Channel or Gigabit Ethernet data will contain a K28.5- character during any period of this length. If a K28.5- is not detected during the monitoring period, SIGDET will go LOW during the next period.

The behavior of SIGDET is affected by EWRAP and ENCDET as shown in Table 1.

Table 1: Signal Detect Behavior

EWRAP	*ENCDET*	*COMDET*	*Transition Detect*	*All Zeros/ All Ones*	*K28.5 Presence*	*Mode*
0	0	Disabled	Enabled	Enabled	Enabled	Normal
0	1	Enabled	Enabled	Enabled	Disabled	SIGDET ignores commas
1	0	Disabled	Enabled	Disabled	Disabled	Loopback
1	1	Enabled	Enabled	Disabled	Disabled	Loopback

NOTE: COMDET, RCLK, RCLKN and R(0:9) are unaltered by SIGDET.

JTAG Access Port

A JTAG Access Port is provided to assist in board-level testing. Through this port most pins can be accessed or controlled and all TTL outputs can be tri-stated. A full description of the JTAG functions on this device is available in “VSC7123/VSC7133 JTAG Access Port Functionality.”

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Figure 4: Transmit Timing Waveforms

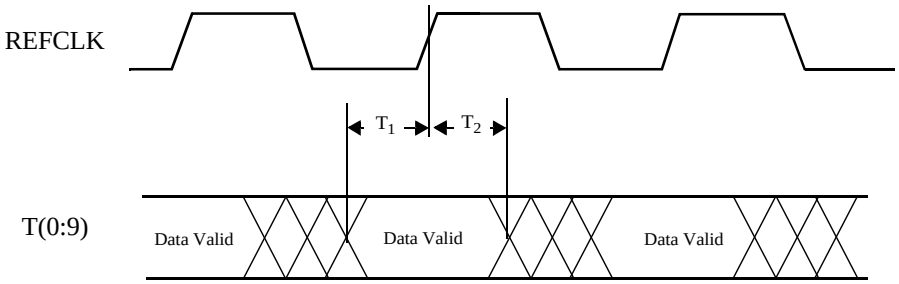

Table 2: Transmit AC Characteristics

Parameters	***Description***	***Min***	***Typ***	***Max***	***Units***	***Conditions***
T_1	T(0:9) Setup time to the rising edge of REFCLK	1.5	—	—	ns	Measured between the valid data level of T(0:9) to the 1.4V point of REFCLK
T_2	T(0:9) hold time after the rising edge of REFCLK	1.0	—	—	ns	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—	—	300	ps	20% to 80%, 50Ω load to V_{DD}- 2.0
T_{LAT}	Latency from rising edge of REFCLK to T0 appearing on TX+/TX-	8bc	—	8bc+ 4ns	ns	bc = bit clocks ns = nano second
Transmitter Output Jitter Allocation						
RJ	Random jitter (RMS)	—	5	8	ps	Measured at SO+/-, 1 sigma deviation of 50% crossing point.
DJ	Serial data output deterministic jitter (pk-pk)	—	30	80	ps	IEEE 802.3Z Clause 38.68, tested on a sample basis

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Figure 5: Receive Timing Waveforms

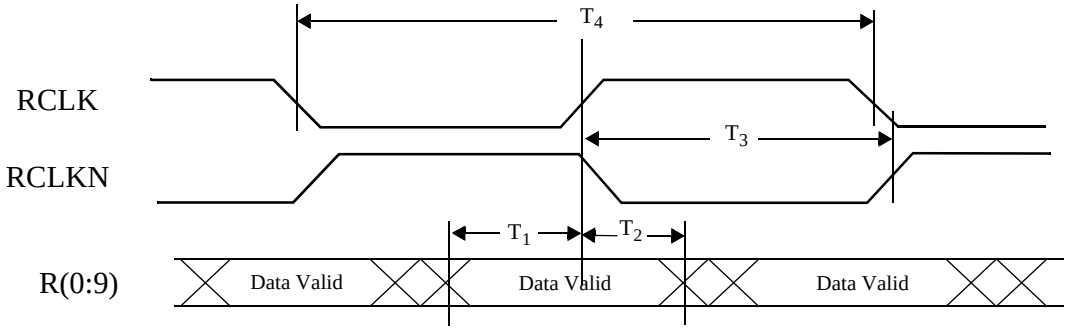

Table 3: Receive AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	TTL outputs valid prior to RCLK/RCLKN rise	4.0 3.0	— —	ns	@ 1.0625Gb/s @ 1.25Gb/s
T_2	TTL outputs valid after RCLK or RCLKN rise	3.0 2.0	— —	ns	@ 1.0625Gb/s @ 1.25Gb/s
T_3	Delay between rising edge of RCLK to rising edge of RCLKN	10 x T_{RX} –500	10 x T_{RX} +500	ps	T_{RX} is the bit period of the incoming data on Rx.
T_4	Period of RCLK and RCLKN	1.98 x T_{REFCLK}	2.02 x T_{REFCLK}	ps	Whether or not locked to serial data.
T_R, T_F	R(0:9), COMDET, SIGDET, RCLK and RCLKN rise and fall time	—	2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$, into 10pF load.
R_{LAT}	Latency from RX to R(0:9)	12 bc + 1 ns	13 bc + 9 ns	bc ns	bc = bit clock ns = nano second
T_{LOCK}(1)	Data acquisition lock time	—	1400	bc	8B/10B IDLE pattern, bc= bit clocks
Note: (1) Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH rev. 4.3.					

Figure 6: REFCLK Timing Waveforms

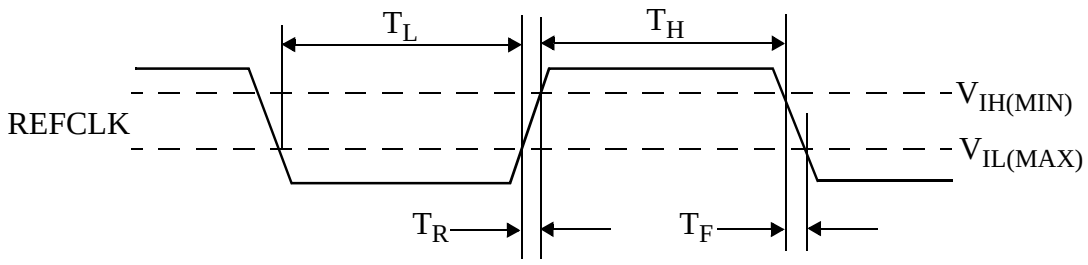

Table 4: Reference Clock Requirements

Parameter	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	98	136	MHz	Range over which both transmit and receive reference clocks on any link may be centered.
FO	Frequency Offset	–200	200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link
DC	REFCLK duty cycle	35	65	%	Measured at 1.5V.
T_R,T_F	REFCLK rise and fall time	—	1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.

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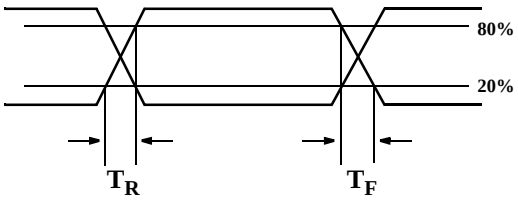
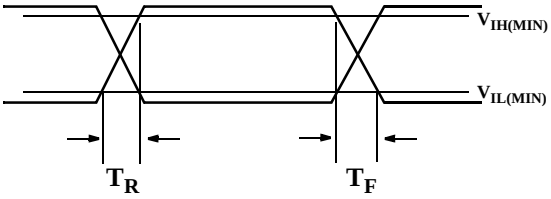
Figure 7: Parametric Measurement Information

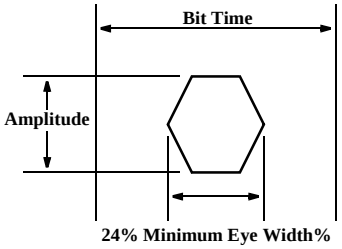
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

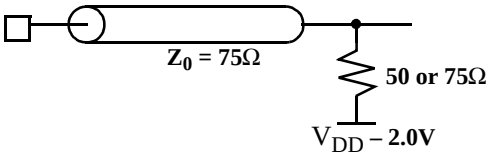


Receiver Input Eye Diagram Jitter Tolerance Mask

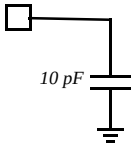


Parametric Test Load Circuit

Serial Output Load



TTL AC Output Load



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Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... –0.5V to +4V
DC Input Voltage (PECL inputs) ..... –0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to +5.5V
DC Output Voltage (TTL Outputs) ..... –0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... ±50mA
Output Current (PECL Outputs) ..... ±50mA
Case Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C

Note: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V ±5%
Operating Temperature Range ..... –40° Ambient to +95°C Case Temperature

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC7123 is rated to the following ESD voltages based on the human body and charge device models:

1. All pins are rated at or above 1000V (charge device model).
2. All pins are rated at or above 2000V (human body model).

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DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = –1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	5V Tolerant Inputs
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current (TTL)	—	—	–500	µA	V_{IN} = 0.5V
ΔV_{OUT75}(1)	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V (TX+) – (TX-)
ΔV_{OUT50}(1)	TX Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V (TX+) – (TX-)
ΔV_{IN}(1)	RX Input differential peak-to-peak input sensitivity	300	—	2600	mVp-p	Internally biased to V_{DD}/2 (RX+) – (RX-)
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	650	900	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current (all supplies)	—	190	260	mA	Outputs open, Case temp = 95°C, V_{DD} = V_{DD} max
I_{DDA}	Analog supply current	—	—	100	mA	V_{DDA} = V_{DDA} max

NOTE: (1) Refer to Application Note, AN-37, for differential measurement techniques.

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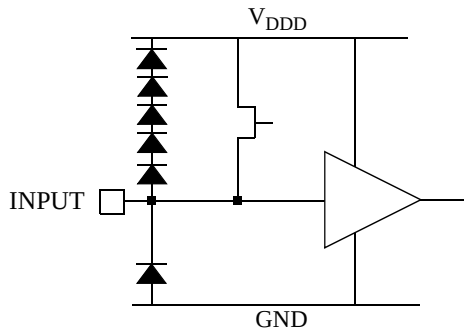
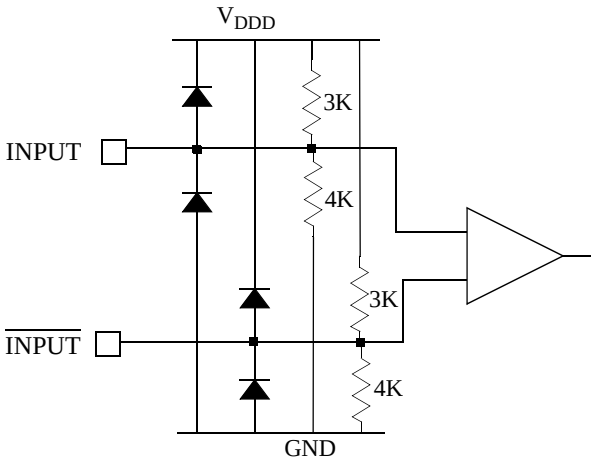
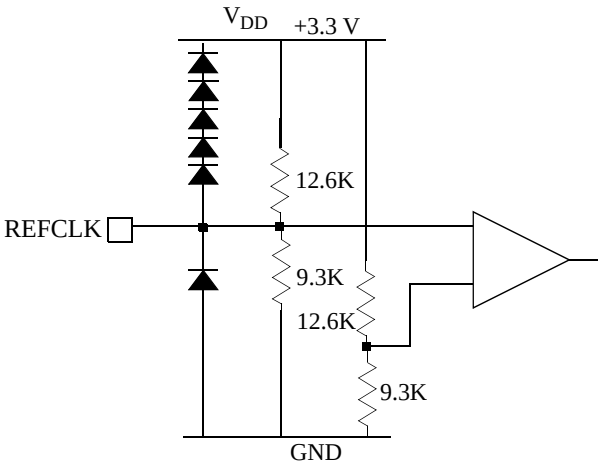
Figure 8: Input Structures



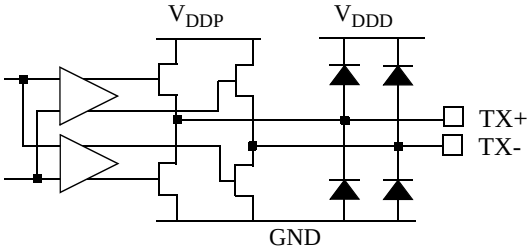
TTL Inputs (not REFCLK)



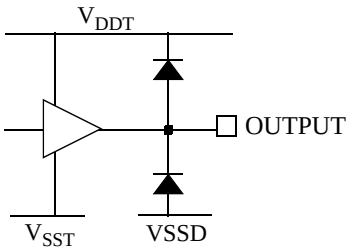
High-Speed Input (RX+/RX-)



REFCLK TTL Input



High-Speed Outputs (TX+/-)



TTL Outputs

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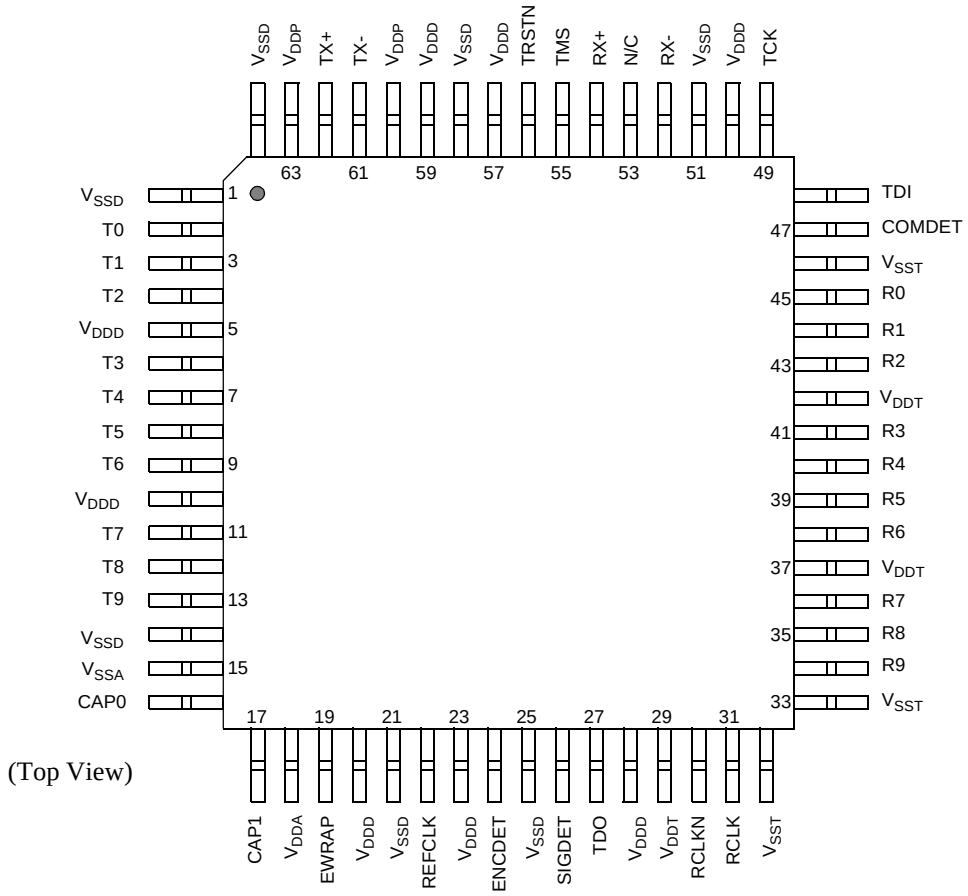
Package Pin Descriptions

Figure 9: Pin Diagram



(Top View)

Table 5: Pin Identification

Pin #	*Name*	*Description*
2,3,4,6,7,8,9 ,11,12,13	T0,T1,T2,T3 T4,T5,T6,T7 T8,T9	INPUTS - TTL: 10-Bit Transmit Character. Parallel data on this bus is clocked in on the rising edge of REFCLK. The data bit corresponding to T0 is transmitted first.
22	REFCLK	INPUT - TTL: This rising edge of this clock latches T(0:9) into the input register. It also provides the reference clock, at one tenth the baud rate to the PLL.
62, 61	TX+, TX-	OUTPUTS - Differential PECL (AC-coupling recommended): These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW.

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Pin #	*Name*	*Description*
45,44,43,41 40,39,38,36 35,34	R0,R1,R2,R3 R4,R5,R6,R7 R8,R9	OUTPUTS - TTL: 10-Bit Received Character. Parallel data on this bus is clocked out on the rising edges of RCLK and RCLKN. R0 is the first bit received on RX+/RX-.
19	EWRAP	INPUT - TTL: LOW for Normal Operation. When HIGH, an internal loop back path from the transmitter to the receiver is enabled and the TX outputs are held HIGH.
54, 52	RX+, RX-	INPUTS - Differential PECL (AC Coupling recommended): The serial receive data inputs selected when EWRAP is LOW. Internally biased to $V_{DD}/2$, with 3.3kΩ resistors from each input pin to V_{DD} and GND.
31, 30	RCLK, RCLKN	OUTPUT - Complementary TTL: Recovered clocks derived from $1/20^{th}$ of the RX+/- data stream. Each rising transition of RCLK or RCLKN corresponds to a new word on R(0:9).
24	ENCDET	INPUT - TTL Enables COMDET and word resynchronization when HIGH. When LOW, maintains current word alignment and disables COMDET.
47	COMDET	OUTPUT - TTL: This output goes HIGH for half of an RCLK period to indicate that R(0:9) contains a Comma Character (‘0011111XXX’). COMDET will go HIGH only during a cycle when RCLKN is rising. COMDET is enabled by ENCDET being HIGH.
26	SIGDET	OUTPUT - TTL: SIGnal DETect. This output goes HIGH when the RX input contains a valid Fibre Channel or Gigabit Ethernet signal. A LOW indicates an invalid signal.
16, 17	CAP0, CAP1	ANALOG: Differential capacitor for the CMU’s VCO. 0.1 µF nominal.
49	TCK	INPUT - TTL: JTAG clock input. Not normally connected.
48	TDI	INPUT - TTL: JTAG data input. Not normally connected.
55	TMS	INPUT - TTL: JTAG mode select input. Normally tied to V_{DDD}
56	TRSTN	INPUT - TLL: JTAG reset input. Tie to V_{SSD} for normal operation.
27	TDO	OUTPU - TTL: JTAG data output. Normally tri-stated.
18	VDDA	Analog Power Supply
15	VSSA	Analog Ground
5,10,20,23 28,50,57,59	VDDD	Digital Logic Power Supply
1,14,21,25 51,58,64	VSSD	Digital Logic Ground
29, 37, 42	VDDT	TTL Output Power Supply
32, 33, 46	VSST	TTL Output Ground
60,63	VDDP	PECL I/O Power Supply
53	N/C	No internal connection

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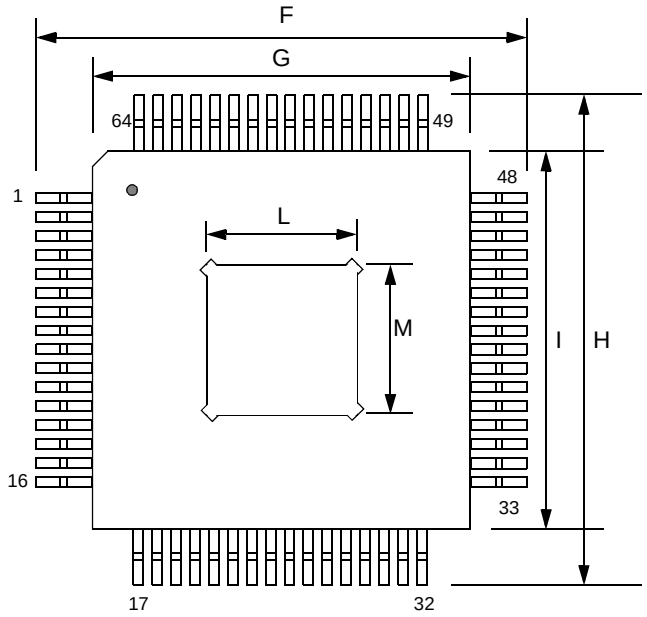
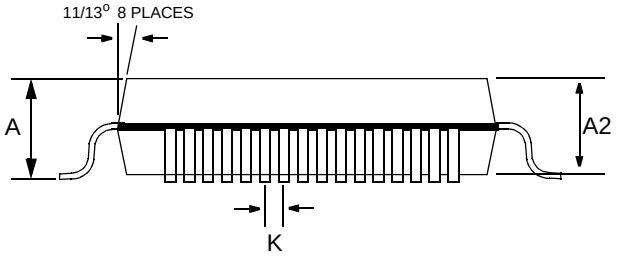
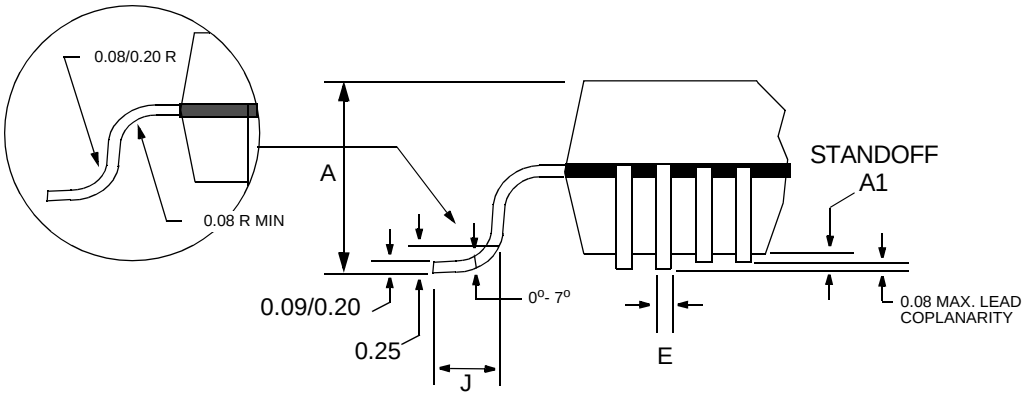
Package Information: 64-pin TQFP



Item	10 mm	Tolerance
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	12.00	BASIC
G	10.00	BASIC
H	12.00	BASIC
I	10.00	BASIC
J	0.60	±0.15
K	0.50	BASIC
L	3.80	BASIC
M	3.80	BASIC





NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.

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Package Thermal Considerations

The VSC7123 ETR is packaged in a 10mm cavity-down, exposed pad TQFP. This package uses an industry-standard EIAJ footprint, which has been enhanced to improve thermal dissipation. The construction of the package is shown in Figure 10.

Figure 10: TQFP Package Cross Section

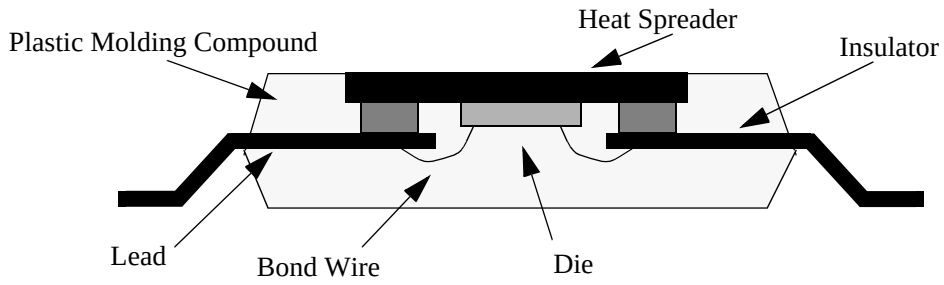

Table 6: Thermal Resistance

Symbol	*Description*	*10mm TQFP*	*Units*
θ_{jc}	Thermal resistance from junction-to-case	7.0	^{o}C/W
θ_{ca}	Thermal resistance from case-to-ambient in still air including conduction through the leads.	40	^{o}C/W
θ_{ca-100}	Thermal resistance from case-to-ambient with 100 LFM airflow	38	^{o}C/W
θ_{ca-200}	Thermal resistance from case-to-ambient with 200 LFM airflow	35	^{o}C/W
θ_{ca-400}	Thermal resistance from case-to-ambient with 400 LFM airflow	33	^{o}C/W
θ_{ca-600}	Thermal resistance from case-to-ambient with 600 LFM airflow	30	^{o}C/W

The VSC7123 ETR is designed to operate with a case temperature up to 95^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown in Table 6, the TQFP package can operate in a still air ambient temperature of 59^{o}C [59^{o}C = 95^{o}C - 0.9W * 40^{o}C/W]. If the ambient air temperature exceeds these limits, then some form of cooling through a heatsink or an increase in airflow must be provided.

Moisture Sensitivity Level

This device is rated at with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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Ordering Information

The part number for this product is formed by a combination of the device type and the package style.

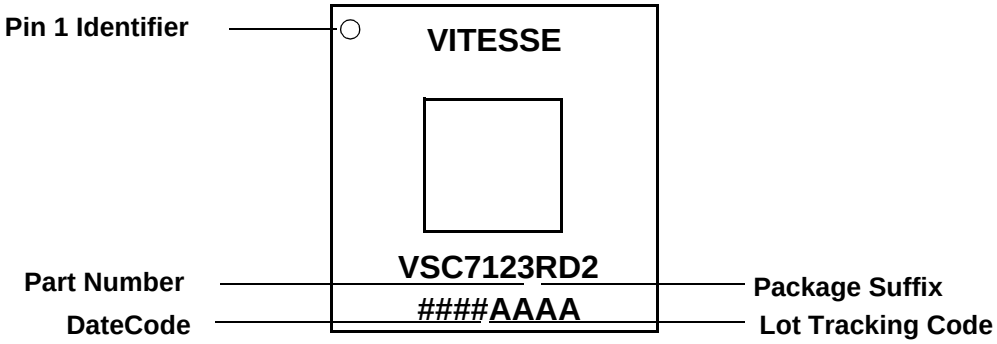
VSC7123 RD 2

- **Device Type**: 10-Bit Transceiver
- **Package**: RD: 64-Pin, 10x10mm TQFP
- Extended Temperature Range (–40°)

Marking Information

The package is marked with three lines of text as shown in Figure 11.

Figure 11: Package Marking Information



Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this data sheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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Revision History

Changes from Rev 1.0 to 1.1

Revised Table 1 on page 4.

Changes from Rev 1.1 to 2.0

Initial Release.

6/29/00 Rev 2.0 to 2.1

Added “case temperature = 95°C” to IDD condition in DC Characteristics table.

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