V53C8129H
ULTRA-HIGH PERFORMANCE, 128K X 8 EDO PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	35	40	45	50
Max. $\overline{RAS}$ Access Time, (t_{RAC})	35 ns	40 ns	45 ns	50 ns
Max. Column Address Access Time, (t_{CAA})	18 ns	20 ns	22 ns	24 ns
Min. Fast Page Mode With EDO Cycle Time, (t_{PC})	14 ns	15 ns	17 ns	19 ns
Min. Read/Write Cycle Time, (t_{RC})	70 ns	75 ns	80 ns	90 ns

Features

- 128K x 8-bit organization
- $\overline{RAS}$ access time: 35, 40, 45, 50 ns
- EDO Page Mode supports sustained I/O data rates up to 71.5 MHz
- Low power dissipation
  - V53C8129H-50
    - — Operating Current: 135 mA max
    - — TTL Standby Current: 2.0 mA max
- Low CMOS Standby Current: 1.0 mA max
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval: 512 cycles/8 ms
- Available in 26/24 pin 300 mil SOJ package

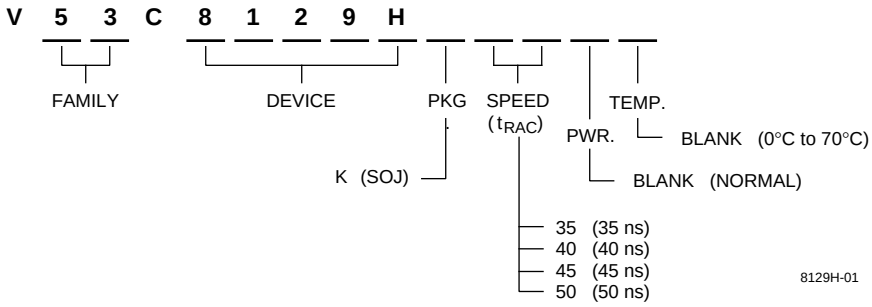
Description

The V53C8129H is a high speed 131,072 x 8 bit CMOS dynamic random access memory. The V53C8129H offers a combination of features: EDO Page Mode for high data bandwidth, fast usable speed, CMOS standby current.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Page Mode with extended data out operation allows random access of up to 256 columns (x8) bits within a row with cycle times as short as 14 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8129H ideally suited for graphics, digital signal processing and high performance peripherals.

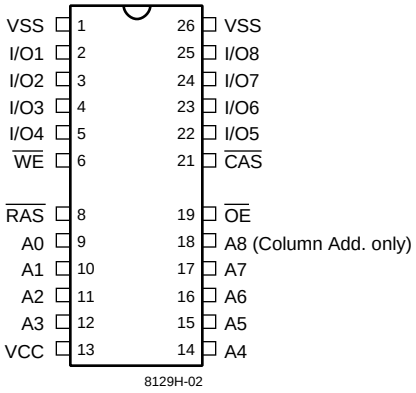
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)				Power	Temperature Mark
	K	35	40	45	50	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
SOJ	K	26/24

26/24 Lead SOJ PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs (A_8: Column Address only)
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
I/O_1–I/O_8	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) ..... –55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

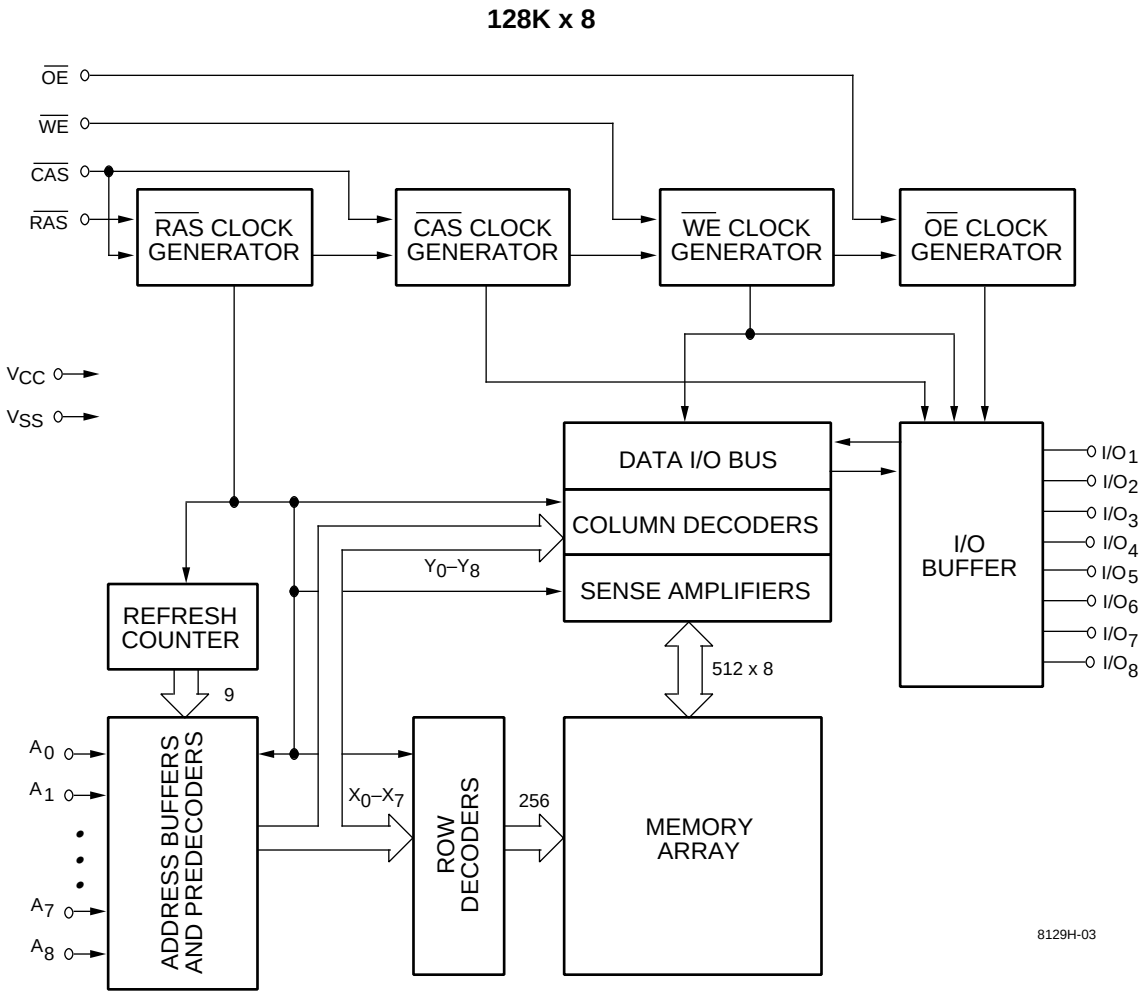
*Capacitance**

T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

*** Note:** Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C8129H			Unit	Test Conditions	Notes
			Min.	Typ.	Max..			
I_{LI}	Input Leakage Current (any input pin)		–10		10	µA	$V_{SS} \le V_{IN} \le V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	35			160	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		40			150			
		45			145			
		50			135			
I_{CC2}	V_{CC} Supply Current, TTL Standby				4	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	35			160	mA	$t_{RC} = t_{RC}$ (min.)	2
		40			150			
		45			145			
		50			135			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	35			95	mA	Minimum cycle	1, 2
		40			90			
		45			85			
		50			80			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				2	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$ other inputs ≥ V_{SS}	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V, All other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{CC} + 1	V		3
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	35	75K	40	75K	45	75K	50	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	70		75		80		90		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25		25		25		30		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	35		40		45		50		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	7		8		9		9		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	16	23	17	28	18	32	19	36	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	6		7		8		9		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	4		5		6		7		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8		9		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		12		13		14	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$ (EDO)		12		12		13		14	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		35		40		45		50	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		18		20		22		24	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	Output buffer turn-off delay time	0	6	0	6	0	7	0	8	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	28		30		35		40		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	17	12	20	13	23	14	26	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	12		12		13		14		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	12		12		13		14		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	5		5		6		7		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	5		5		6		7		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	28		30		35		40		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12		12		13		14		ns	

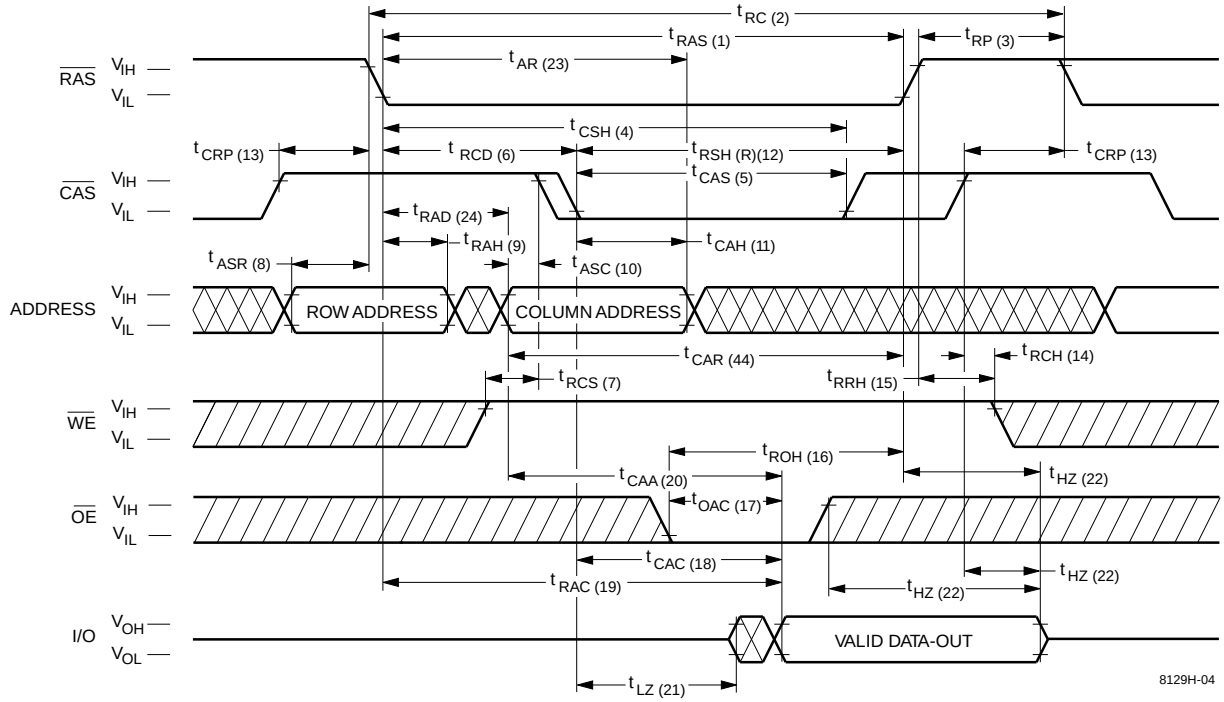
AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	4		5		6		7		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	5		6		7		8		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	5		6		7		8		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	105		110		115		130		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	70		75		80		87		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	28		30		32		34		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	54		58		62		68		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	46		48		50		52		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	35		38		41		42		ns	12
42	t_{CL2CL2}	t_{PC}	EDO Page Mode Read or Write Cycle Time	14		15		17		19		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	4		5		6		7		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	18		20		22		24		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		21		23		25		27	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	28		30		35		40		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	8		8		10		12		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	58		60		65		70		ns	
51	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
52		t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	
53		t_{COH}	Output Hold After $\overline{CAS}$ Low	5		5		5		5		ns	

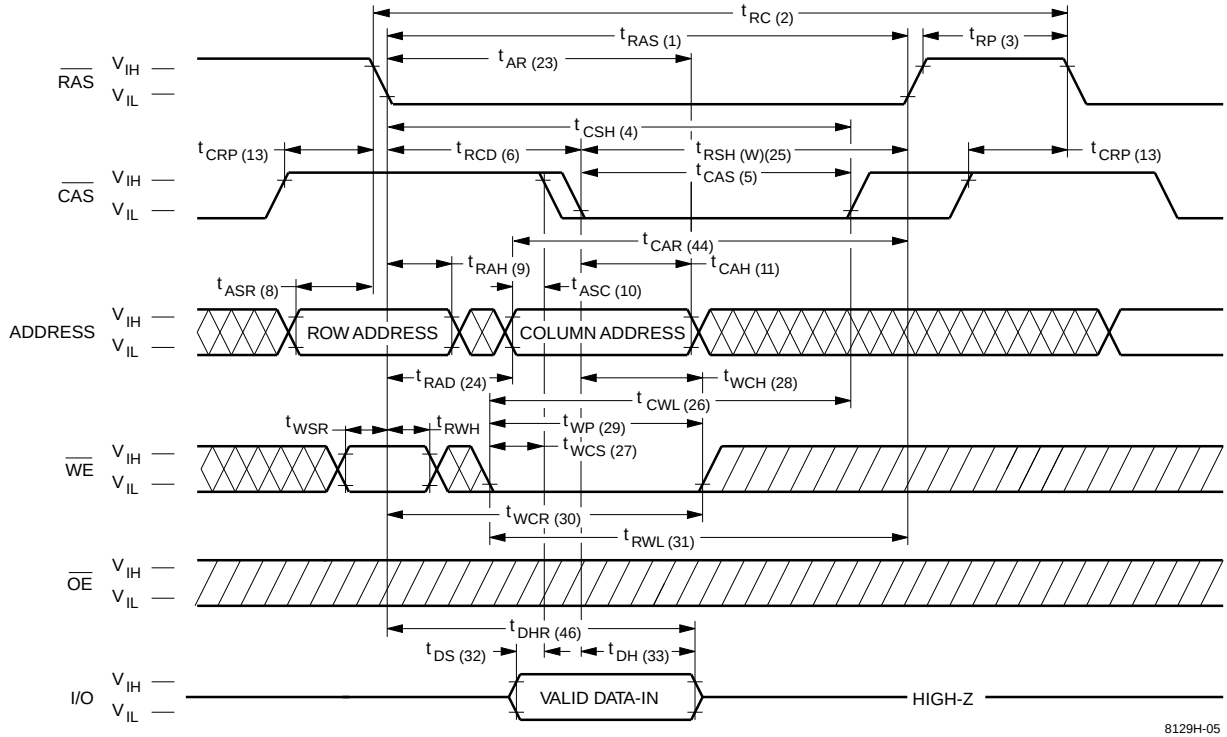
Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 3 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle

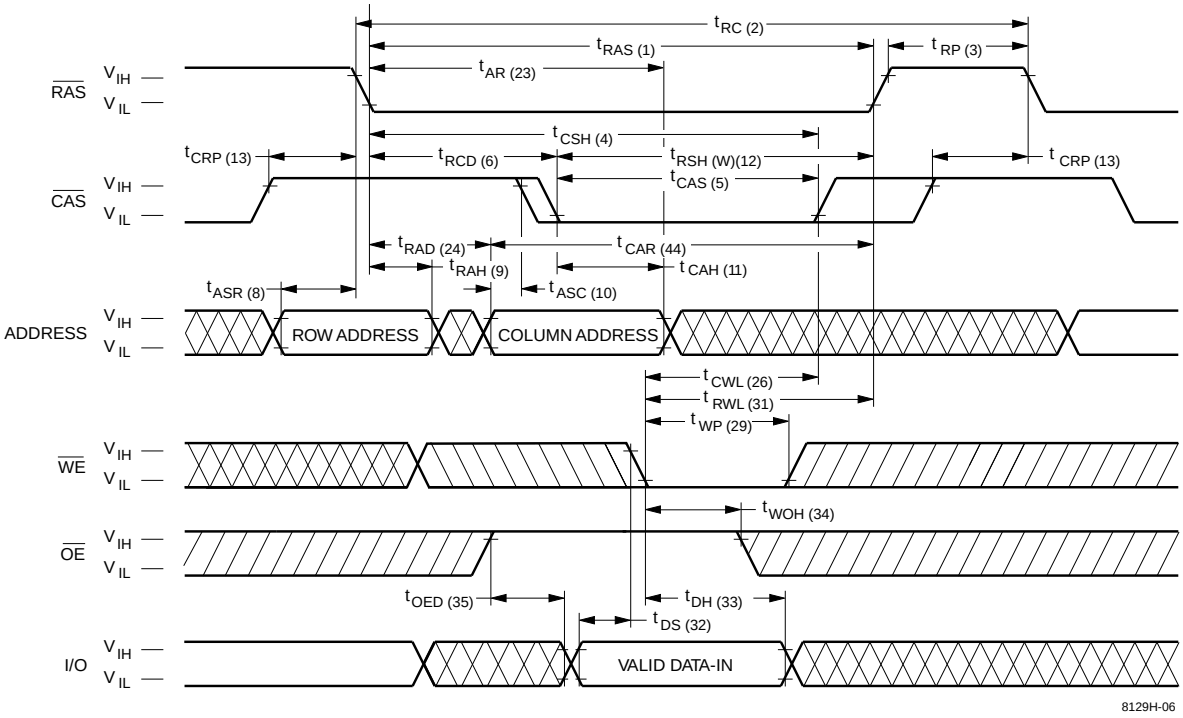


Waveforms of Early Write Cycle

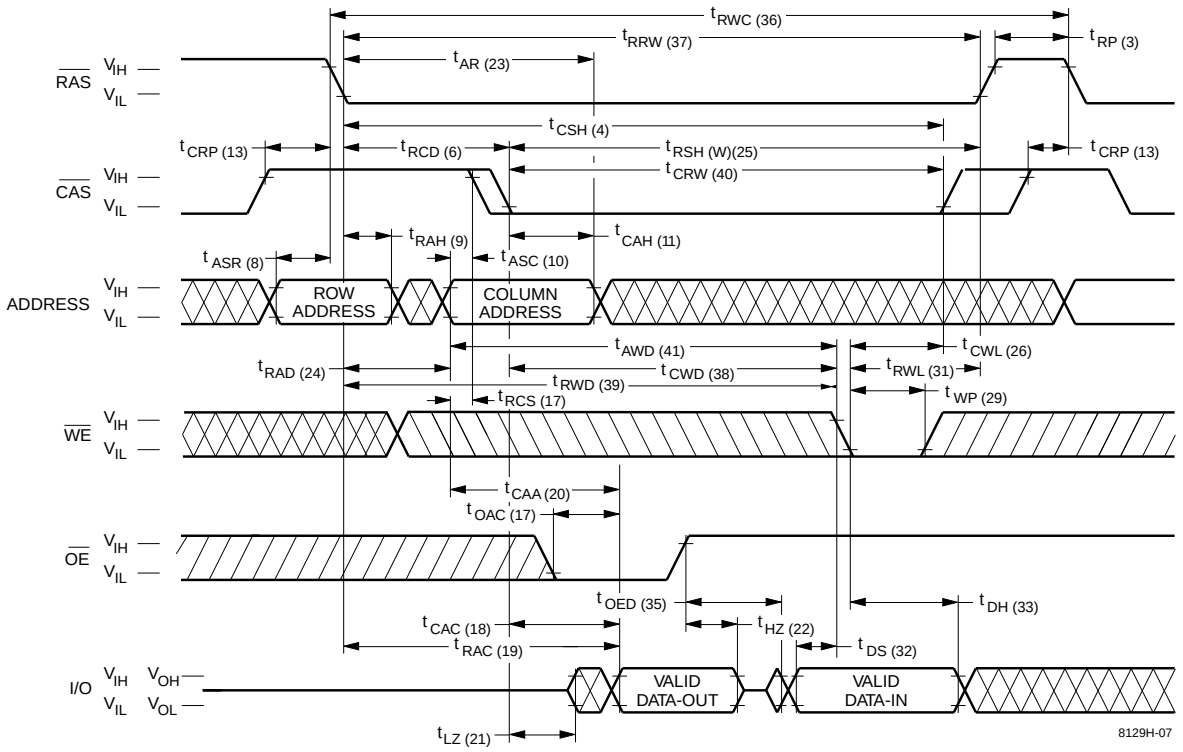


Don't Care Undefined

Waveforms of $\overline{OE}$-Controlled Write Cycle

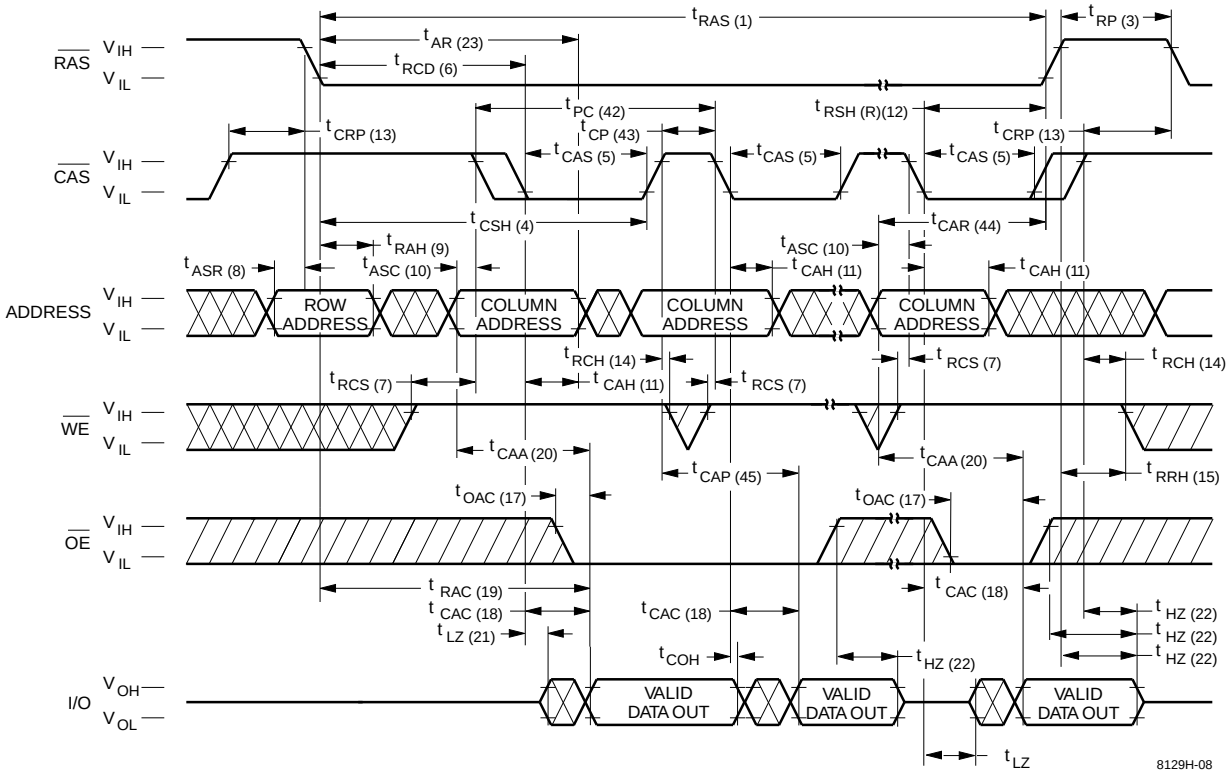


Waveforms of Read-Modify-Write Cycle

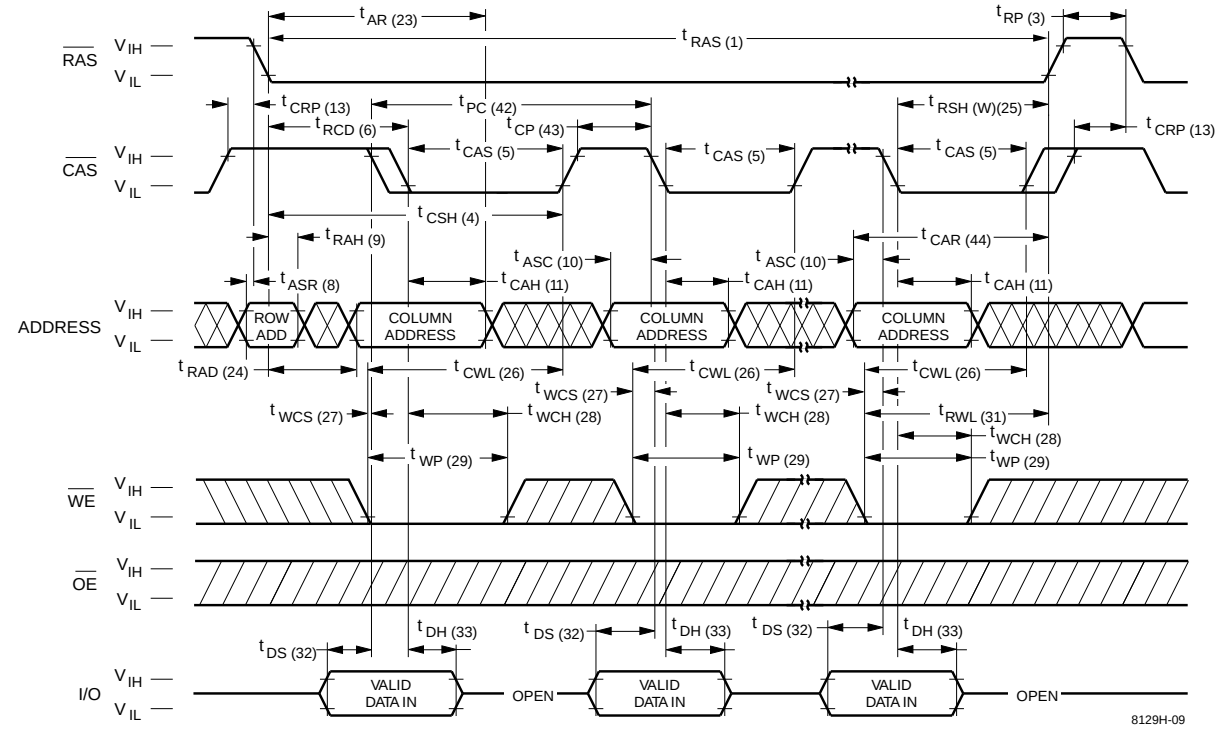


Don't Care Undefined

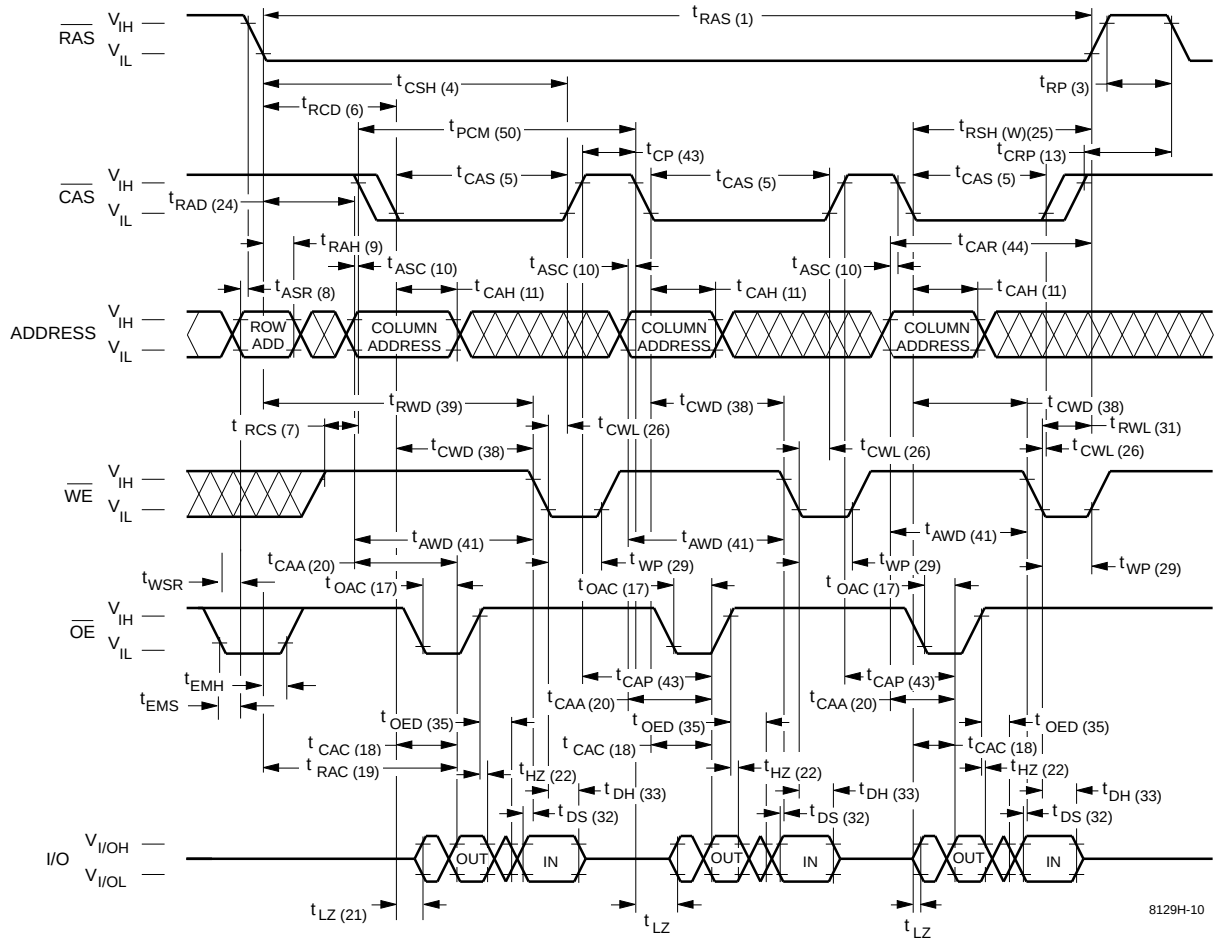
Waveforms of EDO Page Mode Read Cycle



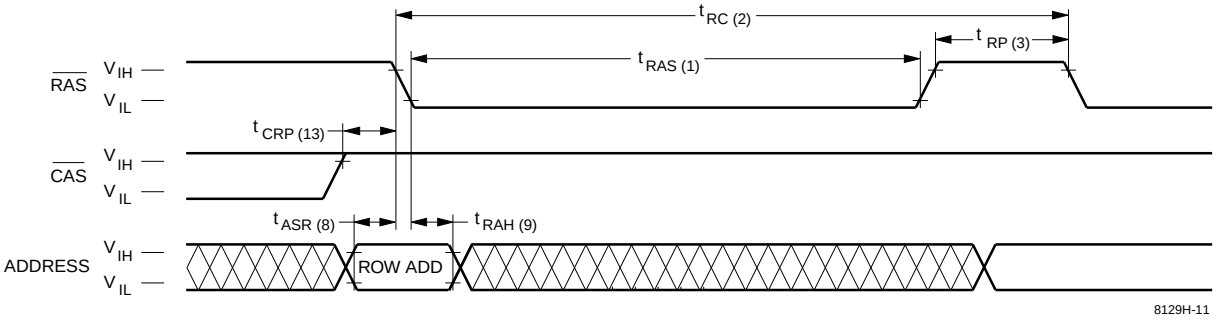
Waveforms of EDO Page Mode Write Cycle



Waveforms of EDO Page Mode Read-Write Cycle



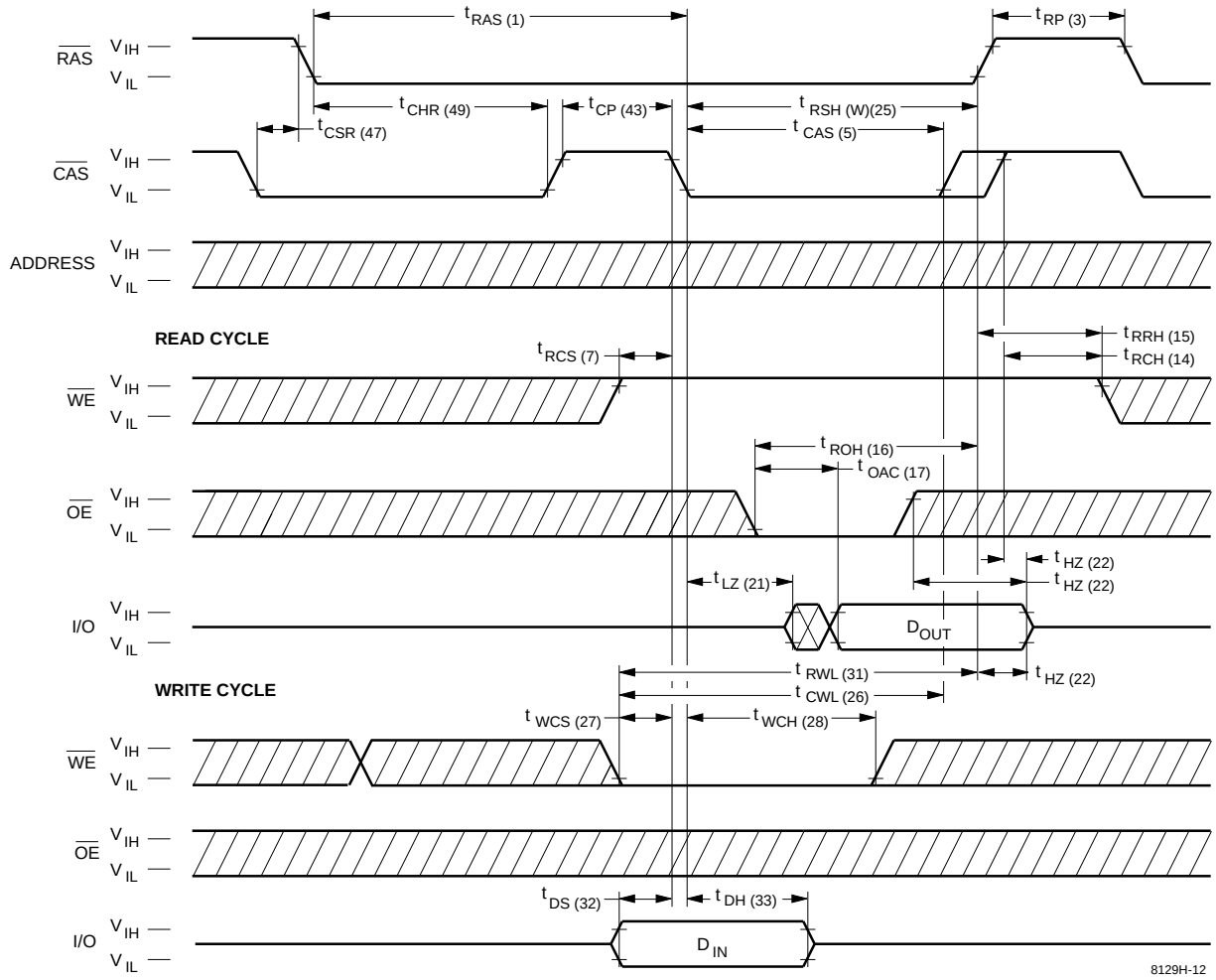
Waveforms of $\overline{RAS}$-Only Refresh Cycle



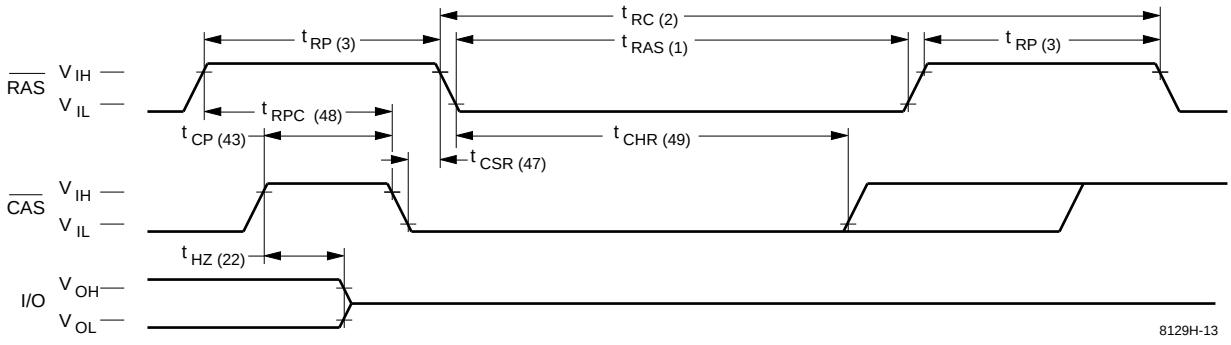
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Don't Care Undefined

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



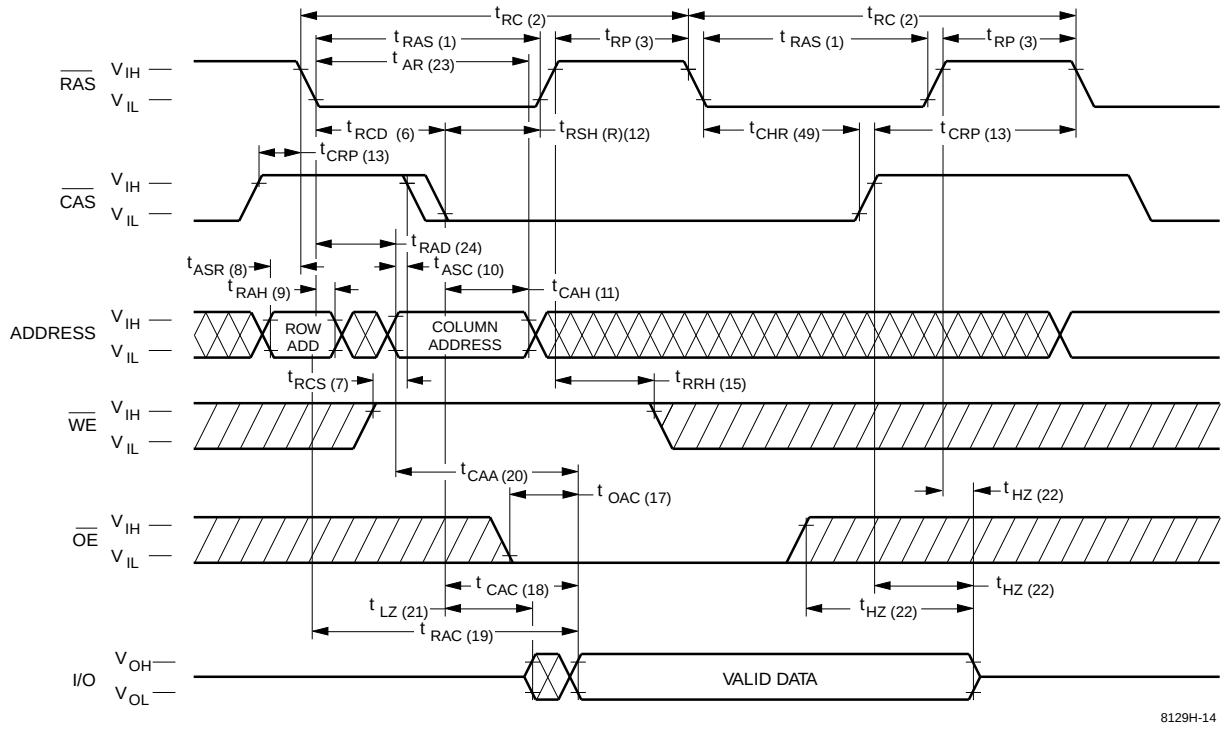
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



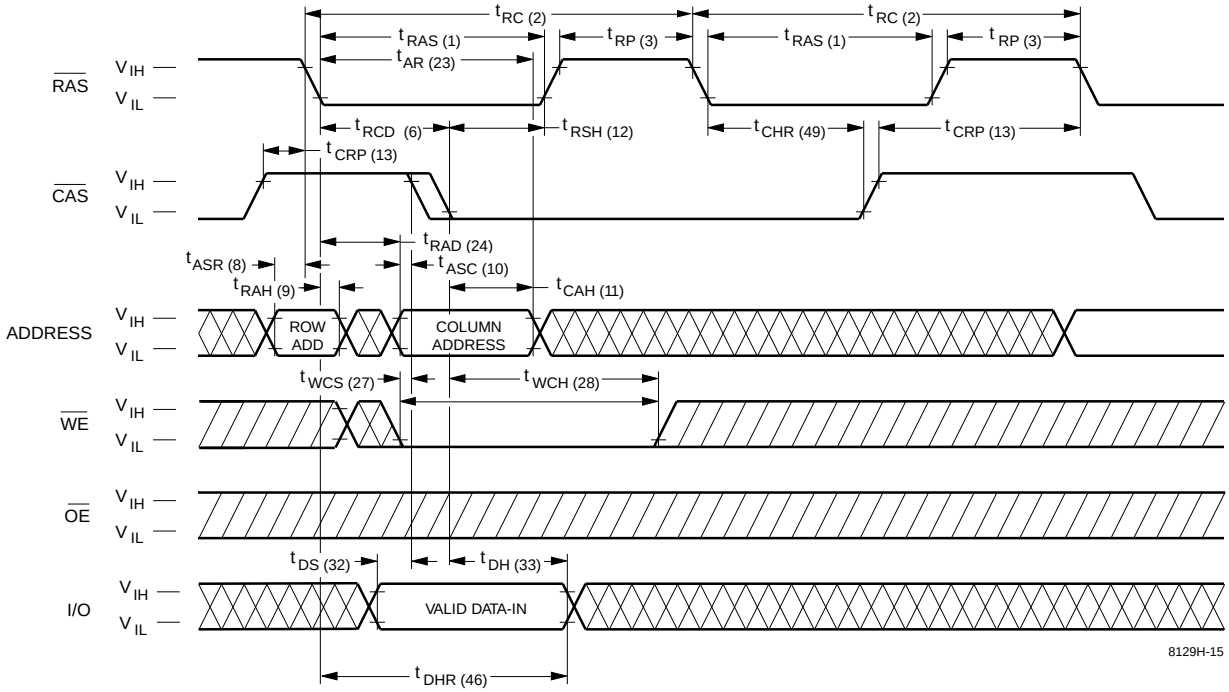
NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

Don't Care Undefined

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Don't Care Undefined

Functional Description

The V53C8129H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8129H reads and writes data by multiplexing an 17-bit address into a 8-bit row and an 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C8129H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Extended Data Out Page Mode

The V53C8129H offers fast access within a row. Unlike ordinary fast page mode DRAM, the V53C8129H output remains active and valid even after $\overline{CAS}$ goes high and it will stay valid for 5ns after $\overline{CAS}$ changes low. The feature allows the V53C8129H to $\overline{CAS}$ cycle faster than ordinary page mode DRAM since the cycle time be short as data access time.

The outputs are disabled at the tHZ time after $\overline{RAS}$ and $\overline{CAS}$ are high. The tHZ time is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$ whichever occurs last. In addition, high on $\overline{OE}$ input and activation of the write-cycle will also disable the outputs.

The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 \times t_{PC}}$$

Data Output Operation

The V53C8129H Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

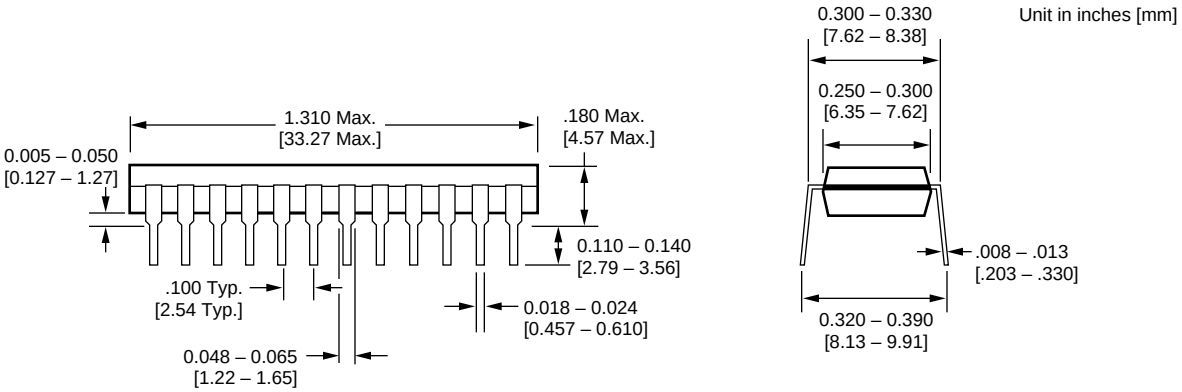
During Power-On, the V_{CC} current requirement of the V53C8129H is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C8129H Data Output
Operation for Various Cycle Types

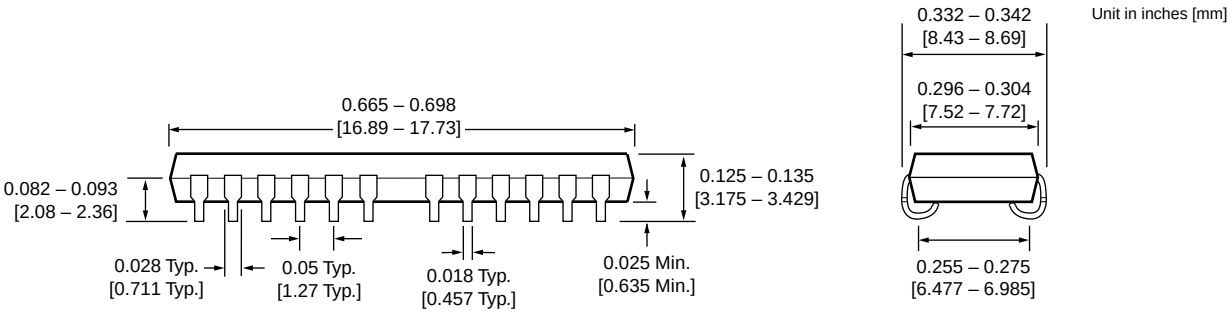
Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Page Mode Read	Data from Addressed Memory Cell
EDO Page Mode Write Cycle (Early Write)	High-Z
EDO Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

Package Outlines

24-pin 300 mil PDIP



26/24-pin 300 mil SOJ



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