64 Mbit DDR SDRAM
4M X 16, 3.3VOLT

	36	4	5
System Frequency (f_{CK})	275 MHz	250 MHz	200 MHz
Clock Cycle Time (t_{CK3})	3.6 ns	4 ns	5 ns
Clock Cycle Time ($t_{CK2.5}$)	4.3ns	4.8 ns	6 ns
Clock Cycle Time (t_{CK2})	5.4ns	6 ns	7.5 ns

Features

- 4 banks x 1Mbit x 16 organization
- High speed data transfer rates with system frequency up to 275 MHz
- Data Mask for Write Control (DM)
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 2.5, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  2, 4, 8 for Sequential Type
  2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Suspend Mode and Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 66-pin 400 mil TSOP-II
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQs) for input and output data, active on both edges
- On-Chip DLL aligns DQ and DQs transitions with CLK transitions
- Differential clock inputs CLK and $\overline{CLK}$
- Power supply 3.3V ± 0.3V
- VDDQ (I/O) power supply 2.5 ± 0.2V

Description

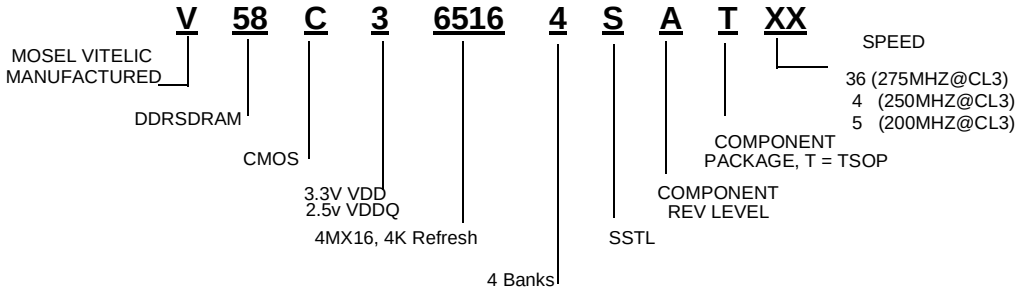
The V58C365164S is a four bank DDR DRAM organized as 4 banks x 1Mbit x 16. The V58C365164S achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock

All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.

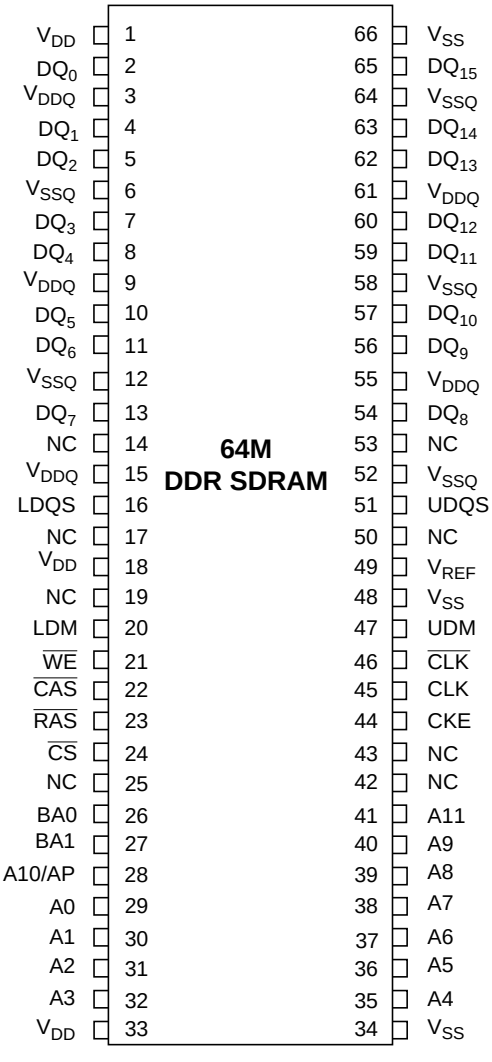
Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

Device Usage Chart

Operating Temperature Range	Package Outline	CLK Cycle Time (ns)			Power		Temperature Mark
	JEDEC 66 TSOP II	-36	-4	-5	Std.	L	
0°C to 70°C	•	•	•	•	•	•	Blank



66 Pin Plastic TSOP-II PIN CONFIGURATION Top View



Pin Names

CLK, $\overline{CLK}$	Differential Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
UDQS, LDQS	Data Strobe (Bidirectional)
A_0–A_{11}	Address Inputs
BA0, BA1	Bank Select
DQ_0–DQ_{15}	Data Input/Output
UDM, LDM	Data Mask
V_{DD}	Power (+3.3V)
V_{SS}	Ground
V_{DDQ}	Power for I/O's (+2.5V)
V_{SSQ}	Ground for I/O's
NC	Not connected
V_{REF}	Reference Voltage for Inputs

*Capacitance**

T_A = 0 to 70°C, V_{CC} = 3.3 V ± 0.2 V, f = 1 Mhz

Symbol	Parameter	Max.	Unit
C_{I1}	Input Capacitance (A0 to A11)	5	pF
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE	5	pF
C_{IO}	Output Capacitance (DQ)	6.5	pF
C_{CLK}	Input Capacitance (CCLK, $\overline{CLK}$)	4	pF

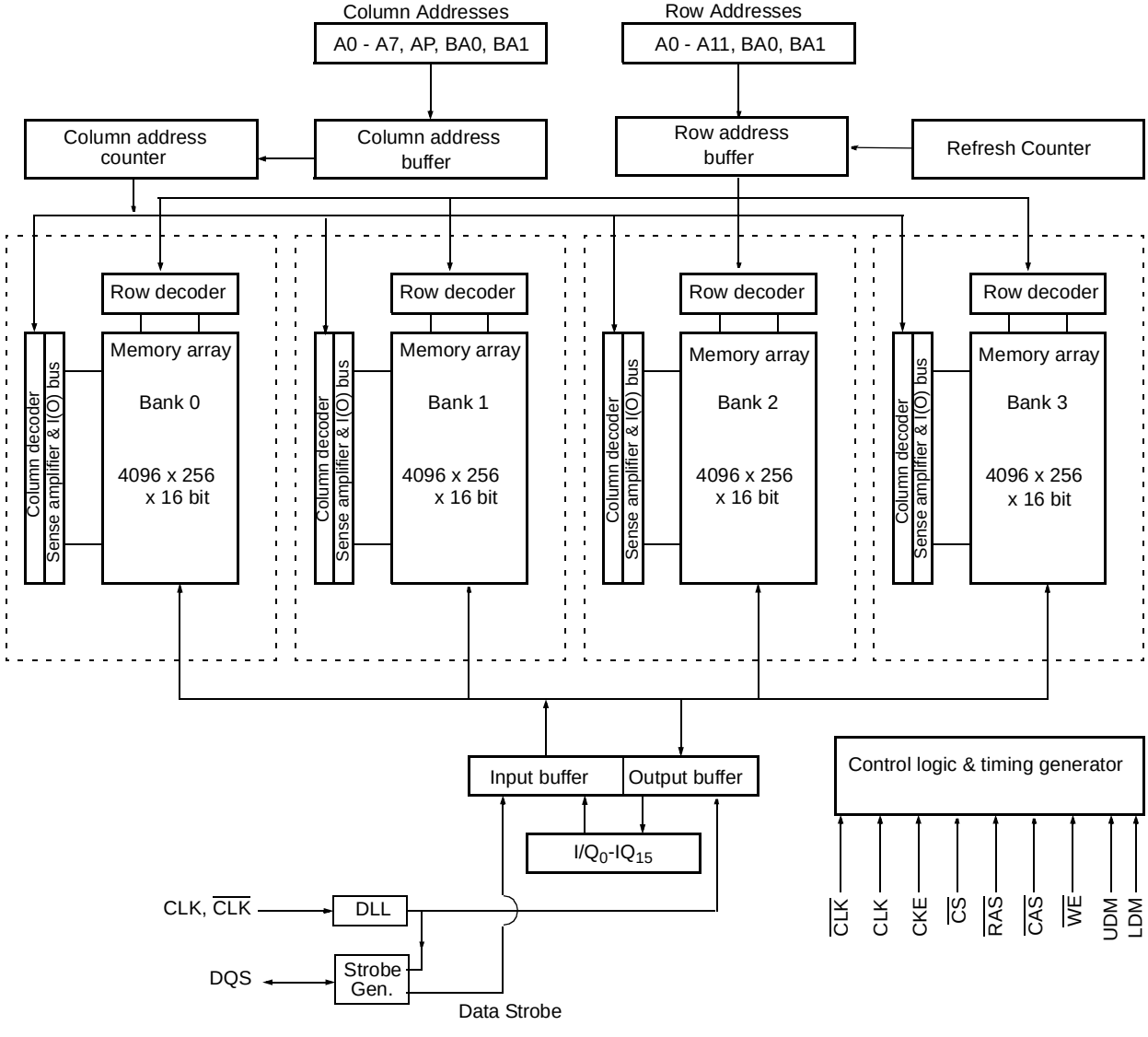
***Note:** Capacitance is sampled and not 100% tested.

*Absolute Maximum Ratings**

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Input/output voltage ..... -0.3 to (V_{CC}+0.3) V
Power supply voltage ..... -0.3 to 4.6 V
Power dissipation ..... 2.0 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK $\overline{CLK}$	Input	Pulse	Positive Edge	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CLK.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
DQS	Input/ Output	Pulse	Active High	Active on both edges for data input and output. Center aligned to input data Edge aligned to output data
A0 - A11	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization: 8M x 8 SDRAM CAn = CA8 (Page Length = 512 bits) In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input/ Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DM	Input	Pulse	Active High	In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high.
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Input	Level	—	SSTL Reference Voltage for Inputs

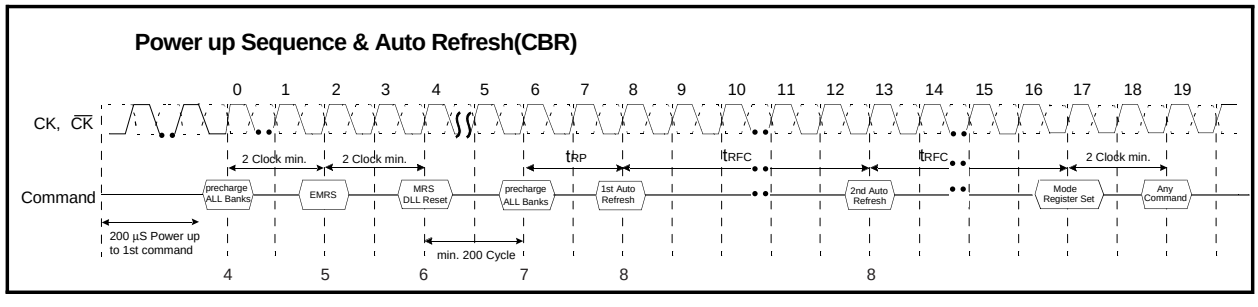
Functional Description

■ Power-Up Sequence

The following sequence is required for POWER UP.

1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock (CLK, $\overline{CLK}$), apply NOP & take CKE high.
4. Precharge all banks.
5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command to initialize device operation.

Note1 Every "DLL enable" command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.



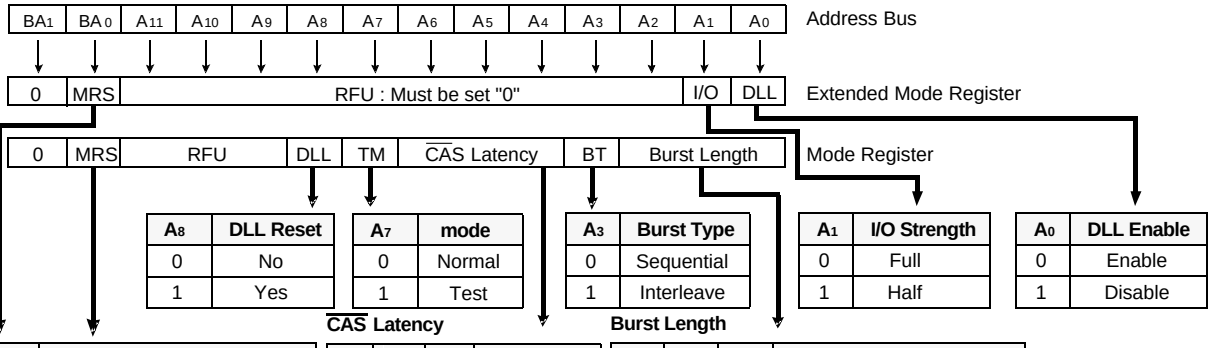
Extended Mode Register Set (EMRS)

The extended mode register stores the data for enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA_0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A_0 ~ A_{11} and BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A_0 is used for DLL enable or disable. "High" on BA_0 is used for EMRS. All the other address pins except A_0 and BA_0 must be set to low for proper EMRS operation. A_1 is used at EMRS to indicate I/O strength A_1 = 0 full strength, A_1 = 1 half strength. Refer to the table for specific codes.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for a variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA_0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 low is written in the mode register. Two clock cycles are required to meet t_{MRD} spec. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, $\overline{CAS}$ latency (read latency from column address) uses A_4 ~ A_6. A_7 is a Mosel Vitelic specific test mode during production test. A_8 is used for DLL reset. A_7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.

1. MRS can be issued only at all banks precharge state.
2. Minimum tRP is required to issue MRS command.



A_8	DLL Reset
0	No
1	Yes

A_7	mode
0	Normal
1	Test

A_3	Burst Type
0	Sequential
1	Interleave

A_1	I/O Strength
0	Full
1	Half

A_0	DLL Enable
0	Enable
1	Disable

BA_0	A_n ~ A_0
0	(Existing)MRS Cycle
1	Extended Funtions(EMRS)

* RFU(Reserved for future use) should stay "0" during MRS cycle.

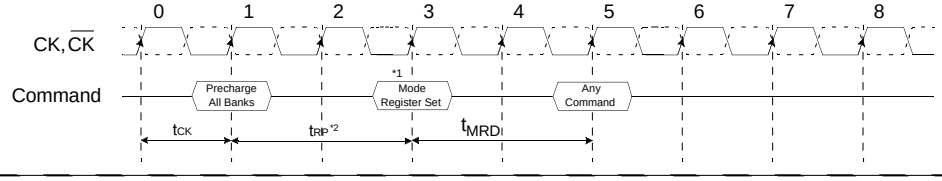
$\overline{CAS}$ Latency

A_6	A_5	A_4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	2.5
1	1	1	Reserve

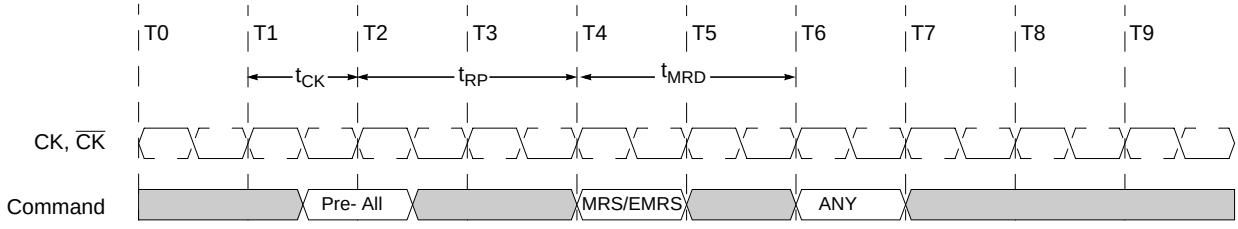
Burst Length

A_2	A_1	A_0	Latency	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

Mode Register Set



Mode Register Set Timing



Mode Register set (MRS) or Extended Mode Register Set (EMRS) can be issued only when all banks are in the idle state.

If a MRS command is issued to reset the DLL, then an additional 200 clocks must occur prior to issuing any new command to allow time for the DLL to lock onto the clock.

Burst Mode Operation

Burst Mode Operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits A_0—A_3 during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

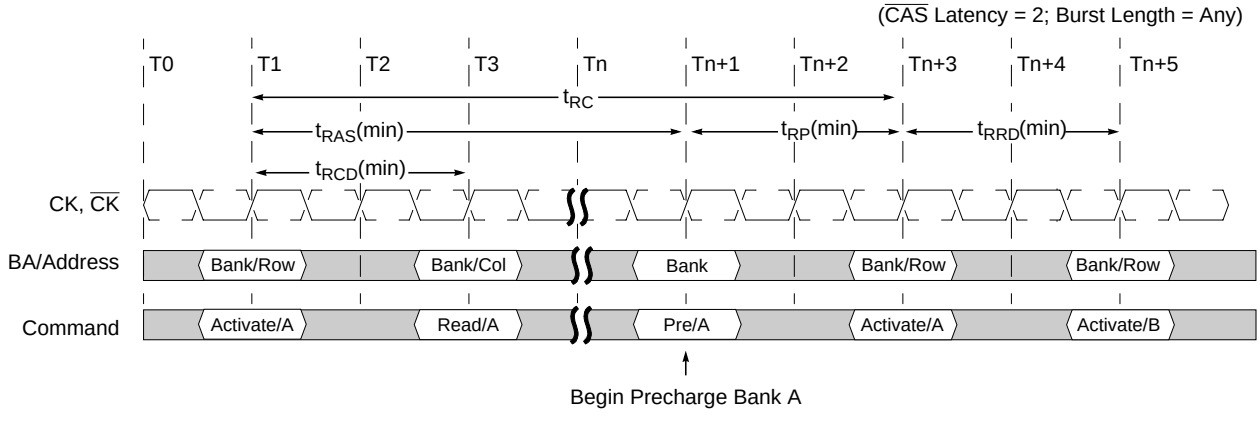
Burst Length and Sequence

Burst Length	Starting Length (A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0,1, 2, 3, 4, 5, 6, 7	0,1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5, 6	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses (BA_0 and BA_1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Timing



Read Operation

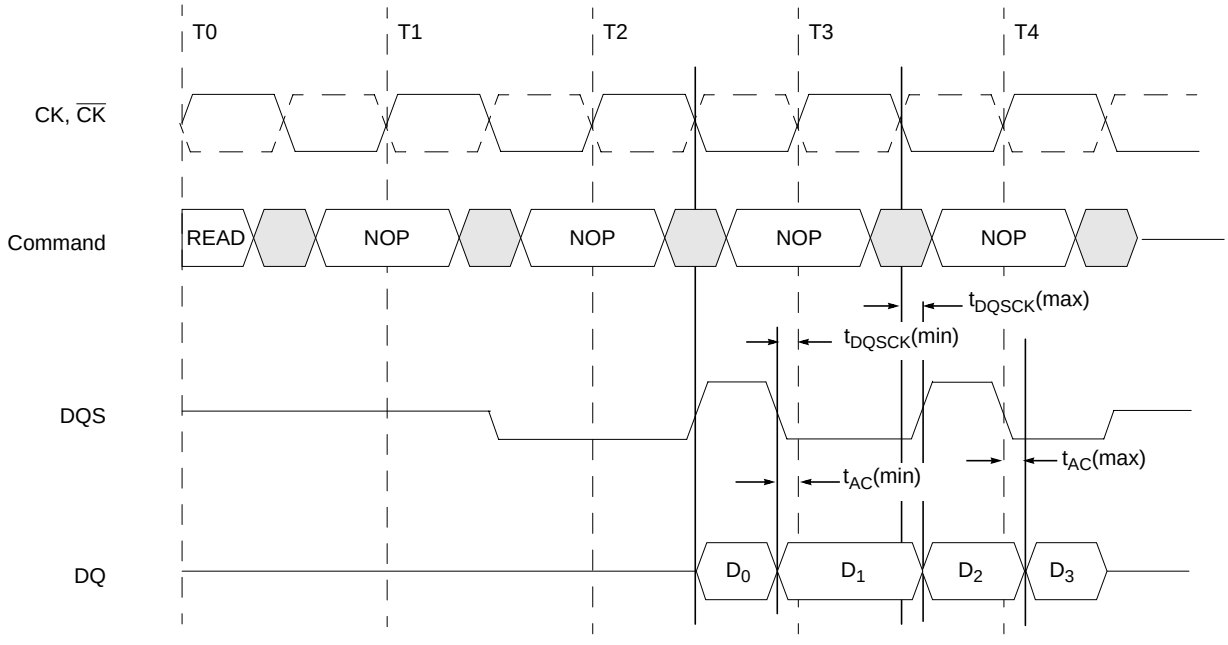
With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation.

The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input differential clock (CK, $\overline{CK}$) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned.

Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ (t_{DQSQ}) is tighter than that possible for CK to DQ (t_{AC}) or DQS to CK (t_{DQSCK}).

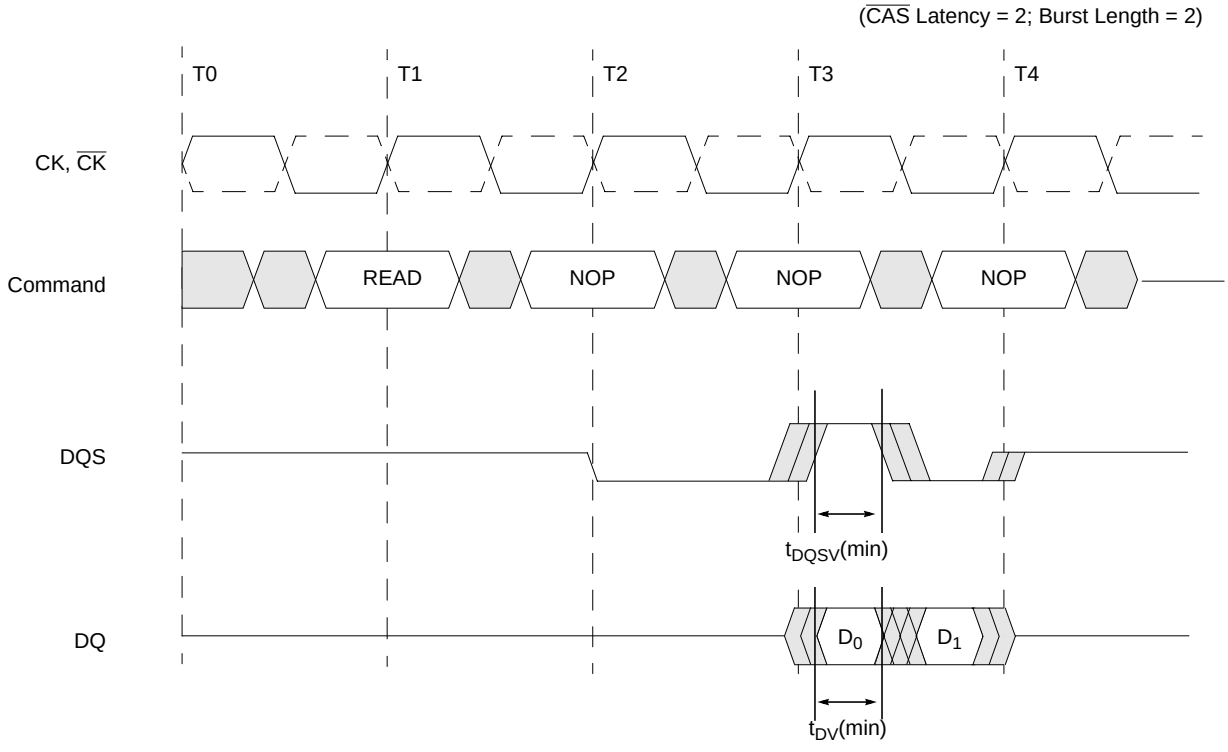
Output Data (DQ) and Data Strobe (DQS) Timing Relative to the Clock (CK) During Read Cycles

($\overline{CAS}$ Latency = 2.5; Burst Length = 4)



The minimum time during which the output data (DQ) is valid is critical for the receiving device (i.e., a memory controller device). This also applies to the data strobe during the read cycle since it is tightly coupled to the output data. The minimum data output valid time (t_{DV}) and minimum data strobe valid time (t_{DQSV}) are derived from the minimum clock high/low time minus a margin for variation in data access and hold time due to DLL jitter and power supply noise.

Output Data and Data Strobe Valid Window for DDR Read Cycles



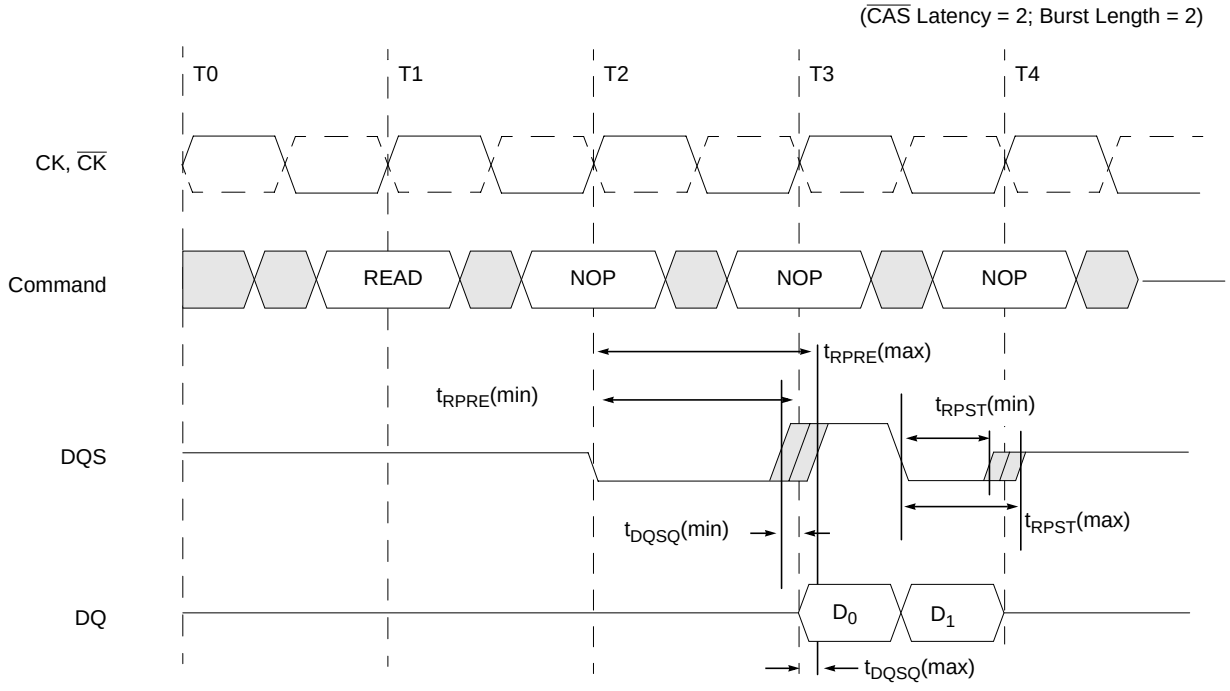
Read Preamble and Postamble Operation

Prior to a burst of read data and given that the controller is not currently in burst read mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. The is referred to as the data strobe “read preamble” (t_{RPRE}). This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data.

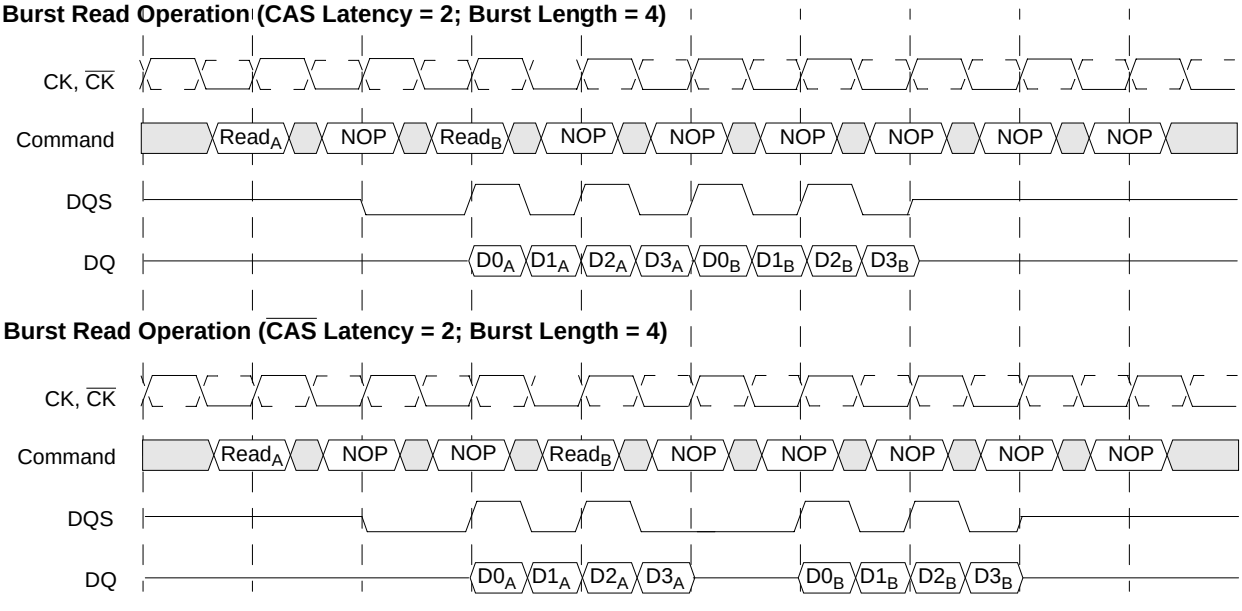
Once the burst of read data is concluded and given that no subsequent burst read operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “read postamble” (t_{RPST}). This transition happens nominally one-half clock period after the last edge of valid data.

Consecutive or “gapless” burst read operations are possible from the same DDR SDRAM device with no requirement for a data strobe “read” preamble or postamble in between the groups of burst data. The data strobe read preamble is required before the DDR device drives the first output data off chip. Similarly, the data strobe postamble is initiated when the device stops driving DQ data at the termination of read burst cycles.

Data Strobe Preamble and Postamble Timings for DDR Read Cycles



Consecutive Burst Read Operation and Effects on the Data Strobe Preamble and Postamble



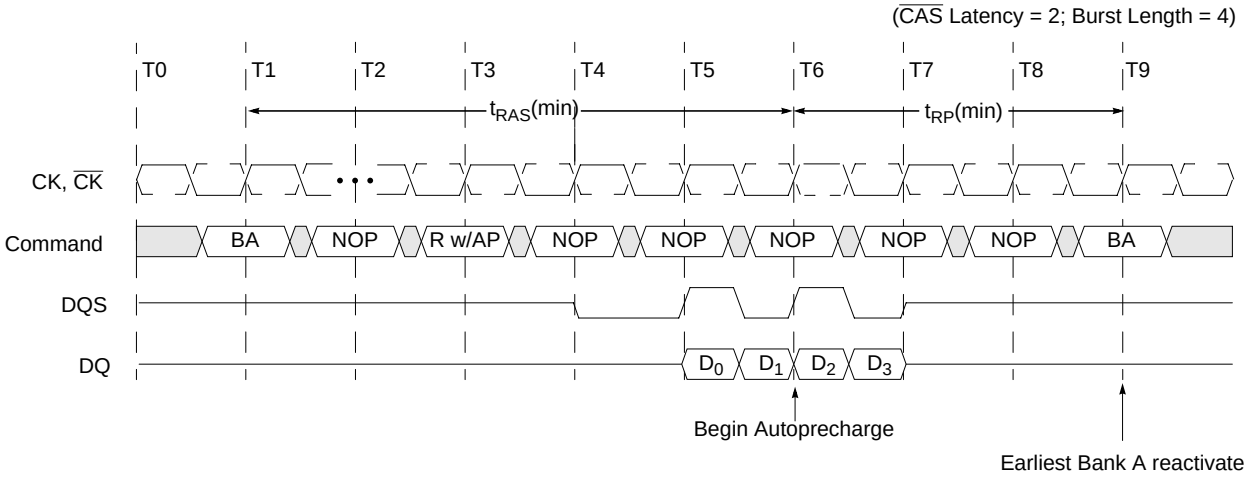
Auto Precharge Operation

The Auto Precharge operation can be issued by having column address A_{10} high when a Read or Write command is issued. If A_{10} is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once t_{RAS}(min) is satisfied.

Read with Auto Precharge

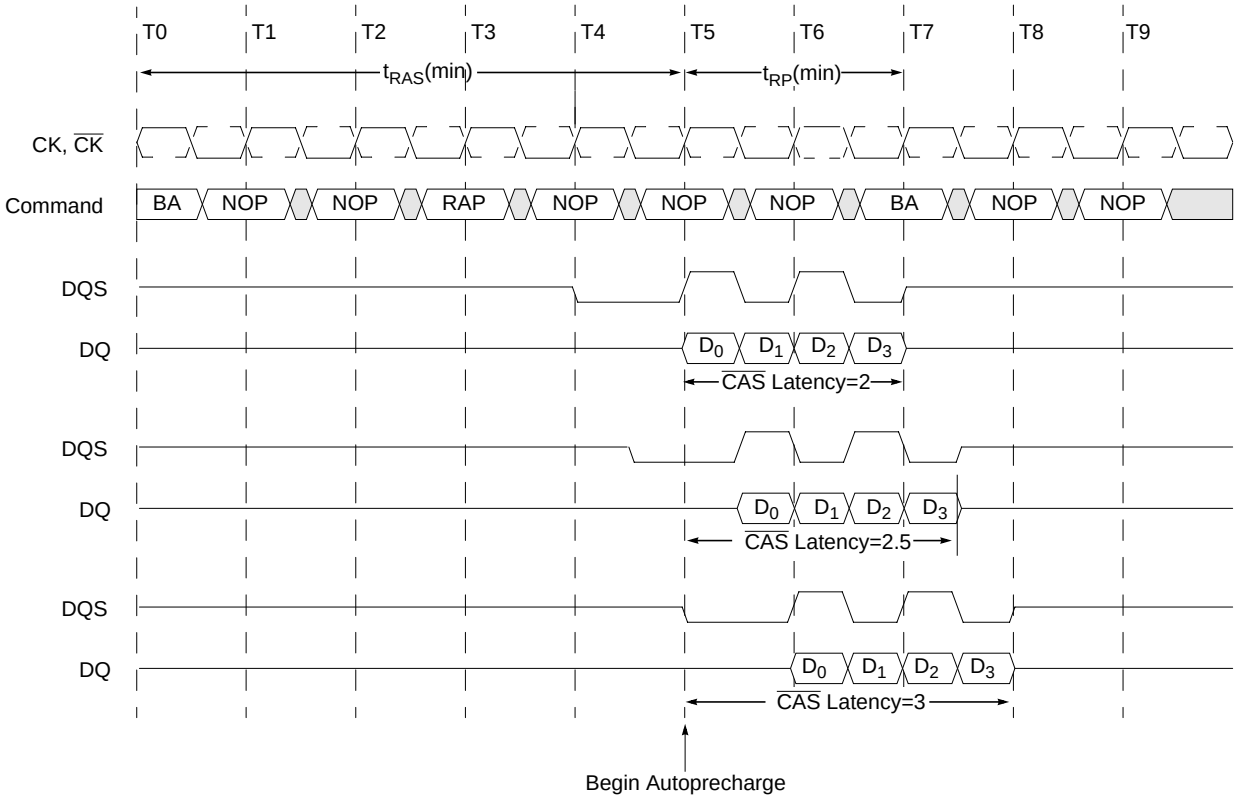
If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the $\overline{CAS}$ latency programmed into the device. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (t_{RP}) has been satisfied.

Read with Autoprecharge Timing



Read with Autoprecharge Timing as a Function of $\overline{CAS}$ Latency

($\overline{CAS}$ Latency = 2, 2.5, 3; Burst Length = 4)

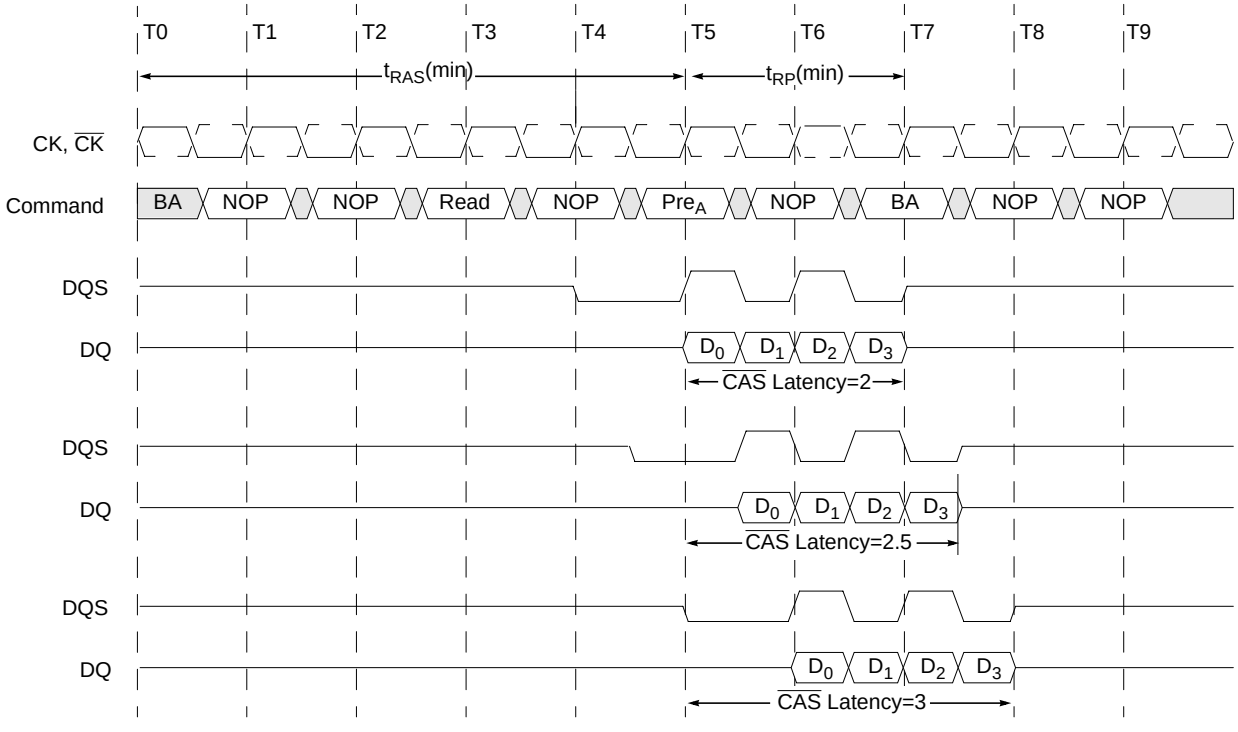


Precharge Timing During Read Operation

For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge which is $\overline{CAS}$ latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the $\overline{RAS}$ precharge time (t_{RP}). A Precharge command can not be issued until t_{RAS}(min) is satisfied.

Read with Precharge Timing as a Function of $\overline{CAS}$ Latency

($\overline{CAS}$ Latency = 2, 2.5, 3; Burst Length = 4)

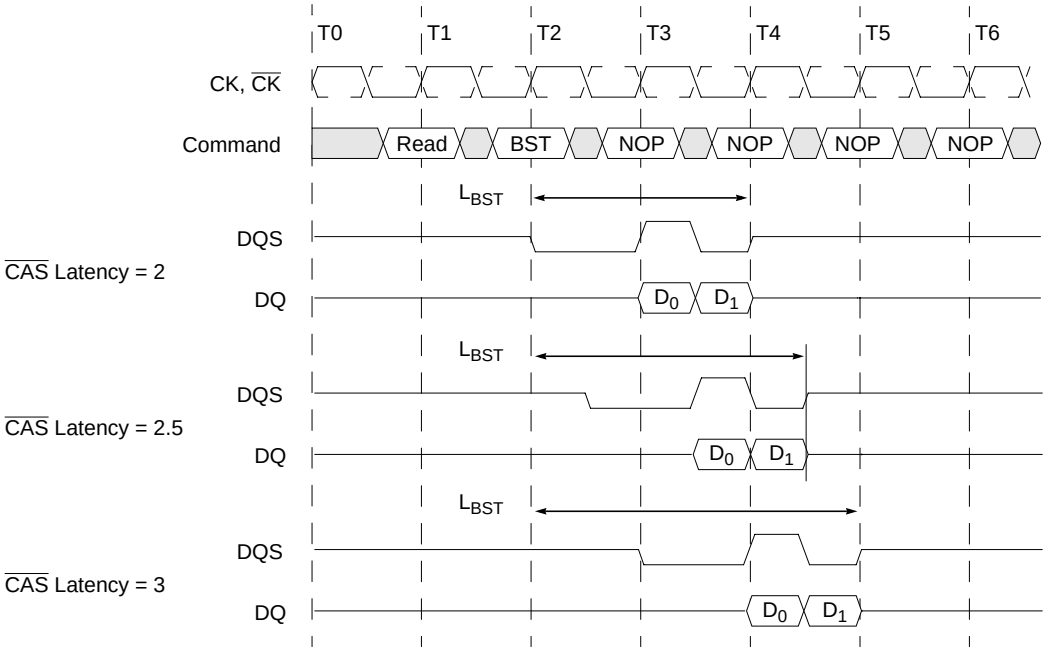


Burst Stop Command

The Burst Stop command is valid only during burst read cycles and is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay (L_{BST}) equal to the $\overline{CAS}$ latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

Read Terminated by Burst Stop Command Timing

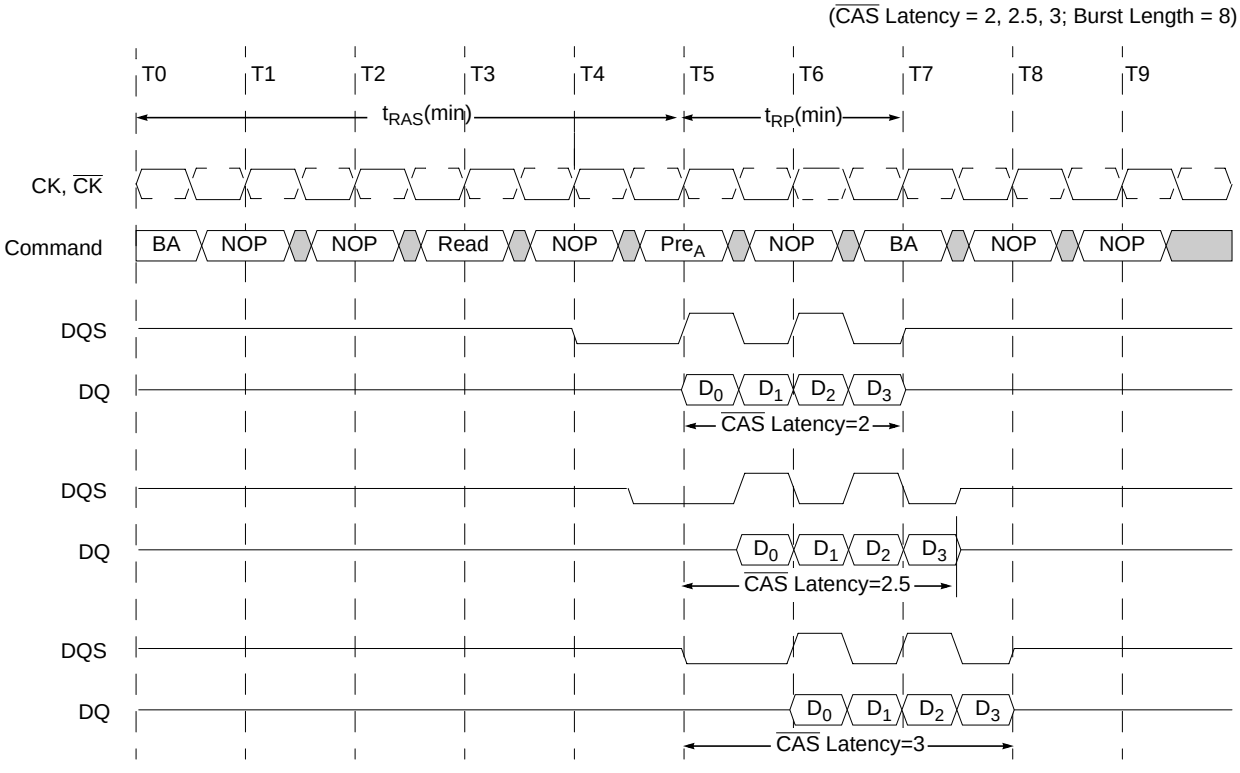
($\overline{CAS}$ Latency = 2, 2.5, 3; Burst Length = 4)



Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a precharge of the same bank. The Precharge command to Output Disable latency is equivalent to the $\overline{CAS}$ latency.

Read Interrupted by a Precharge Timing



Burst Write Operation

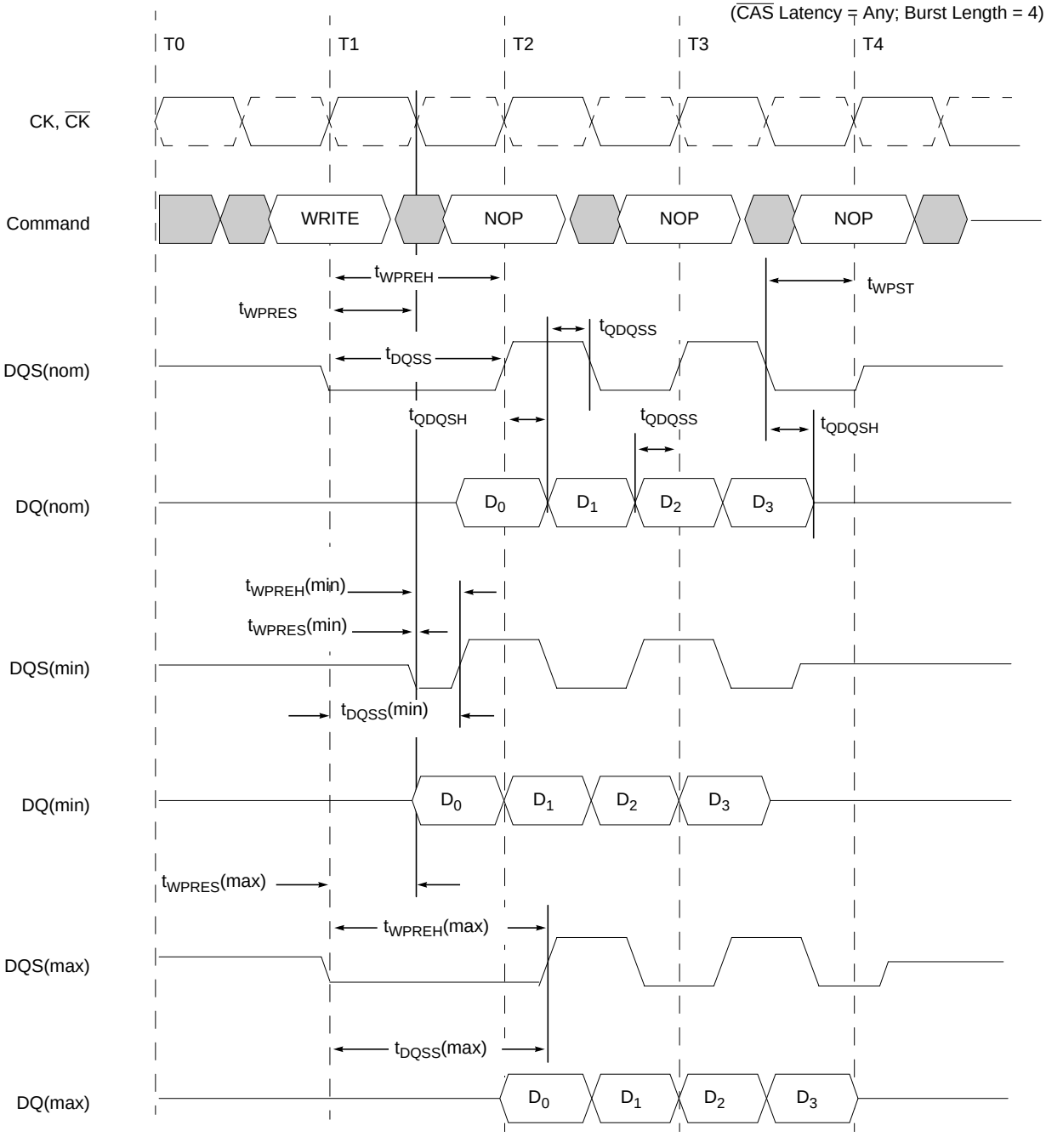
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters t_{DQSS}(min) and t_{DQSS}(max) define the allowable window when the data strobe must be driven high.

Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device (WL=1). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time (t_{QDQSS}) and DQ to DQS hold time (t_{QDQSH}). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

Write Preamble and Postamble Operation

Prior to a burst of write data and given that the controller is not currently in burst write mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe “write preamble”. This transition from Hi-Z to logic low nominally happens on the falling edge of the clock after the write command has been registered by the device. The preamble is explicitly defined by a setup time (t_{WPRES}(min)) and hold time (t_{WPREH}(min)) referenced to the first falling edge of CK after the write command.

Burst Write Timing

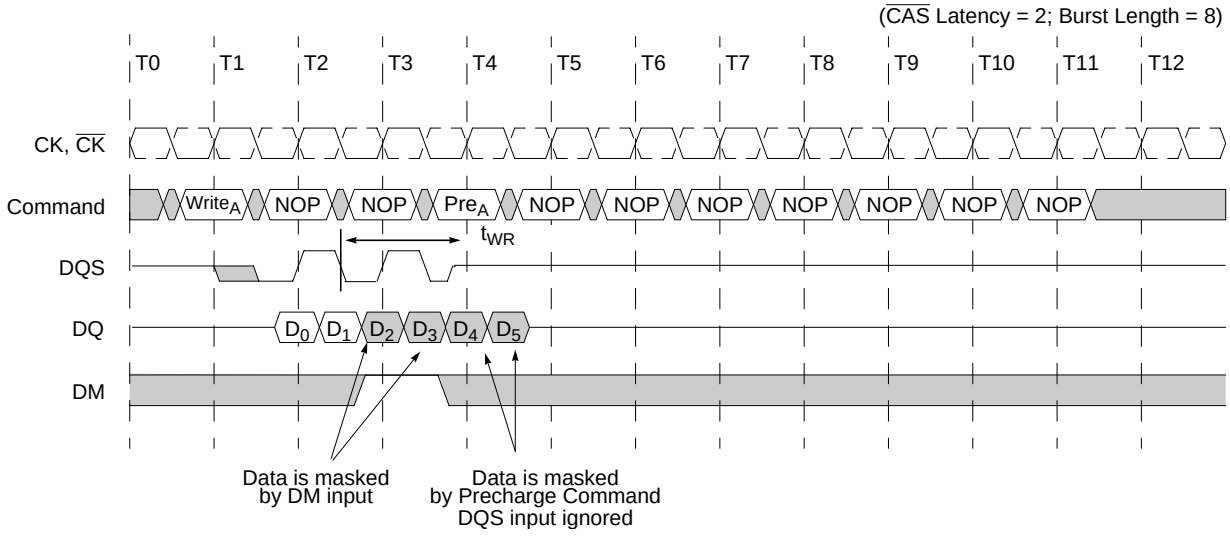


Once the burst of write data is concluded and given that no subsequent burst write operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “write postamble”. This transition happens nominally one-half clock period after the last data of the burst cycle is latched into the device.

Write Interrupted by a Precharge

A Burst Write can be interrupted before completion of the burst by a Precharge command, with the only restriction being that the interval that separates the commands be at least one clock cycle.

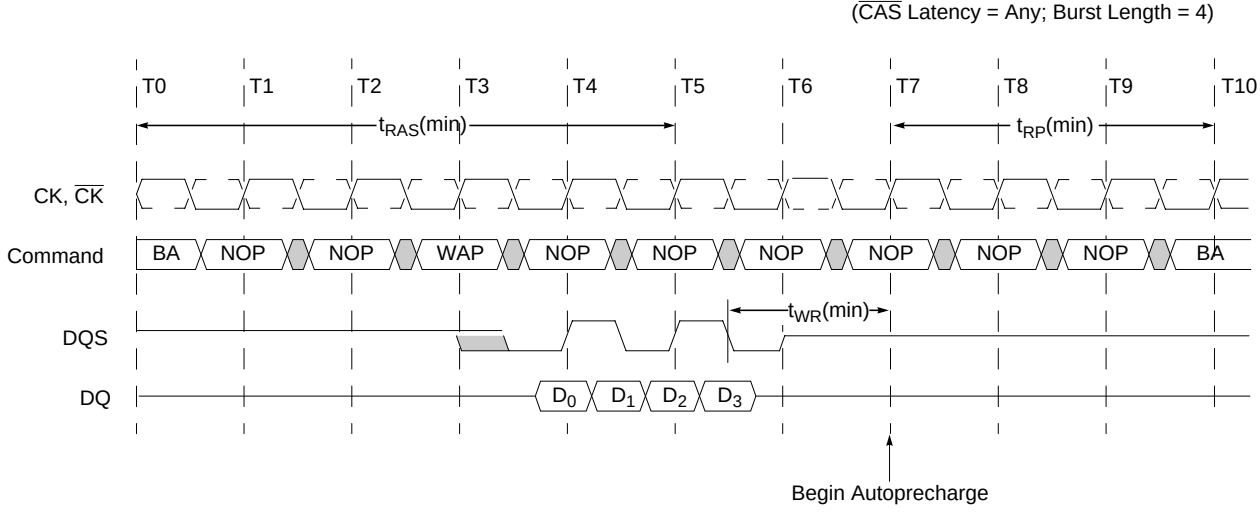
Write Interrupted by a Precharge Timing



Write with Auto Precharge

If A_{10} is high when a Write command is issued, the Write with auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{WR} (min.).

Write with Auto Precharge Timing



Precharge Timing During Write Operation

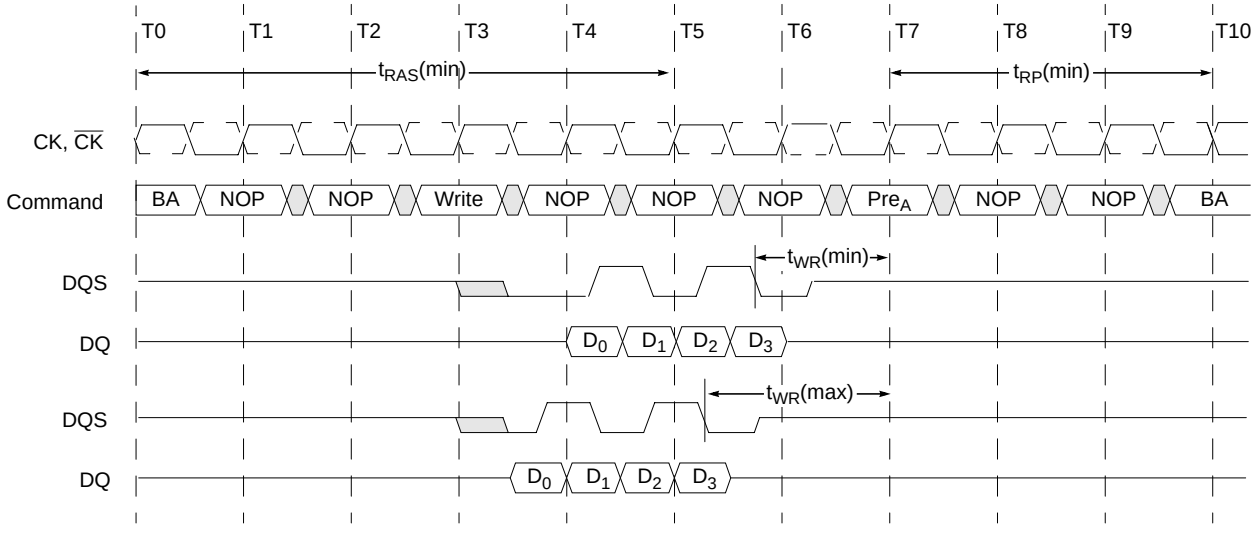
Precharge timing for Write operations in DRAMs requires enough time to satisfy the write recovery requirement. This is the time required by a DRAM sense amp to fully store the voltage level. For DDR SDRAMs, a timing parameter (t_{WR}) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The “write recovery” operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. “Write recovery” is complete on the next rising clock edge that is used to strobe in the Precharge command.

For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for “write recovery” is 1.25 clock cycles. Maximum “write recovery” time is 1.75 clock cycles.

Write with Precharge Timing

($\overline{CAS}$ Latency = Any; Burst Length = 4)



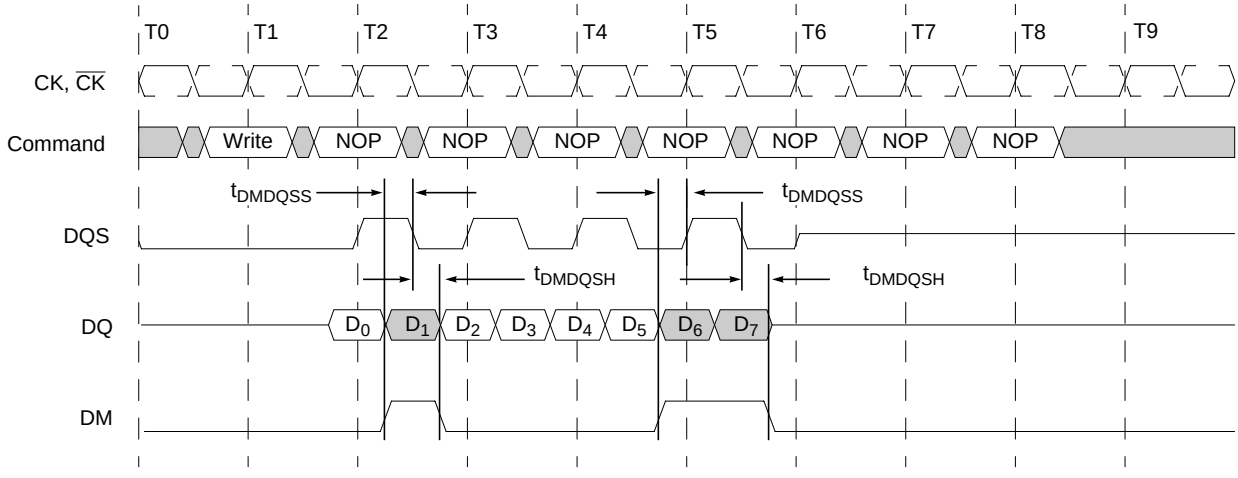
Data Mask Function

The DDR SDRAM has a Data Mask function that is used in conjunction with the Write cycle, but not the Read cycle. When the Data Mask is activated (DM high) during a Write operation, the Write is blocked (Mask to Data Latency = 0).

When issued, the Data Mask must be referenced to both the rising and falling edges of Data Strobe.

Data Mask Timing

($\overline{CAS}$ Latency = Any; Burst Length = 8)



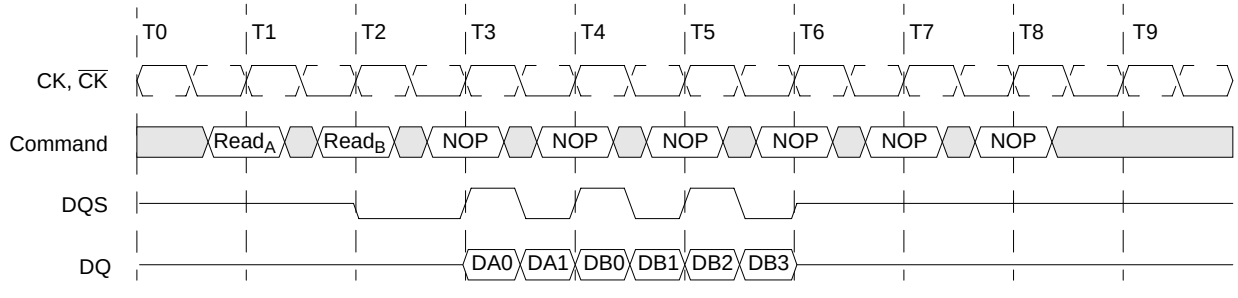
Burst Interruption

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by issuing a new Read command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears on the bus. Read commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Read with autoprecharge command with a Read command.

Read Interrupted by a Read Command Timing

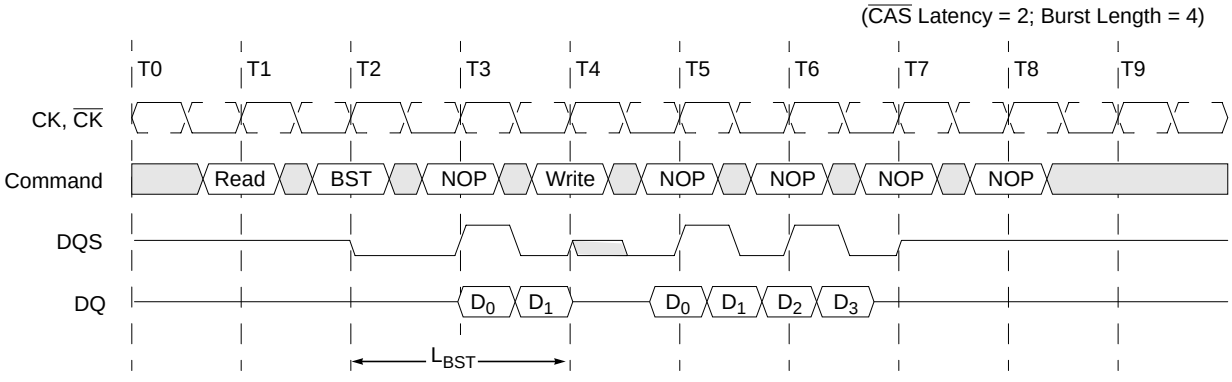
($\overline{CAS}$ Latency = 2; Burst Length = 4)



Read Interrupted by a Write

To interrupt a Burst Read with a Write command, a Burst Stop command must be asserted to stop the burst read operation and 3-state the DQ bus. Additionally, control of the DQS bus must be turned around to allow the memory controller to drive the data strobe signal (DQS) into the DDR SDRAM for the write cycles. Once the Burst Stop command has been issued, a Write command can not be issued until a minimum delay or latency (L_{BST}) has been satisfied. This latency is measured from the Burst Stop command and is equivalent to the CAS latency programmed into the mode register. In instances where CAS latency is measured in half clock cycles, the minimum delay (L_{BST}) is rounded up to the next full clock cycle (i.e., if CL=2 then L_{BST}=2, if CL=2.5 then L_{BST}=3). It is illegal to interrupt a Read with autoprecharge command with a Write command.

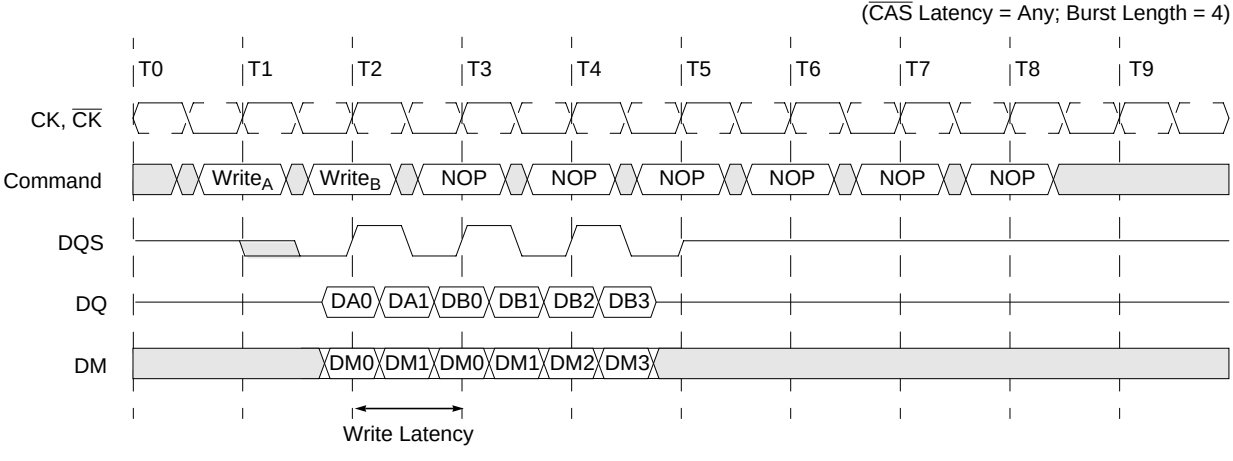
Read Interrupted by Burst Stop Command Followed by a Write Command Timing



Write Interrupted by a Write

A Burst Write can be interrupted before completion by a new Write command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Write command continues to be input into the device until the Write Latency of the interrupting Write command is satisfied (WL=1) At this point, the data from the interrupting Write command is input into the device. Write commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Write with autoprecharge command with a Write command.

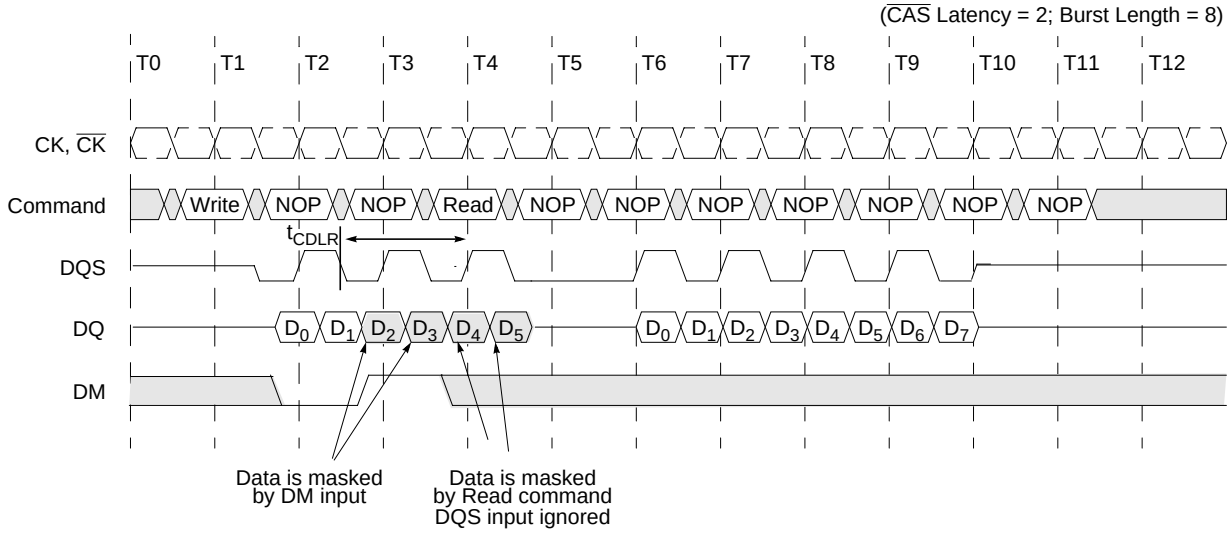
Write Interrupted by a Write Command Timing



Write Interrupted by a Read

A Burst Write can be interrupted by a Read command to any bank. If a burst write operation is interrupted prior to the end of the burst operation, then the last two pieces of input data prior to the Read command must be masked off with the data mask (DM) input pin to prevent invalid data from being written into the memory array. Any data that is present on the DQ pins coincident with or following the Read command will be masked off by the Read command and will not be written to the array. The memory controller must give up control of both the DQ bus and the DQS bus at least one clock cycle before the read data appears on the outputs in order to avoid contention. In order to avoid data contention within the device, a delay is required (t_{CDLR}) from the last valid data input before a Read command can be issued to the device. It is illegal to interrupt a Write with autoprecharge command with a Read command.

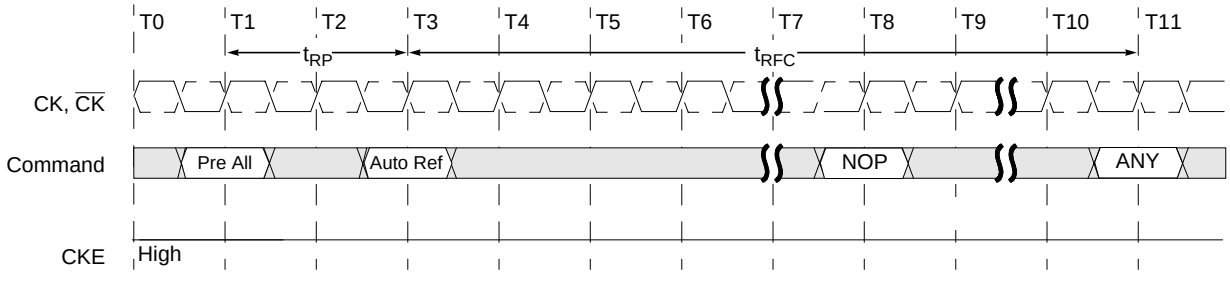
Write Interrupted by a Read Command Timing



Auto Refresh

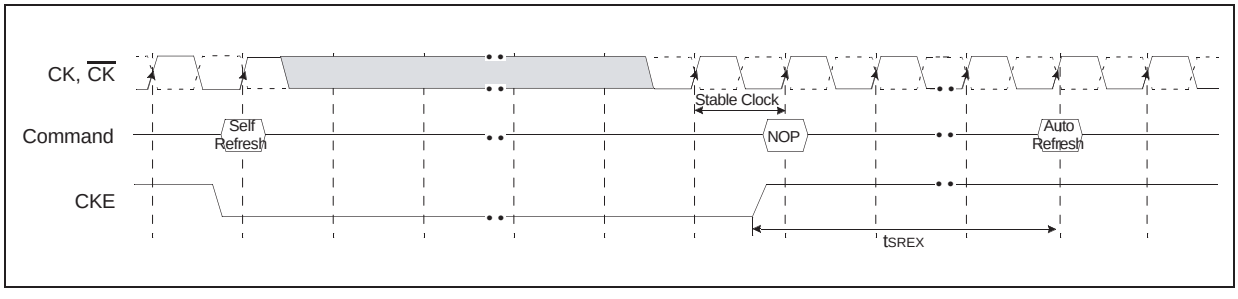
The Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC}(min). Commands may not be issued to the device once an Auto Refresh cycle has begun. $\overline{CS}$ input must remain high during the refresh period or NOP commands must be registered on each rising edge of the CK input until the refresh period is satisfied.

Auto Refresh Timing



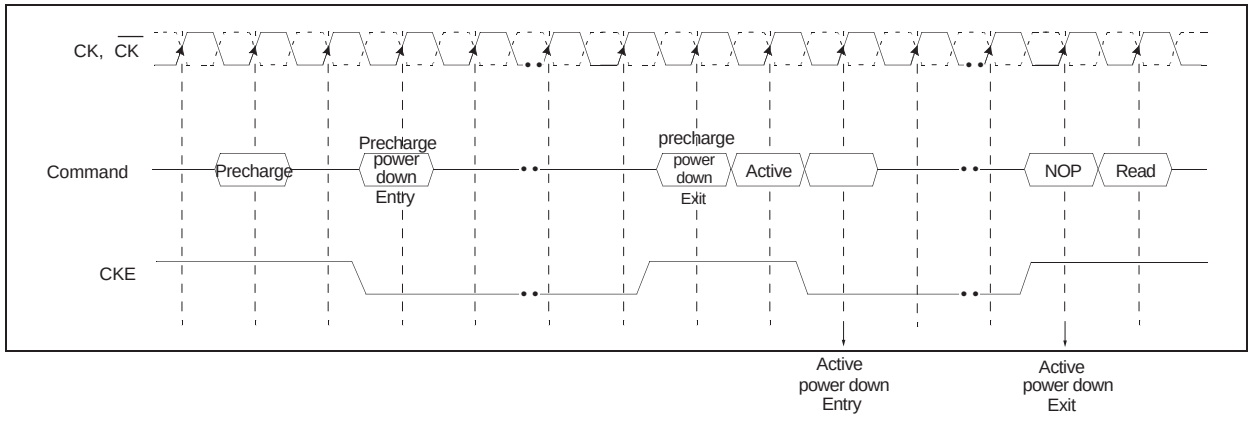
Self Refresh

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{SREX} for locking of DLL. The auto refresh is required before self refresh entry and after self refresh exit.



Power Down Mode

The power down mode is entered when CKE is low and exited when CKE is high. Once the power down mode is initiated, all of the receiver circuits except clock, CKE and DLL circuit tree are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tck+tIS prior to row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period (t_{REF}) of the device.



SSTL_2 Input AC/DC Logic Levels

Symbol	Parameter	Min	Max	Units	Notes
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.18	V_{DDQ}+0.3	V	1
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.35	—	V	
V_{IL} (DC)	DC Input Logic Low	–0.30	V_{REF}–0.18	V	
V_{IL} (AC)	AC Input Logic Low	—	V_{REF}–0.35	V	

Note: 1. The relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of V_{IH} (max) (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0V (High corner V_{DDQ}+300mV.)

SSTL_2 AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{REF}	Input Reference Voltage	0.5*V_{DDQ}	V	1
V_{SWING} (max)	Input Signal Maximum Peak to Peak Swing	1.5	V	1, 2
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns	3

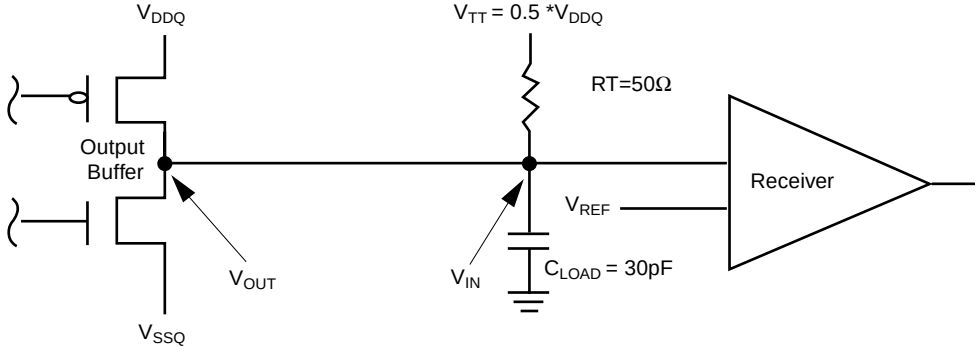
Notes: 1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
3. The 1 V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IL} min (AC) range of the input signal swing.

SSTL_2 Output Buffers

The input voltage provided to the receiver depends on three parameters:

- V_{DDQ} and current drive capabilities of the output buffer
- Termination voltage
- Termination resistance
- V_{DDQ}=2.5 ± 0.2V

Class II SSTL_2 Output Buffer (Driver)



DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_A=0 to 70°C

Parameter	Symbol	Test Condition	$\overline{CAS}$ Latency	Version			Unit
				-36	–4	–5	
Operating Current (One Bank Active)	$I_{CC}1$	Burst Length=2 t_{RC}=t_{RC}(min) I_{OL}=0mA		155	150	140	mA
Precharge Standby Current in Power-Down Mode	$I_{CC2}P$	CKE=V_{IL}(max), t_{CC}=10ns		20			mA
Precharge Standby Current in Non Power-Down Mode	$I_{CC2}N$	CKE=VIH(min), CS=VIH(min), tCC=10ns Input signals are changed once during 20ns		45			mA
Active Standby Current in Power-Down Mode	$I_{CC3}P$	CKE=V_{IL}(max), t_{CC}=10ns		30			mA
Active Standby Current in Non-Power-Down Mode	$I_{CC3}N$	CKE=VIH(min), CS=VIH(min), tCC=10ns Input signals are changed once during 20ns		60			mA
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA Page Burst All Banks activated t_{CCD}=2CKs	3	165	160	150	mA
Refresh Current	I_{CC5}	t_{RC}=t_{RFC} (min)		200			mA
Self Refresh Current	I_{CC6}	CKE=0.2V		2			mA

AC Characteristics (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V)

Symbol	Parameter		-36		–4		–5		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Clock Cycle									
t_{CK}	Clock Cycle	CL = 2.0	5.4	8	6	8	7.5	8	ns
		CL = 2.5	4.3	8	4.8	8	6	8	ns
		CL = 3.0	3.6	8	4	8	5	8	ns
t_{CH}	Clock Duty Cycle		0.45	0.55	0.45	0.55	0.45	0.55	%
t_{CL}			0.45	0.55	0.45	0.55	0.45	0.55	%
Command Cycle									
t_{RAS}	Row Active Time (ACT->PRE)		36	100K	36	100K	40	100K	ns
t_{RP}	Row Precharge (PRE->ACT)		18	-	20	-	20	-	ns
t_{RC}	Row Cycle (ACT->ACT)		54	-	56	-	60	-	ns
t_{RCD}	RAS->CAS Delay (ACT->WR/RD)		18	-	18	-	20	-	ns
t_{RRD}	RAS->RAS Delay (ACTa->ACTb)		7.2	-	8	-	10	-	ns
t_{RFC}	Auto-Refresh (REF->REF/ACT)		68	-	68	-	70	-	ns
t_{REF}	Refresh Cycle		-	64	-	64	-	64	ms
$t_{SREX(DLL)}$	Self-Refresh Exit Delay		200	-	200	-	200	-	cycles
t_{SREX}			1	-	1	-	1	-	t_{RC}
t_{IS}	CMD, ADDR->CLK Setup		0.9	-	0.9	-	1.0	-	ns
t_{IH}	CMD, ADDR->CLK Hold		0.9	-	0.9	-	1.0	-	ns
t_{CCD}	CAS->CAS Delay (Cola->Colb)		1		1		1		t_{CK}
t_{MRD}	Mode Register Set Delay		3		3		2		t_{CK}
t_{PDENT}	Power Down Entry Delay		1		1		1		t_{CK}
$t_{PDEX(DLL)}$	Power Down Exit Delay		1		1		1		t_{CK}
t_{PDEX}			1		1		1		t_{CK}
Read Cycle									
t_{AC}	CLK->DQ Skew		-0.1	0.2	-0.2	0.125	-0.2	0.1	t_{CK}
t_{DQSCK}	CLK->DQS Skew		-0.1	0.2	-0.2	0.125	-0.2	0.1	t_{CK}
t_{DQSQ}	DQS->DQ Skew		-0.075	0.1	-0.075	0.1	-0.075	0.08	t_{CK}
t_{DV}	DQ/DQS Valid Window		0.3	-	0.3	-	0.3	-	t_{CK}
t_{RPRE}	Read DQS Preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read DQS Postamble		0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}

AC Characteristics (Continued) (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V)

Symbol	Parameter	-36		–4		–5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle								
t_{WPRES}	Write Preamble DQS Setup	0	-	0	-	0	-	t_{CK}
t_{WPREH}	Write Preamble DQS Hold	0.42	-	0.375	-	0.3	-	t_{CK}
t_{DQSS}	Write Preamble CLK->DQS (first)	0.8	1.25	0.8	1.25	0.75	1.25	t_{CK}
t_{DSH}	Write DQS High Width	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{DSL}	Write DQS Low Width	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{WPST}	Write Postamble DQS (last) -> Hi-Z	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{DQSR}	Write (last DIN) -> READ Command	2	-	2	-	1	-	t_{CK}
t_{WR}	Write (last DIN) -> PRE Command	3	-	2	-	2	-	t_{CK}
t_{DS}	DQ/DM -> DQS Setup (Data Setup)	0.25	-	0.25	-	0.25	-	t_{CK}
t_{DH}	DQ/DM -> DQS Hold (Data Hold)	0.25	-	0.25	-	0.25	-	t_{CK}
t_{QDQSS}	Date Input to Data Strobe Setup Time	0.075	-	0.075	-	0.075	-	t_{CK}
t_{QDQSH}	Date Input to Data Strobe Hold Time	0.075	-	0.075	-	0.075	-	t_{CK}
t_{DMDSQS}	Date Mask to Data Strobe Setup Time	0.075	-	0.075	-	0.075	-	t_{CK}
t_{DMDQSH}	Date Mask to Data Strobe Hold Time	0.075	-	0.075	-	0.075	-	t_{CK}

DDR SDRAM SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

Complete List of Operation Commands

DDR SDRAM Function Truth Table

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{BS}$	Addr	ACTION
Idle	H	X	X	X	X	X	NOP or Power Down
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh[5]
	L	L	L	L	Op-	Code	Mode reg. Access[5]
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; DetermineAP
	L	H	L	L	BS	CA,AP	Begin Write; Latch CA; DetermineAP
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Term Burst
	L	H	L	H	BS	CA,AP	Term Burst, New Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	ILLEGAL (Need Term Burst before Write)
	L	L	H	H	BS	X	ILLEGAL to Same Bank, other Bank 0K if tRRD is Satisfied
	L	L	H	L	BS	AP	Term Burst, Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	NOP
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, New Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge[3]
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
with	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
Auto	L	H	H	L	BS	X	ILLEGAL[2]
Precharge	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL

DDR SDRAM Function Truth Table (continued)

CURRENT STATE[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{BS}$	Addr	ACTION
Write	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
with	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
Auto	L	H	H	L	BS	X	ILLEGAL[2]
Precharge	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Precharging	H	X	X	X	X	X	NOP;> Idle after tRP
	L	H	H	H	X	X	NOP;> Idle after tRP
	L	H	H	L	BS	X	NOP
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	(0K Provided tRP Satisfied) ACT
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	X	X	X	ILLEGAL
Row	H	X	X	X	X	X	NOP;> Row Active after tRCD
Activating	L	H	H	H	X	X	NOP;> Row Active after tRCD
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	(0K if tRCD satisfied) Read/Write
	L	L	H	H	BS	X	(0K to other Bank if tRRD Satisfied) ACT
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP
Recovering	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	NOP;> Idle after tRC
	L	H	H	X	X	X	NOP;> Idle after tRC
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode	H	X	X	X	X	X	NOP
Register	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
Accessing	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

Clock Enable (CKE) Truth Table

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	H	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All. Banks Idle[7]	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power- Down
	H	L	L	H	H	H	X	Enter Power- Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8].
	L	L	X	X	X	X	X	Maintain Clock Suspend.

Abbreviations:

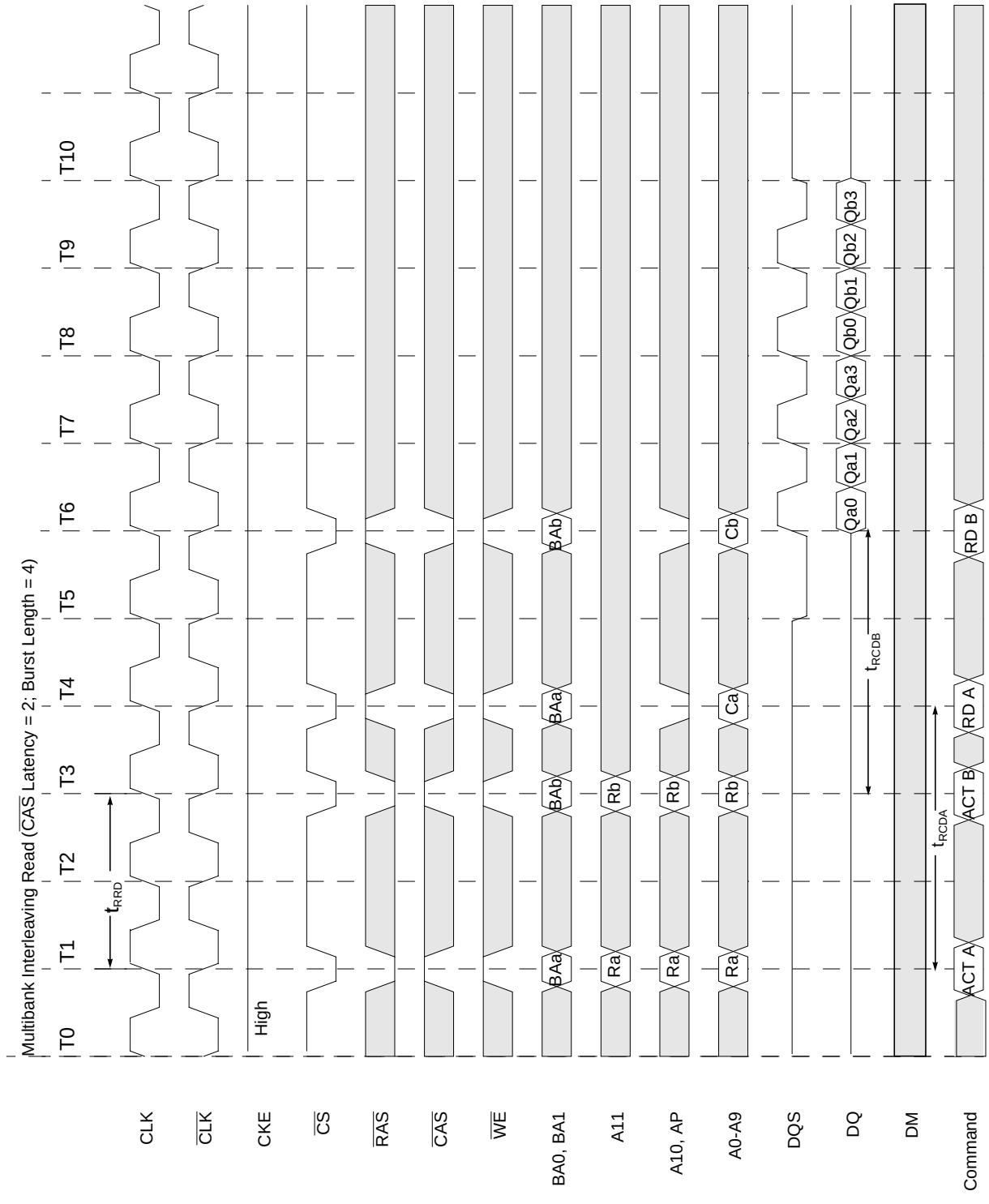
RA = Row Address BS = Bank Select Address

CA = Column Address AP = Auto Precharge

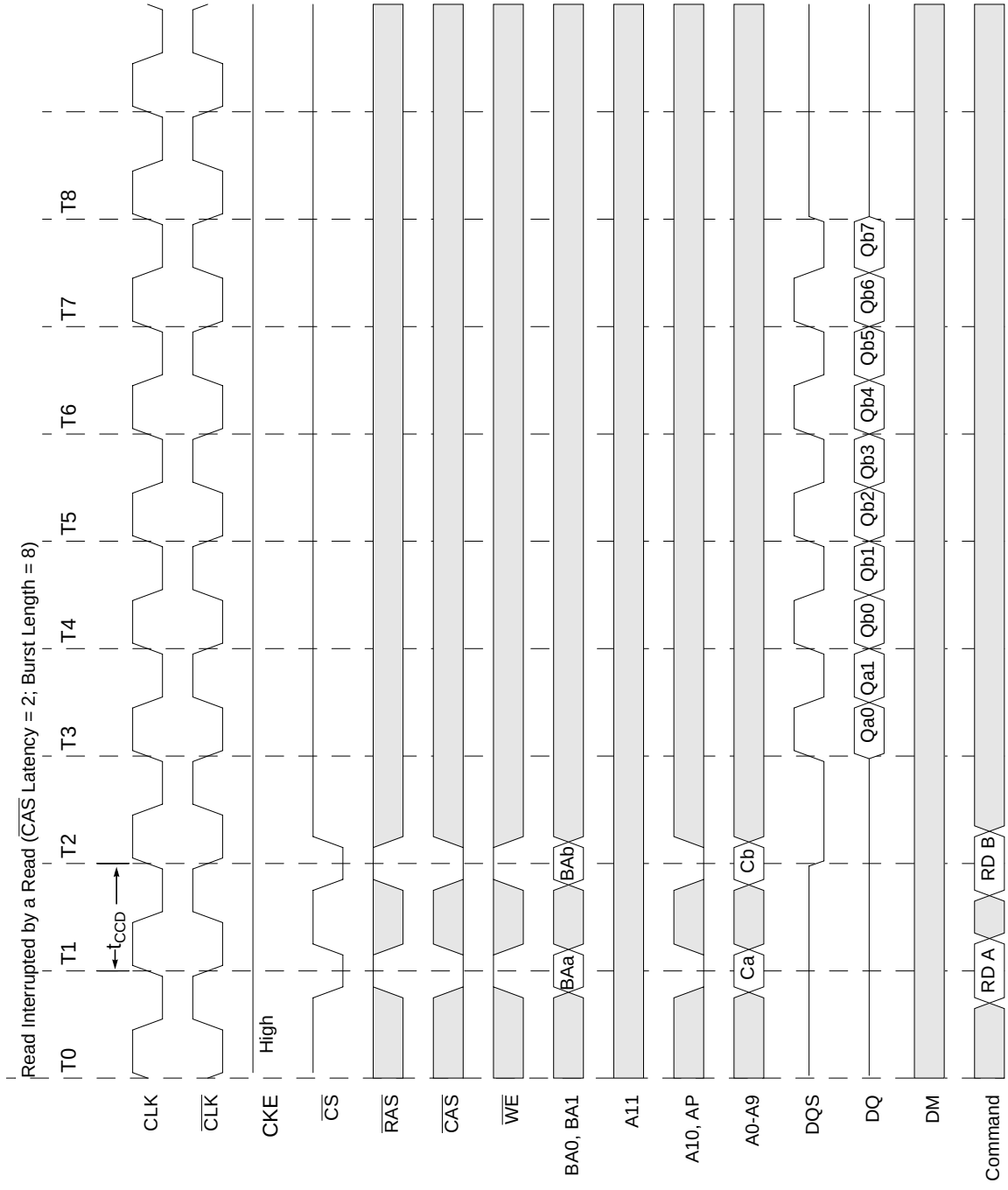
Notes for SDRAM function truth table:

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. The precharge bank(s) indicated by BS and AP.
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

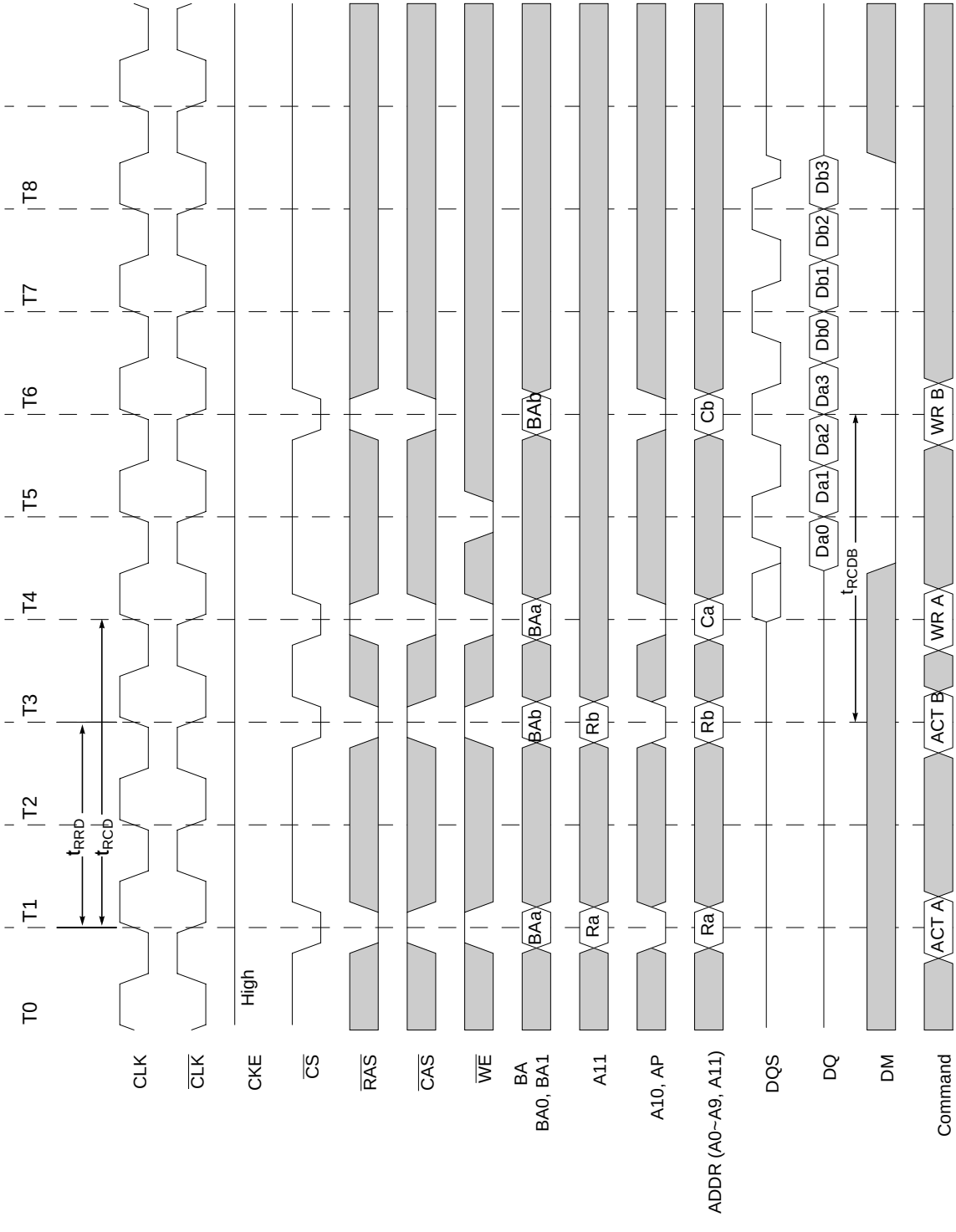
Multibank Interleaving Read



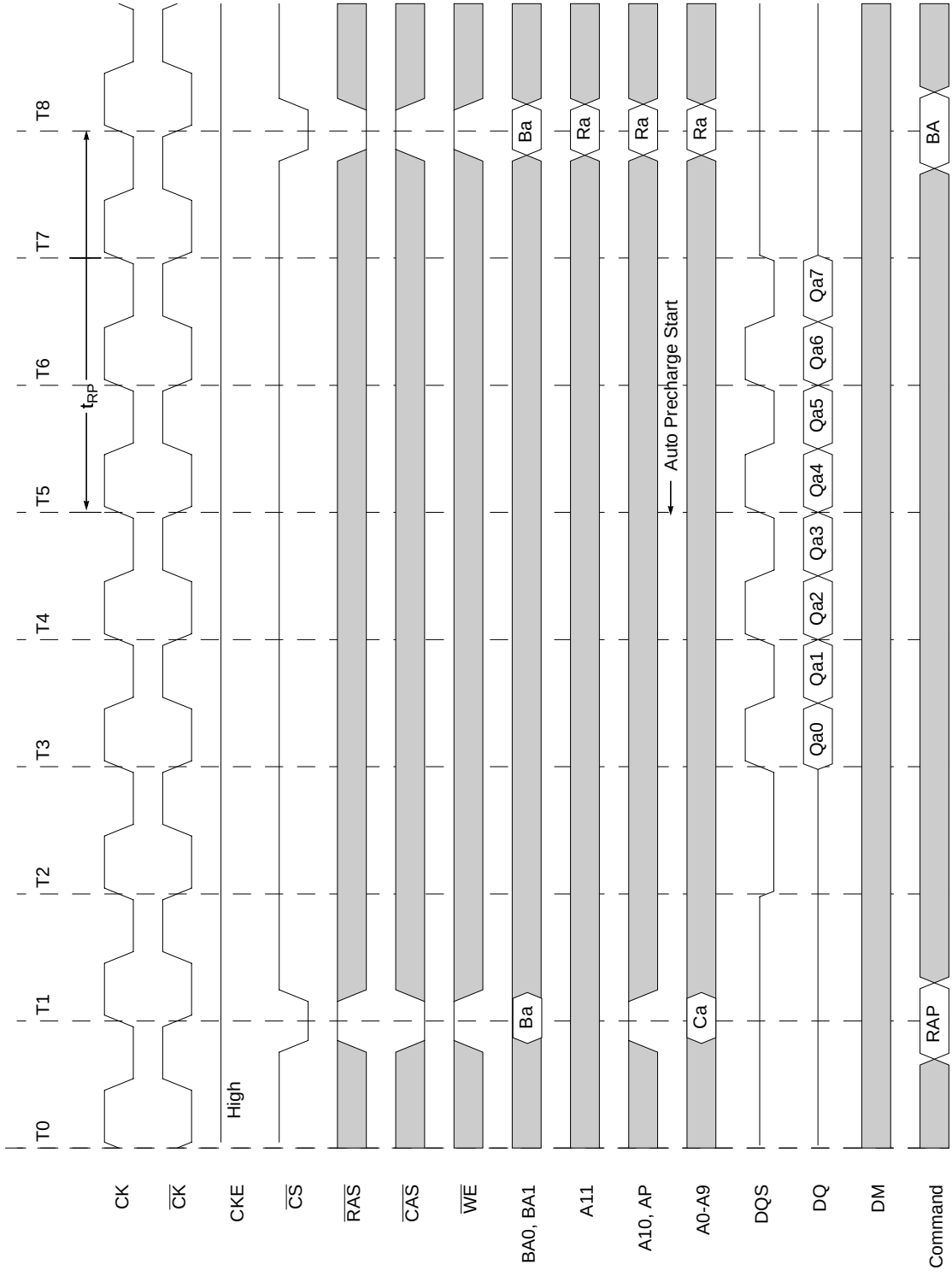
Read Interrupted by a Read



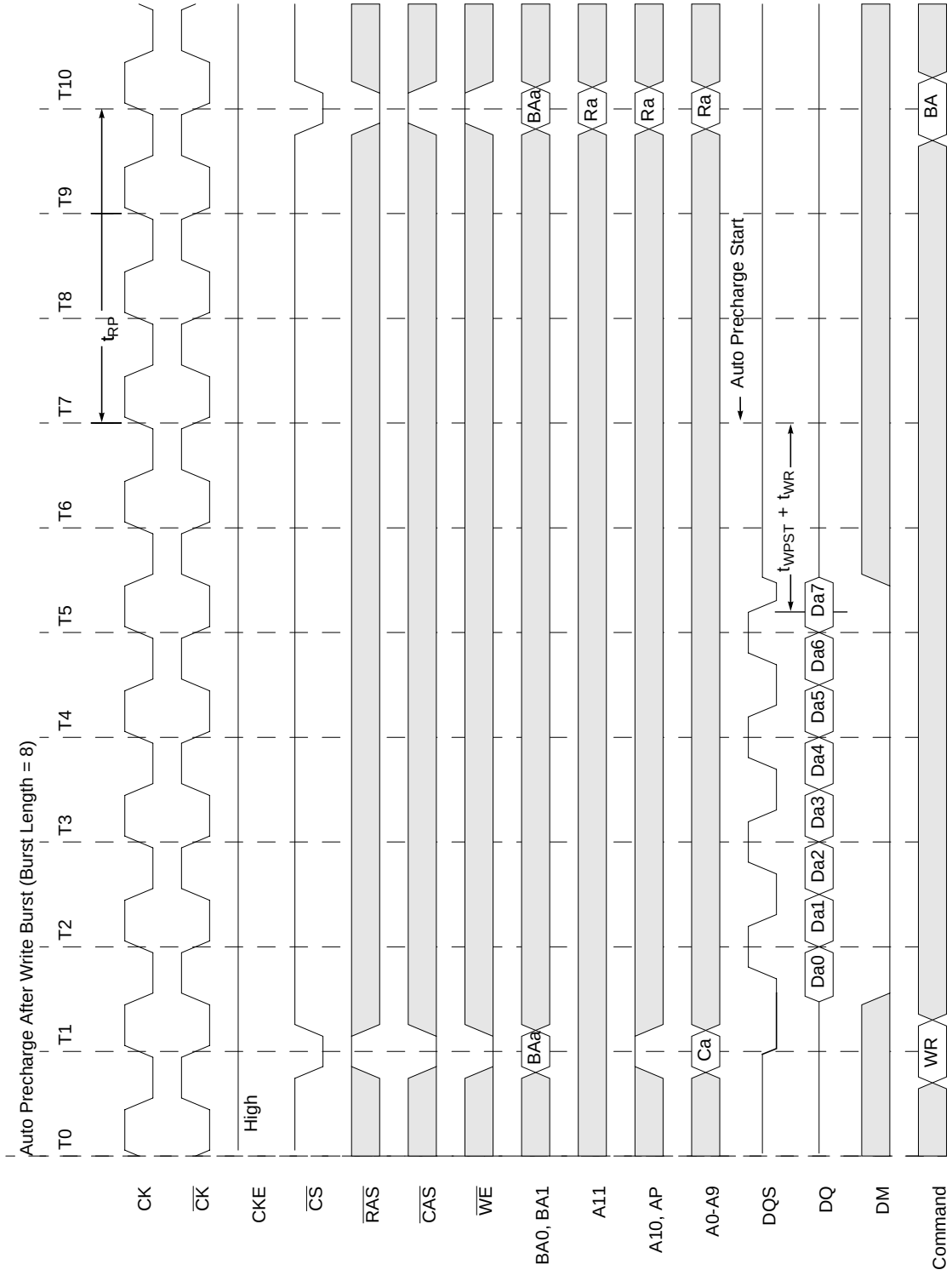
Multi Bank Interleaving Write (@ BL = 4)



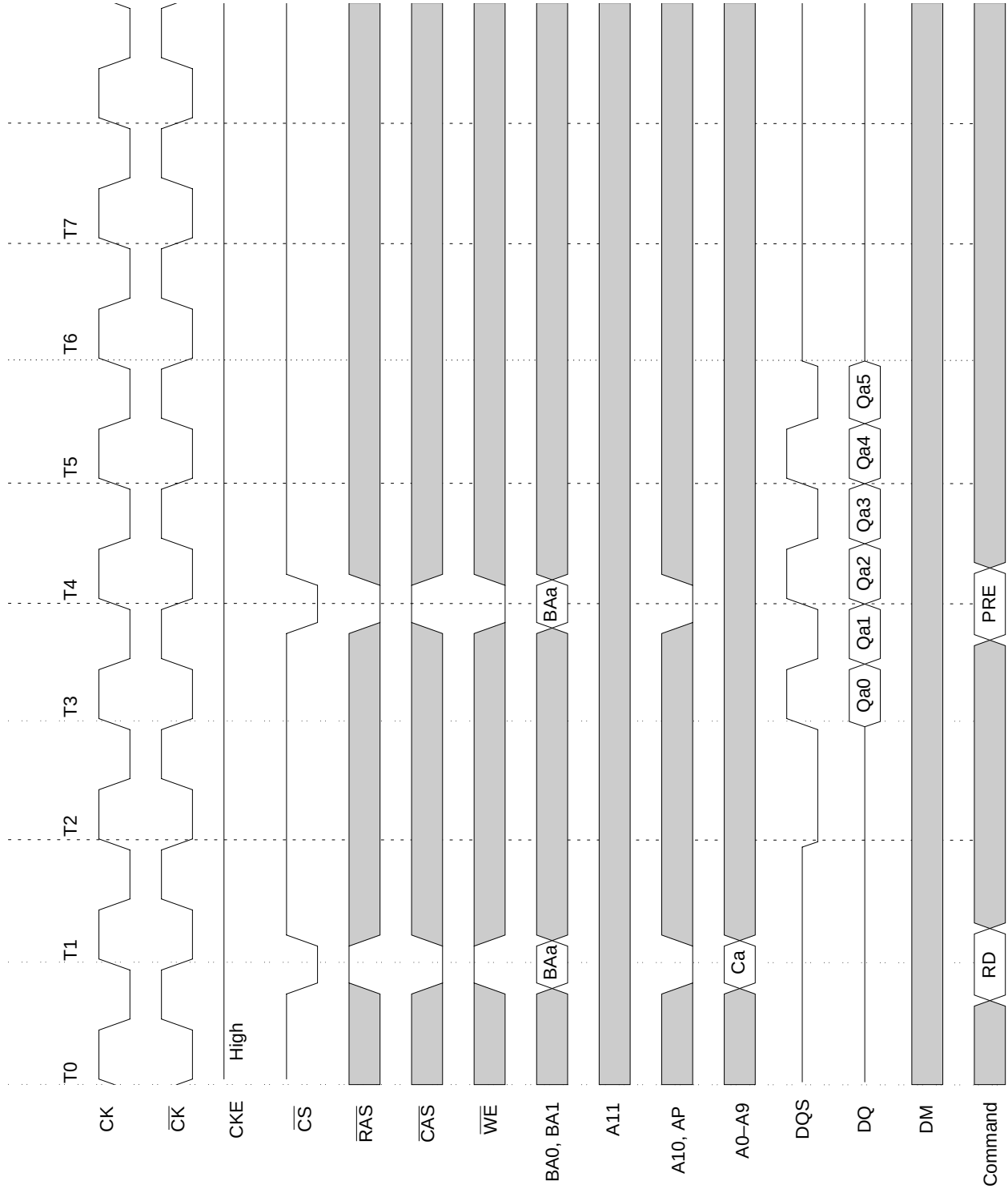
Auto Precharge After Read Burst (@ BL = 8, CL = 2)



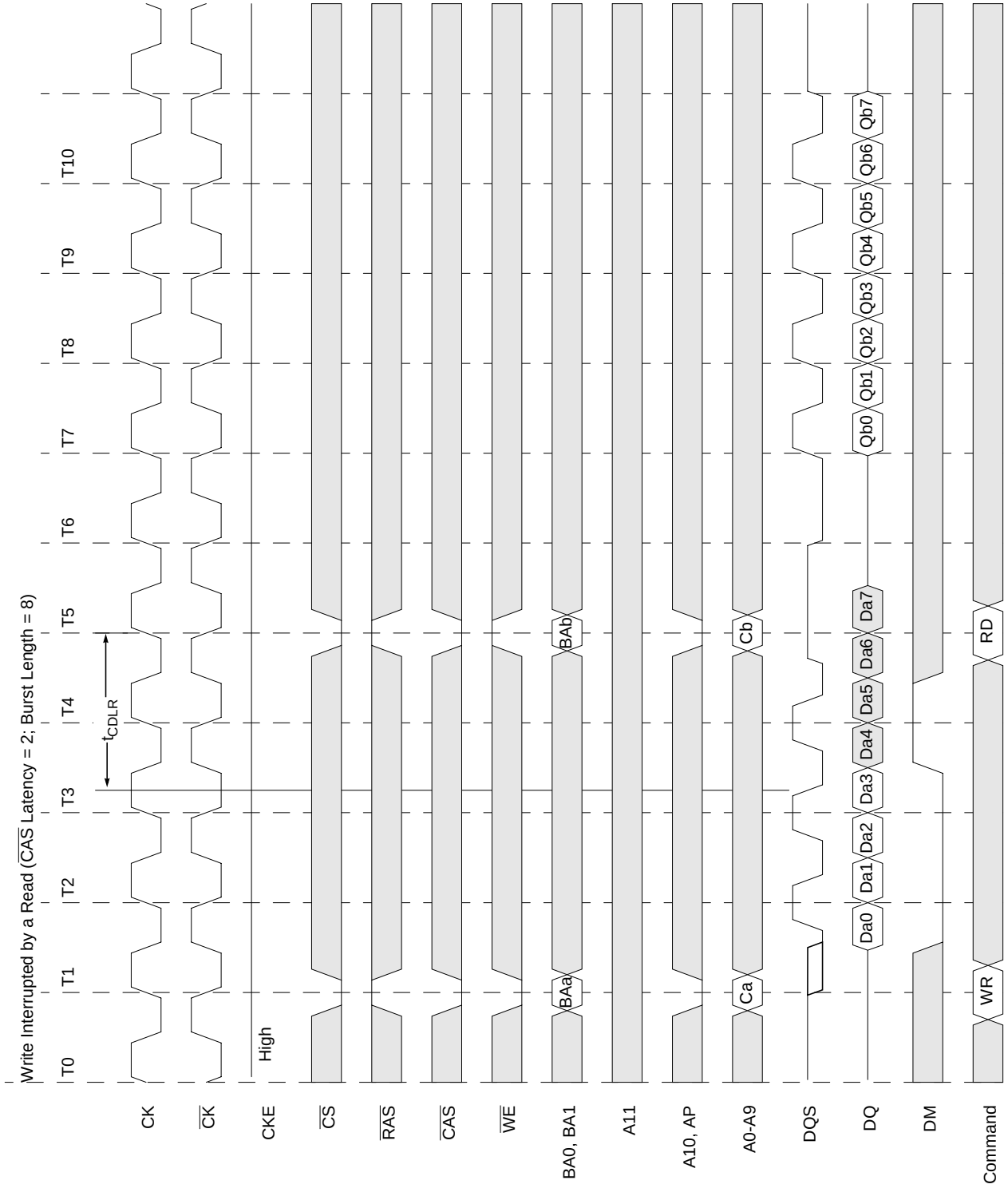
Auto Precharge After Write Burst (@ BL=8)



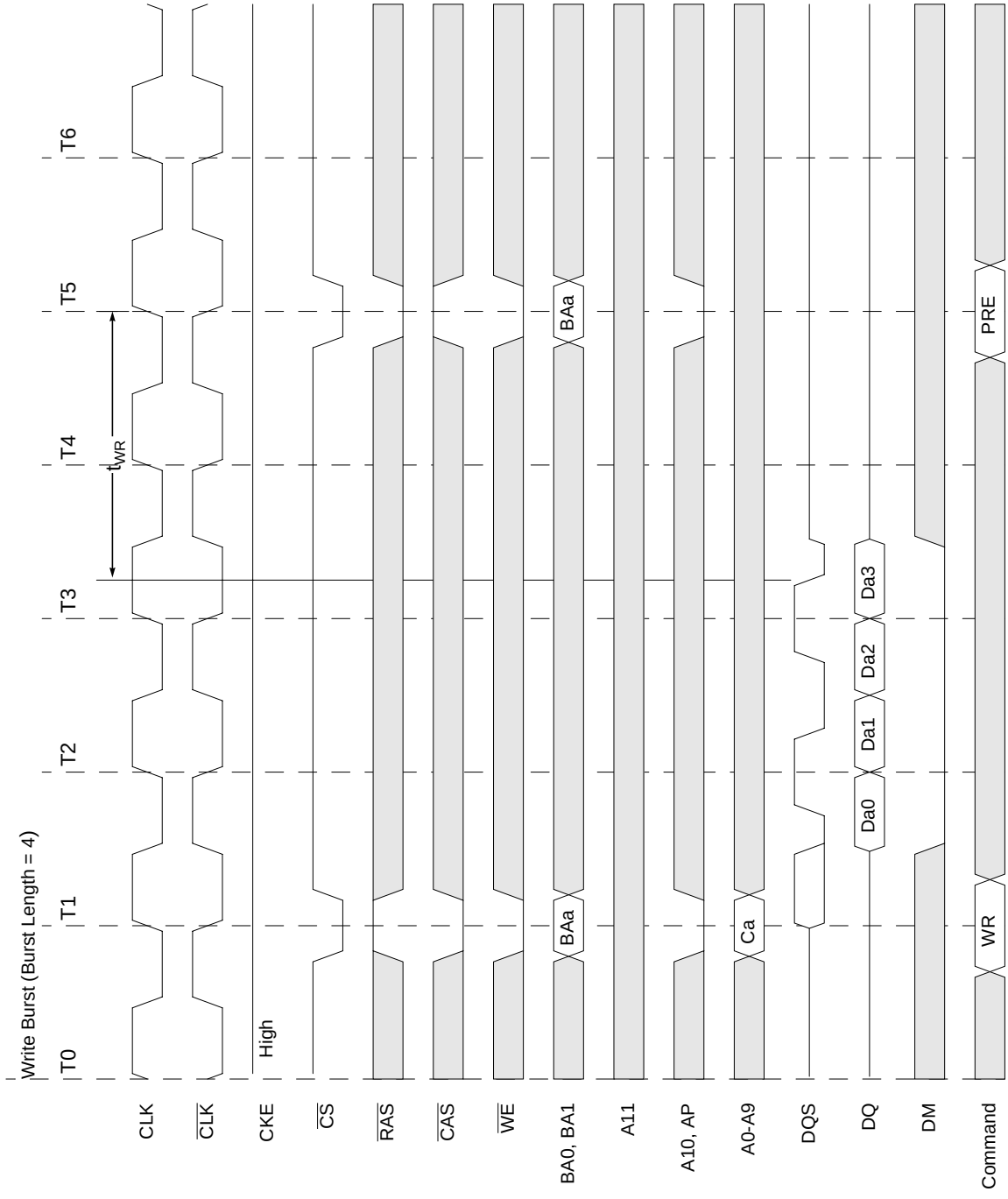
Read Interrupted by Precharge (@BL = 8, CL = 2)



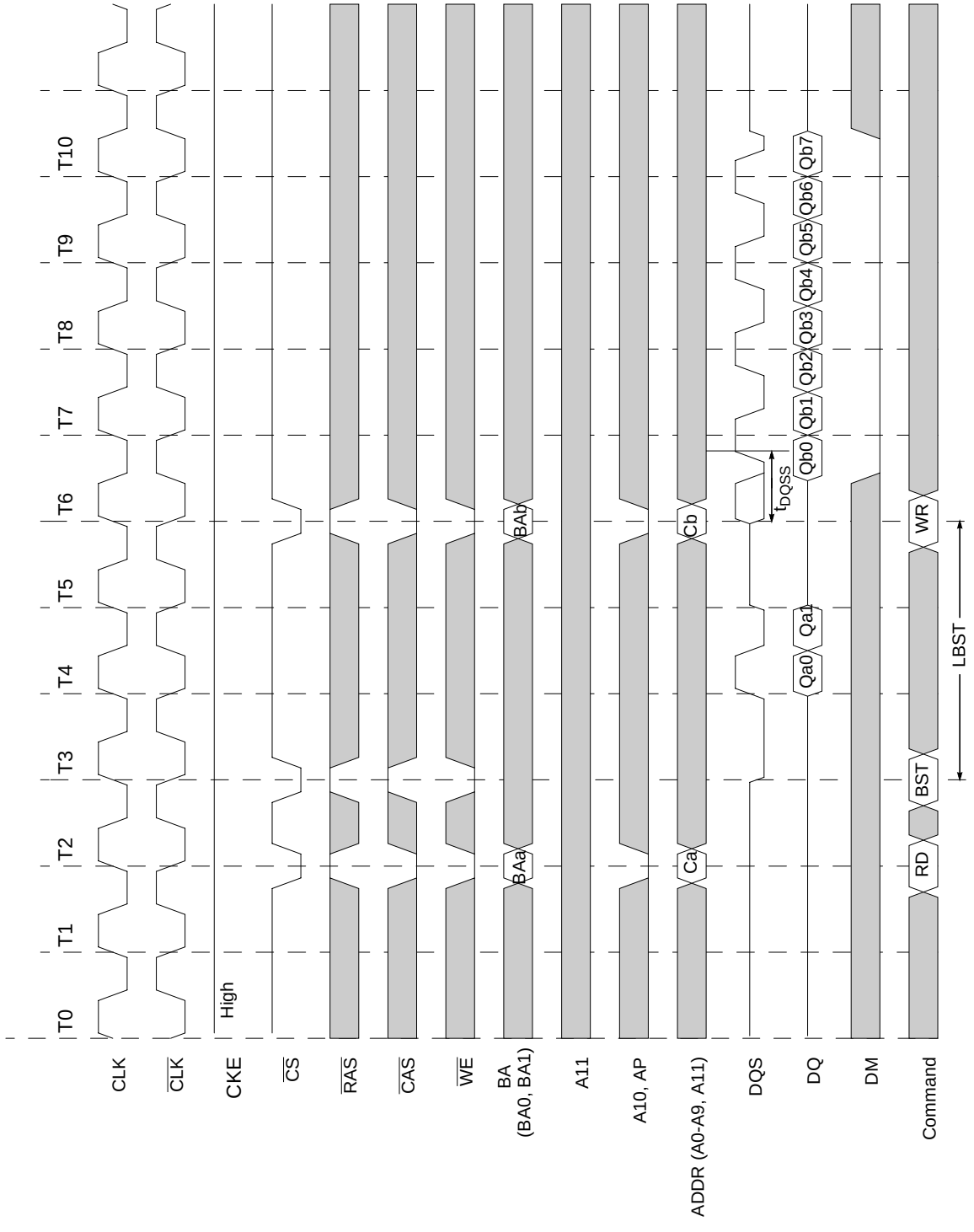
Write Interrupted by a Read (@BL=8, CL=2)



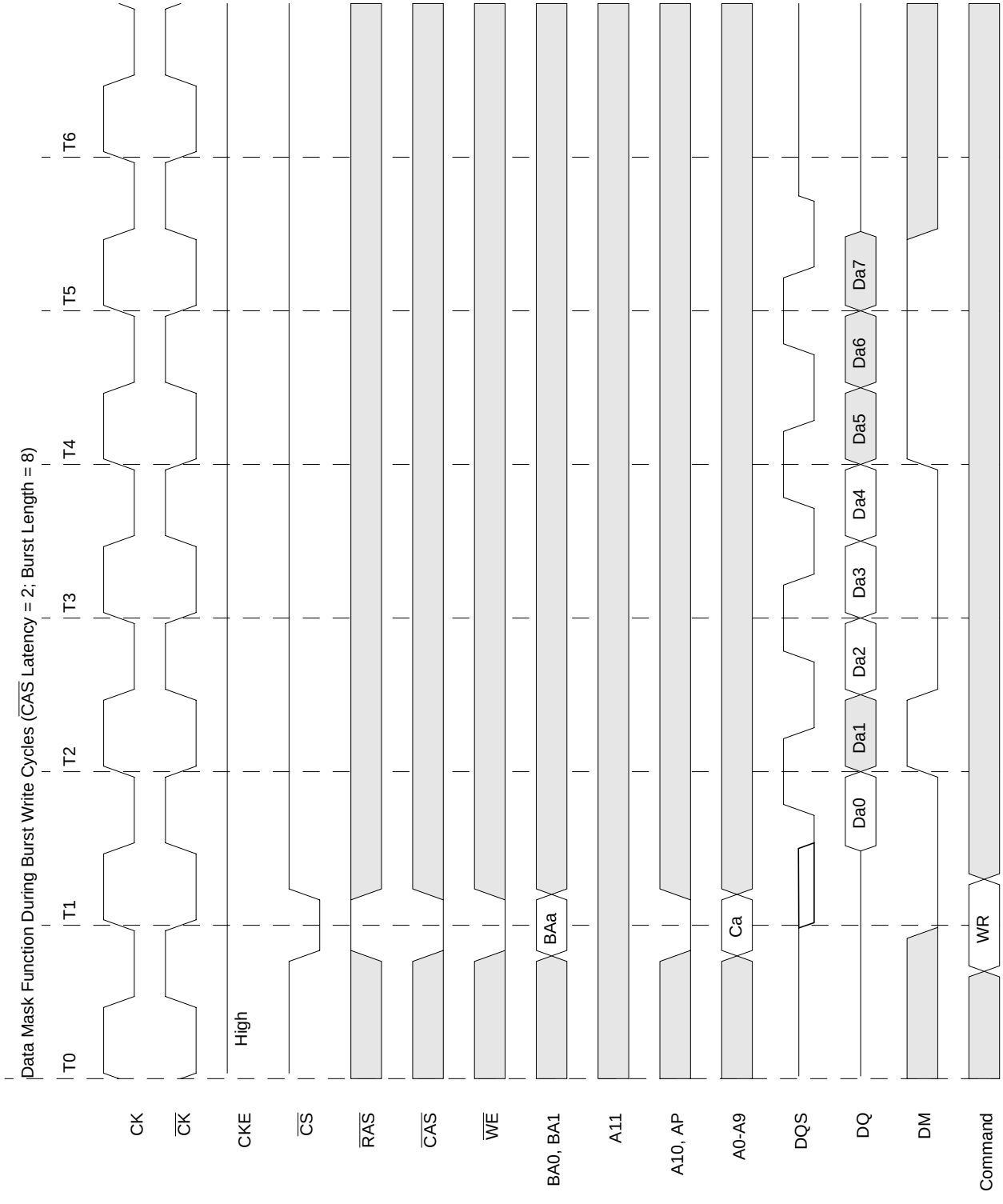
Write Burst


Write Burst (Burst Length = 4)
T0
T1
T2
T3
T4
T5
T6
tWR
High
BAa
Ca
Da0
Da1
Da2
Da3
WR
PRE
CLK
CLK
CKE
CS
RAS
CAS
WE
BA0, BA1
A11
A10, AP
A0-A9
DQS
DQ
DM
Command

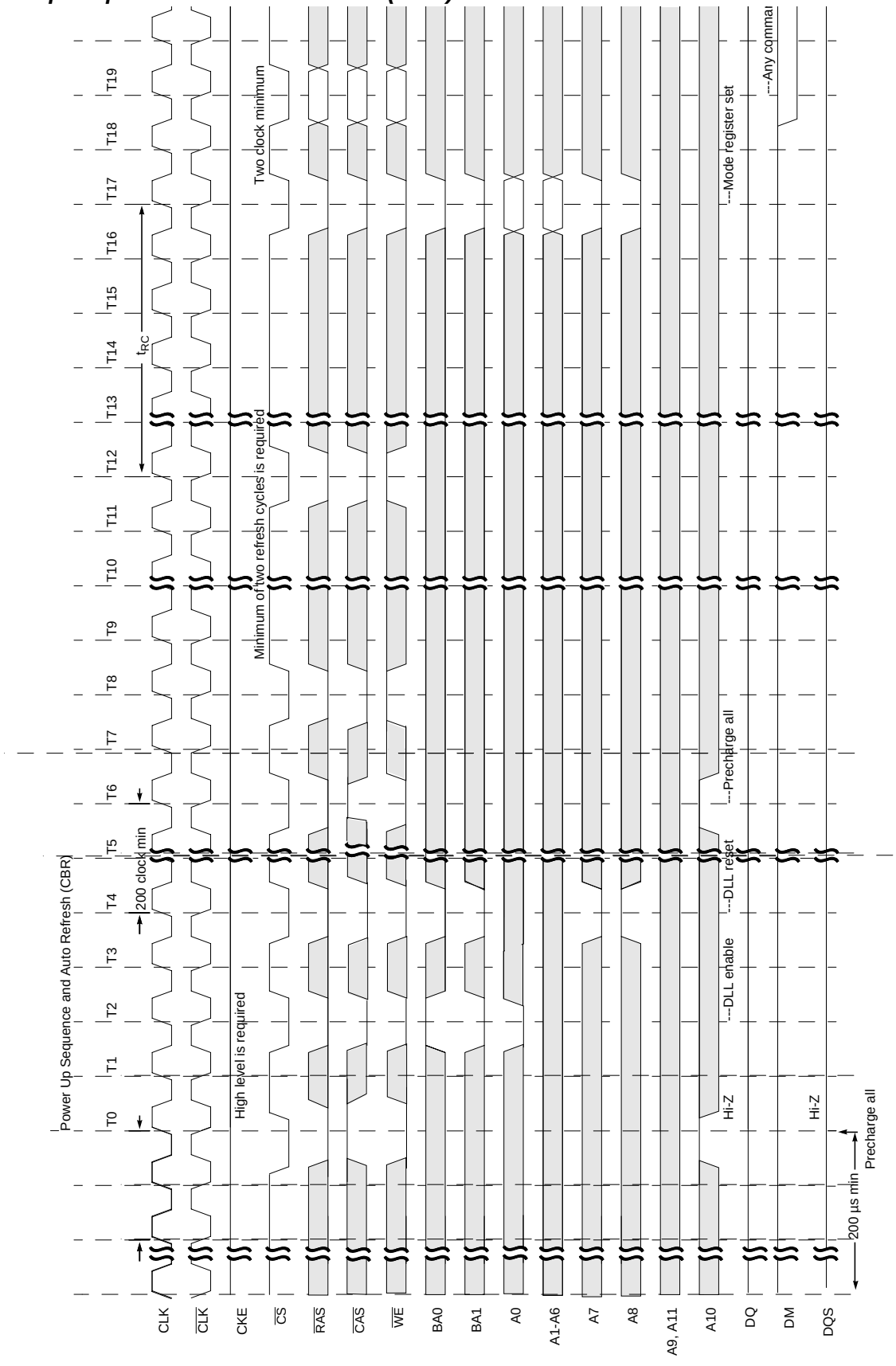
Read Interrupted by a Write and Burst Stop



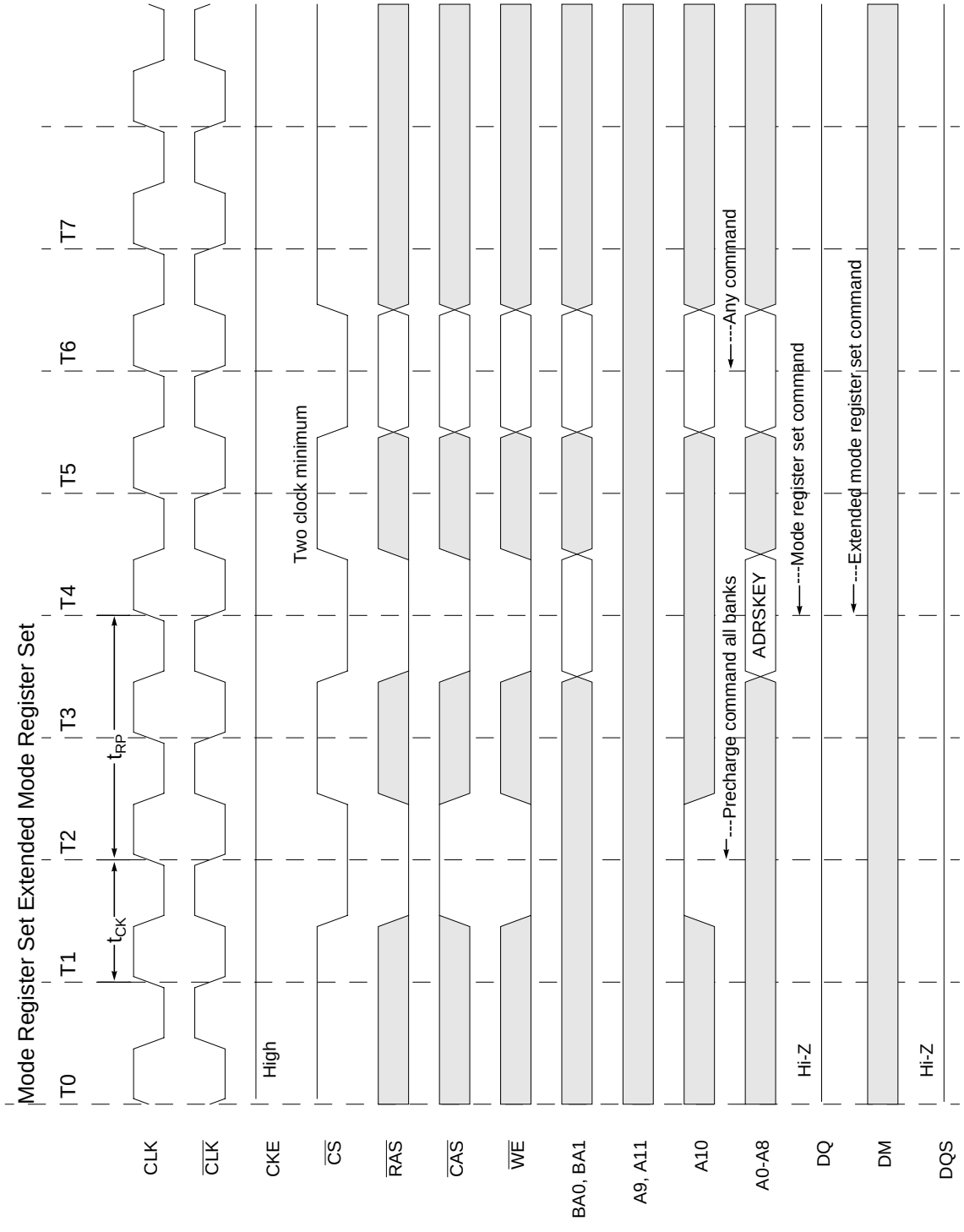
Data Mask Function (@BL=8) Only for Write



Power up Sequence and Auto Refresh (CBR)

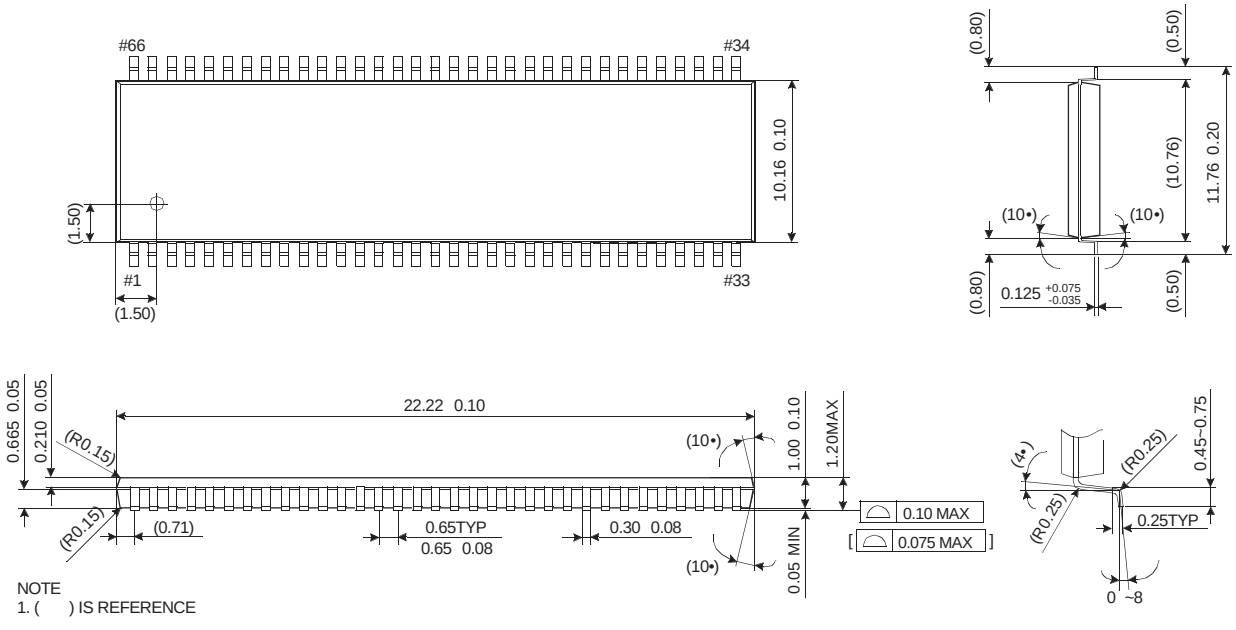


Mode Register/Extended Mode Register Set



Package Diagram
66-Pin TSOP-II (400 mil)

Units : Millimeters



NOTE
1. ( ) IS REFERENCE

WORLDWIDE OFFICES

U.S.A.
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

TAIWAN
7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

NO 19 LI HSIN ROAD
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

SINGAPORE
10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-6323-1801
FAX: 65-6323-7013

JAPAN
ONZE 1852 BUILDING 6F
2-14-6 SHINTOMI, CHUO-KU
TOKYO 104-0041
PHONE: 03-3537-1400
FAX: 03-3537-1402

UK & IRELAND
SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 44-1698-748515
FAX: 44-1698-748516

U.S. SALES OFFICES

WEST
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

CENTRAL / EAST
604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 214-352-3775
FAX: 214-904-9029