VERSA1: FULLY INTEGRATED MICROCONTROLLER WITH DSP

Datasheet Rev 2.2

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Overview

The VERSA1 is a fully integrated, high performance microcontroller based data acquisition system designed to provide single chip solutions. Innovative in its architecture, the VERSA1 includes a set of non-traditional onboard components like a programmable current source driver, which can be used to excite traditional resistive components such as resistive bridges or a thermistor, and a proprietary MAC block, which allows the user to perform mathematical calculations to a much higher degree of accuracy and speed than standard methods.

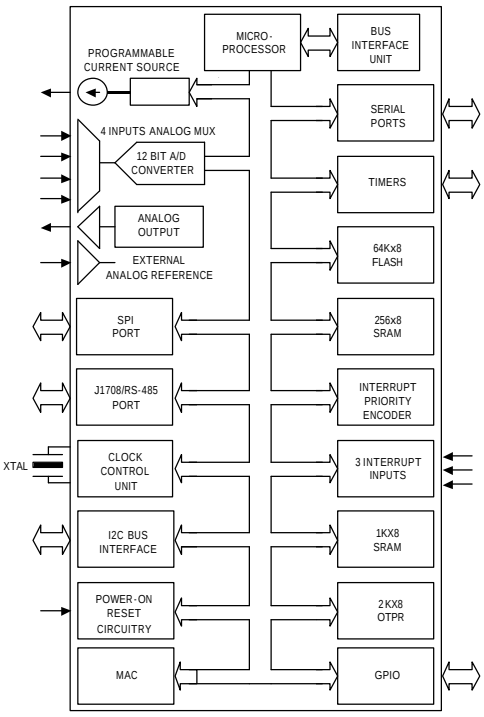
Applications

- Automotive Applications
- Medical Devices
- Industrial Controls / Measurement Systems
- Intelligent Sensors (IEEE 1451.2 Compatible)
- Instrumentation
- Consumer Products
- Battery Powered Systems (Instruments, Monitors)
- Pattern Recognition

Functional Diagram

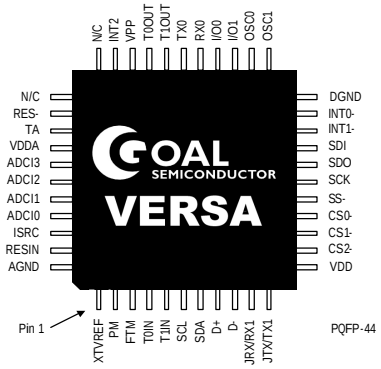
The following figure shows the functional diagram of the VERSA1.

FIGURE 1 FUNCTIONAL DIAGRAM



Features

- 4 Channel Calibrated 12-bit A/D Converter
  - o 0-2.7 Volts Input Range
  - o Programmable Continuous Free-Running Conversion (Single or all 4 Channels) with Interrupt to Processor
  - o Programmable One-Shot Conversion (Single or all 4 Channels)
- On-Chip Temperature Calibrated Precision Reference Voltage
- Analog Output/Reference Loop-Back
- Programmable Current Source
  - o 33/133µA Drive (Software Programmable)
- 8051 Compatible µProcessor
  - o Standard 8051 Instruction Set
  - o Dual Data Pointers
  - o 4 Clocks/Instruction
  - o 2.5x Average Improvement in Instruction Execution Time over Standard 8051
  - o Supports industry standard compilers, assemblers, emulators, and ROM monitors
- DSP Function via MAC
- On-chip Flash Memory
  - o 64Kx8 Program/Storage Memory
  - o 2Kx8 OTPR General Storage Memory Block
  - o Flash Programming via I^2C Interface
- On-chip SRAM
  - o 1Kx8 Scratch Pad SRAM Mapped into External Memory Space
  - o 256x8 SRAM Mapped into Internal Processor RAM
- RS-485/J1708 Bi-directional Transceiver
- 2 Full Duplex Asynchronous UARTS
- SPI Bus (Master/Slave)
  - o 3 Addressable Chip Enable Outputs for Controlling Multiple Slaves (Master Mode)
- 2 General Purpose I/Os
- 3 General Purpose Interrupt Inputs
- 3 General Purpose Timers/Counters
- Power Saving Features
- Power-on Reset with Brown-Out Detect
- Available in both Commercial and Industrial grade versions



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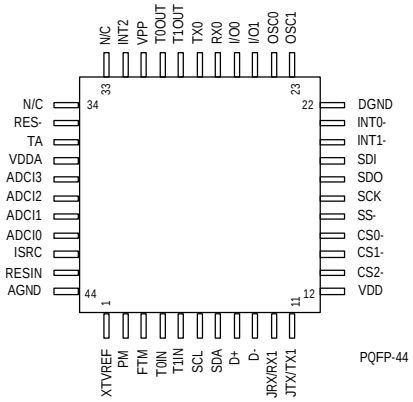
Pins Description

TABLE 1 PIN OUT DESCRIPTION

PIN	NAME	FUNCTION
1	XTVREF	External Reference Voltage Input (optional)
2	PM	Mode Control Input
3	FTM	Mode Control Input
4	T0IN	Timer 0 Input
5	T1IN	Timer 1 Input
6	SCL	I^2C Clock Input
7	SDA	I^2C Bi-directional Data Bus
8,9	D+, D-	RS-485 Differential Transceiver Bus
10	JRX/RX1	RS-485 External Differential Transceiver Input, or Asynchronous UART1 Receiver Input
11	JTX/TX1	RS-485 External Differential Transceiver Control Output, or Asynchronous UART1 Transmitter Output
12	VDD	Digital Logic Supply Input
13	CS2-	SPI Chip Enable Output (Master Mode)
14	CS1-	SPI Chip Enable Output (Master Mode)
15	CS0-	SPI Chip Enable Output (Master Mode)
16	SS-	SPI Chip Enable Input (Slave Mode)
17	SCK	SPI Clock (Input in Slave Mode, Output in Master Mode)
18	SDO	SPI Data Output Bus
19	SDI	SPI Data Input Bus
20	INT1-	Interrupt Input (Negative Level Triggered)
21	INT0-	Interrupt Input (Negative Level or Edge Triggered)
22	DGND	Digital Ground
23	OSC1	Oscillator Crystal Output
24	OSC0	Oscillator Crystal Input/External Clock Source Input
25	I/O1	Programmable I/O
26	I/O0	Programmable I/O
27	RX0	Asynchronous UART0 Receiver Input
28	TX0	Asynchronous UART0 Transmitter Output
29	T1OUT	Timer 1 Output
30	T0OUT	Timer 0 Output
31	VPP	Flash Programming Voltage Input
32	INT2	Interrupt Input (Positive Edge Triggered)
33	N/C	No Connection (leave pin unconnected)
34	N/C	No Connection (leave pin unconnected)
35	RES-	Hardware Reset Input
36	TA	Analog Output
37	VDDA	Analog Supply Input
38	ADCI3	Analog Input for Channel 3
39	ADCI2	Analog Input for Channel 2
40	ADCI1	Analog Input for Channel 1
41	ADCI0	Analog Input for Channel 0
42	ISRC	Programmable Current Source Output
43	RESIN	Current Source Reference Input
44	AGND	Analog Ground

Pin Configuration

FIGURE 2 VERSA1 PINOUT



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Absolute Maximum Ratings

V_{DD} to DGND	–0.3V, +6V	Digital Output Voltage to DGND	–0.3V, V_{DD}+0.3V
V_{DDA} to DGND	-0.3V, +6V	V_{PP} to DGND	+13V
AGND to DGND	–0.3V, +0.3V	Power Dissipation	
V_{DD} to V_{DDA}	-0.3V, +0.3V	• To +75°C	1000mW
ADCI(0-3) to AGND	-0.3V, V_{DDA}+0.3V	• Derate above +75°C	10mW/°C
XTVREF to AGND	-0.3V, V_{DDA}+0.3V	Operating Temperature range	-40° to +85°C
Digital Input Voltage to DGND	-0.3V, V_{DD}+0.3V	Storage Temperature Range	–65°C to +150°C
		Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

TABLE 2 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS (V_{DD} = +5V, V_{DDA} = +5V, T_A = +25°C, 16MHz input clock, unless otherwise noted.)						
Power Supply Voltage	V_{DD}		4.5	5.0	5.5	V
	V_{DDA}		4.5	5.0	5.5	V
V_{DDA} Power Supply Rejection						
Power Supply Current	I_{DD}		5.5	-	12.5	mA
	I_{DDA}		2.5	-	7.5	
Flash Programming Voltage	V_{PP}			+12		V
DIGITAL INPUTS						
Minimum High-Level Input Voltage	V_{IH}	V_{DD} = +5V		2.0		V
Maximum Low-Level Input Voltage	V_{IL}	V_{DD} = +5V		0.8		V
Input Current	I_{IN}			±0.05		µA
Input Capacitance	C_{IN}			5	10	pF
DIGITAL OUTPUTS						
Minimum High-Level Output Voltage	V_{OH}	I_{SOURCE} = 4mA		4.2		V
Maximum Low-Level Output Voltage	V_{OL}	I_{SINK} = 4mA		0.2		V
Output Capacitance	C_{OUT}			10	15	pF
Tri-state Output Leakage Current	I_{OZ}				0.25	µA
POWER SUPPLY MONITOR						
V_{DD} Trip Point	V_{TRIP}			3.75		V
ANALOG INPUTS						
ADCI(0-3) Input Voltage Range	V_{ADCI}		0		2.7	V
ADCI(0-3) Input Resistance	R_{ADCI}			100		MΩ
ADCI(0-3) Input Capacitance	C_{ADCI}			5		pF
ADCI(0-3) Input Leakage Current	I_{ADCI}			TBD		nA
Channel-to-Channel Crosstalk				TBD		dB
ANALOG OUTPUT						
TA Output Voltage (Note 1)	V_{TA}=$V_{ADCI(0-3)}$	(Note 2)		$V_{ADCI-IN}$		V
	V_{TA}=V_{BGI}	(Note 3)		1.23/1.179		
	V_{TA}=V_{BGH}	(Note 4)		1.23/1.179		
	V_{TA}=V_{ADC}			2.7		
	V_{TA}=V_{SR}	(Note 5)		200/800		mV
TA Output Drive Capabilities (Maximum Load Resistance)	V_{TA}=$V_{ADCI(0-3)}$		10			kΩ
	V_{TA}=V_{BGI}		Requires buffering			

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	$V_{TA=}V_{BGH}$	Must be buffered	10			
	$V_{TA=}V_{ADC}$		10			
	$V_{TA=}V_{SR}$		80			
TA Output Drive Capabilities (Maximum Load Capacitance)	$V_{TA=}V_{ADCI(0-3)}$				50	pF
	$V_{TA=}V_{BGI}$	Must be buffered			15	
	$V_{TA=}V_{BGH}$	Must be buffered			50	
	$V_{TA=}V_{ADC}$				50	
	$V_{TA=}V_{SR}$				5	
CURRENT SOURCE						
ISRC Current Drive	I_{ISRC}	(Note 6, Note7)		33/133	530uA	µA
ISRC Output Resistance	R_{ISRC}			50		MΩ
ISRC Output Capacitance	C_{ISRC}			25		pF
RESIN Input Reference Resistance	R_{RESIN}			100		MΩ
RESIN Input Reference Capacitance	C_{RESIN}			5		pF
INTERNAL REFERENCE						
Bandgap Reference Voltage				1.23/1.179		V
Bandgap Reference Tempco				7		ppm/°C
EXTERNAL REFERENCE						
Input Impedance	R_{XTVREF}			100		MΩ
PGA						
PGA Gain adjustment			2.15		2.36	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG TO DIGITAL CONVERTER						
ADC Resolution				12		Bits
Differential Non linearity	DNL	No missing codes guaranteed			±1	LSB
Integral Non linearity	INL				±1	LSB
Full-Scale Error (Gain Error)		All channels, ADCI(0-3)		±4		LSB
Offset Error		All channels, ADCI(0-3)		±0.5		LSB
Channel-to-Channel Mismatch		All channels, ADCI(0-3)		±0.5		LSB
Conversion Time		4 channels			1.75	ms
		Single Channel			0.5	
RS-485 TRANSCEIVER						
Input hysteresis			0		80	mV
Input Voltage			-5		+10	V
Input Common Mode			-2.5		+7.5	V
Input Impedance				1		MΩ
Output Drive Current				30	50	mA

Note 1: TA is the output of an analog multiplexer that can be programmed to switch through one of eight analog inputs $-V_{ADCI(0-3)}$, V_{BGI}, V_{BGH}, V_{ADC} and V_{SR}, which correspond to the 4 analog inputs to the VERSA1, on-chip Bandgap reference, a buffered on-chip reference, on-chip ADC reference and current source reference, respectively.

Note 2: $V_{ADCI(0-3)}$ are buffered versions of the $V_{ADCI(0-3)}$ inputs to the VERSA1.

Note 3: The V_{BGI} reference can be programmed for a 1st or 2nd order correction of the internal voltage reference.

Note 4: The V_{BGH} signal can be programmed to be derived from the on-chip Bandgap reference this signal is buffered.

Note 5: The V_{SR} is the voltage reference used for the on-chip current source. This can be programmed for two values: 200 and 800mV.

Note 6: The on-chip current source can be programmed to provide 2 current values: 33 and 133µA. using the calibrated internal Bandgap reference and a 6.00k precision feedback resistor between RESIN and analog Ground.

Note 7: The Feedback resistor between RESIN and analog Ground can be lowered to 1.5k resulting in an ISRC maximum output of about 530uA. In such conditions, the resistive element between ISRC output and RESIN should have > 1k in value.

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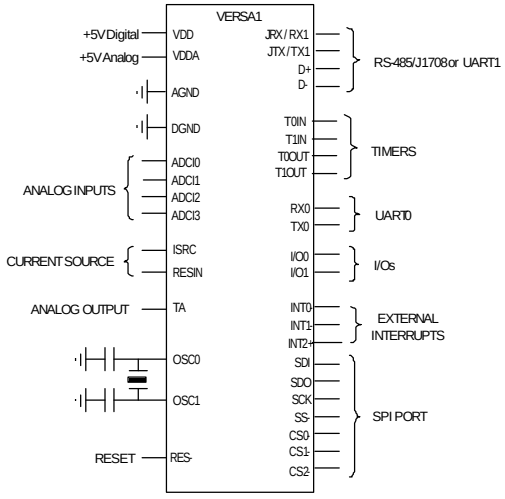
Detailed Description

The following sections will describe the VERSA1 architecture and peripherals.

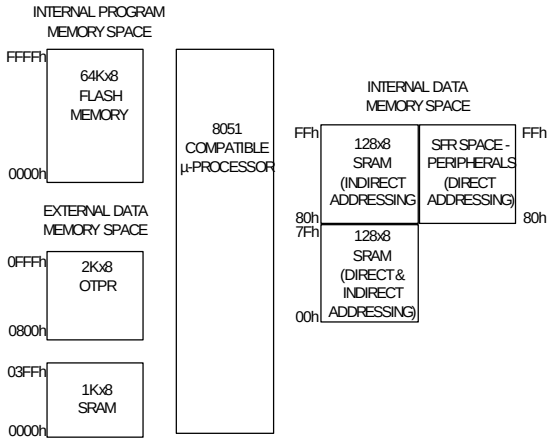
FIGURE 3 OPERATIONAL DIAGRAM FOR THE VERSA1



Memory Organization

The following figure shows the memory organization of the VERSA1.

FIGURE 4 MEMORY ORGANIZATION OF THE VERSA1

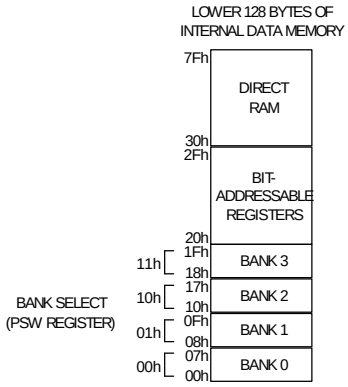


At power-up/reset code is executed from the 64Kx8 Flash memory mapped into the processor's internal ROM space. An extra 2Kx8 of Secondary Flash memory is mapped into the external data memory space.

Note that 0000–0005h and 0195–0210h are reserved in the OTPR. A 1Kx8 block of SRAM is also mapped into the external data memory of the VERSA1. This block can be used as general-purpose scratch pad or storage memory. A 256x8 block of SRAM is mapped to the internal data memory space. This block of RAM is broken into 2 sub-blocks, with the upper block accessible via indirect addressing only, and the lower block accessible via both direct and indirect addressing.

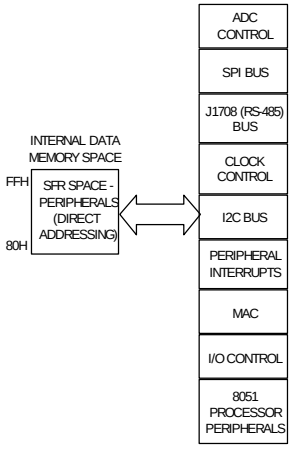
The following figure describes access to the lower block of 128 bytes.

FIGURE 5 LOWER BLOCK INTERNAL MEMORY MAP



The SFR (Special Function Register) space is also mapped into the upper 128 bytes of internal data memory space. This SFR space is accessible via direct-access only. The SFR space provides the interface to all the on-chip peripherals. The following figure describes this interface.

FIGURE 6 SFR SPACE ORGANIZATION



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Instruction Set

All VERSA1 instructions are binary code compatible and perform the same functions that they do in the industry standard 8051. However, the timing of the instructions is different. The following two tables describe the instruction set of the VERSA1.

TABLE 3 LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 4 VERSA1 INSTRUCTION SET

Mnemonic	Description	Size (bytes)	Instr. Cycles
Arithmetic instructions			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract data memy from A with borrow	1	1
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment data memory	1	1
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement data memory	1	1
INC DPTR	Increment data pointer	1	3
MUL AB	Multiply A by B	1	5
DIV AB	Divide A by B	1	5
DA A	Decimal adjust A	1	1
Logical Instructions			
ANL A, Rn	AND register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate data to direct byte	3	3
ORL A, Rn	OR register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate data to direct byte	3	3
XRL A, Rn	Exclusive-OR register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR data memory to A	1	1
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Compliment A	1	1
SWAP A	Swap nibbles of A	1	1
RLA	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RRA	Rotate A right	1	1
RRCA	Rotate A right through carry	1	1
Data Transfer Instructions			
MOV A, Rn	Move register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, #data	Move immediate to register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move data memory to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to data memory	1	1
MOV @Ri, direct	Move direct byte to data memory	2	2
MOV @Ri, #data	Move immediate to data memory	2	2
MOV DPTR, #data	Move immediate to data pointer	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (A8) to A	1	3
MOVX A, @DPTR	Move external data (A16) to A	1	3
MOVX @Ri, A	Move A to external data (A8)	1	3
MOVX @DPTR, A	Move A to external data (A16)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange A and register	1	1
XCH A, direct	Exchange A and direct byte	2	2
XCH A, @Ri	Exchange A and data memory	1	1
XCHD A, @Ri	Exchange A and data memory nibble	1	1
Branching Instructions			
ACALL addr 11	Absolute call to subroutine	2	3
LCALL addr 16	Long call to subroutine	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr 11	Absolute jump unconditional	2	3
LJMP addr 16	Long jump unconditional	3	4
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JB bit, rel	Jump on direct bit = 1	3	4
JNB bit, rel	Jump on direct bit = 0	3	4
JBC bit, rel	Jump on direct bit = 1 and clear	3	4
JMP @A+DPTR	Jump indirect relative DPTR	1	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator 1= 0	2	3
CJNE A, direct, rel	Compare A, direct JNE relative	3	4
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	4
DJNZ Rn, rel	Decrement register, JNZ relative	2	3
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous Instruction			
NOP	No operation	1	1

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Special Function Registers

The Special Function Registers (SFRs) control several of the features of the VERSA1. Most of the VERSA1 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051.

TABLE 5 SPECIAL FUNCTION REGISTERS

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
SP	81h	-	-	-	-	-	-	-	-	0000 0111b
DPL0	82h	-	-	-	-	-	-	-	-	0000 0000b
DPH0	83h	-	-	-	-	-	-	-	-	0000 0000b
DPL1	84h	-	-	-	-	-	-	-	-	0000 0000b
DPH1	85h	-	-	-	-	-	-	-	-	0000 0000b
DPS	86h	0	0	0	0	0	0	0	SEL	0000 0000b
PCON	87h	SMOD0	0	1	1	GF1	GF0	0	0	0011 0000b
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000b
TMOD	89h	GATE	C/!T	M1	M0	GATE	C/!T	M1	M0	0000 0000b
TL0	8Ah	-	-	-	-	-	-	-	-	0000 0000b
TL1	8Bh	-	-	-	-	-	-	-	-	0000 0000b
TH0	8Ch	-	-	-	-	-	-	-	-	0000 0000b
TH1	8Dh	-	-	-	-	-	-	-	-	0000 0000b
CKCON	8Eh	0	0	T2M	T1M	T0M	0	0	1	0000 0001b
SPC_FNC	8Fh	0	0	0	0	0	0	0	WRS	0000 0000b
EXIF	91h	-	-	IE3	IE2	1	0	0	0	0000 1000b
MPAGE	92h	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	0000 0000b
ADCCTRL	94h	SV0	MANUAL	ONESHOT	ADCENABLE	ADCIC	ADCIE	CONT	BGENABLE	0000 0000b
BGAPCAL	95h	-	-	-	-	-	-	-	-	0000 0000b
ADCALADR	96h	0	0	0	CALDSBL	CALADR3	CALADR2	CALADR1	CALADR0	0000 0000b
ADCALDAT	97h	0	0	0	DTBL4	DTBL3	DTBL2	DTBL1	DTBL0	0000 0000b
SCON0	98h	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	0000 0000b
SBUF0	99h	-	-	-	-	-	-	-	-	0000 0000b
ADCSTAT	9Ch	0	0	0	0	0	0	0	ADCINT	0000 0000b
ADCD0LO	A4h	ADCD7_0	ADCD6_0	ADCD5_0	ADCD4_0	ADCD3_0	ADCD2_0	ADCD1_0	ADCD0_0	0000 0000b
ADCD0HI	A5h	0	0	0	0	ADCD11_0	ADCD10_0	ADCD9_0	ADCD8_0	0000 0000b
ADCD1LO	A6h	ADCD7_1	ADCD6_1	ADCD5_1	ADCD4_1	ADCD3_1	ADCD2_1	ADCD1_1	ADCD0_1	0000 0000b
ADCD1HI	A7h	0	0	0	0	ADCD11_1	ADCD10_1	ADCD9_1	ADCD8_1	0000 0000b
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	0000 0000b
ADCD2LO	ACh	ADCD7_2	ADCD6_2	ADCD5_2	ADCD4_2	ADCD3_2	ADCD2_2	ADCD1_2	ADCD0_2	0000 0000b
ADCD2HI	ADh	0	0	0	0	ADCD11_2	ADCD10_2	ADCD9_2	ADCD8_2	0000 0000b
ADCD3LO	AEh	ADCD7_3	ADCD6_3	ADCD5_3	ADCD4_3	ADCD3_3	ADCD2_3	ADCD1_3	ADCD0_3	0000 0000b
ADCD3HI	AFh	0	0	0	0	ADCD11_3	ADCD10_3	ADCD9_3	ADCD8_3	0000 0000b
SPICTRL	B4h	0	0	SPICSS_1	SPI_CSS_0	SPIMCLK_1	SPIMCLK_0	SPICLKP	SPIMA_SL	0000 0000b
SPIRX	B5h	-	-	-	-	-	-	-	-	0000 0000b
SPITX	B6h	-	-	-	-	-	-	-	-	0000 0000b
SPIIE	B7h	0	0	0	0	0	SPIRXOVIE	SPIRXDAIE	SPITXEMPIE	0000 0000b
IP	B8h	1	0	0	PS0	PT1	PX1	PT0	PX0	1000 0000b
IOCTRL	BAh	0	0	0	0	IODIRCTRL1	IOOUT1	IODIRCTRL0	IOOUT0	0000 0000b
IOREAD	BBh	0	0	0	0	0	0	IOREAD1	IOREAD0	0000 0000b
SPIINTSTAT	BCh	0	0	0	0	0	SPIRXOV	SPIRXDA	SPITXEMP	0000 0000b
SPIRXOVC	BDh	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	0000 0000b
SCON1	C0h	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	0000 0000b
SBUF1	C1h	-	-	-	-	-	-	-	-	0000 0000b
MACACC0*	C4h	-	-	-	-	-	-	-	-	0000 0000b
MACACC1*	C5h	-	-	-	-	-	-	-	-	0000 0000b
MACACC2*	C6h	-	-	-	-	-	-	-	-	0000 0000b

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
MACACC3*	C7h	-	-	-	-	-	-	-	-	0000 0000b
T2CON	C8h	TF2	FIRQT2	RCLK0	TCLK0	0	TR2	T2=0	-RL2	0000 0000b
RCAP2L	CAh	-	-	-	-	-	-	-	-	0000 0000b
RCAP2H	CBh	-	-	-	-	-	-	-	-	0000 0000b
TL2	CCh	-	-	-	-	-	-	-	-	0000 0000b
TH2	CDh	-	-	-	-	-	-	-	-	0000 0000b
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000b
J17CTRL	D7h	J17ACTIVATE	J17IOCTRL	-	J17EOPACKET	J17TXERRC	J17TXEMPC	J17RXOVCLR	J17RXDACLR	0000 0100b
EICON	D8h	SMOD1	1	EPFI	PFI	INT2	0	0	0	0100 0000b
J17PRIREG	D9h	-	-	-	-	-	-	-	-	0000 0000b
J17IDLE	DAh	-	-	-	-	-	-	-	-	1111 1111b
J17BDLO	DBh	-	-	-	-	-	-	-	-	1111 1111b
J17BDHI	DCh	-	-	-	-	-	-	-	-	1111 1111b
J17DATA	DDh	-	-	-	-	-	-	-	-	0000 0000b
J17IE	DEh	0	0	0	0	J17TXEMPIE	J17TXERRIE	J17RXOVIE	J17RXDAIE	0000 0000b
J17INTSTAT	DFh	0	0	J17BUSRDY	J17BUSIDLE	J17TXERR	J17TXEMP	J17RXOVR	J17RXDA	0000 0000b
ACC	E0h	-	-	-	-	-	-	-	-	0000 0000b
INTSRC	E4h	-	-	-	-	-	-	-	-	0000 0000b
CLKDIV	E5h	0	0	0	0	DIVCTL_2	DIVCTL_1	DIVCTL_0	NORMSPD	0000 0000b
MACA0*	E6h	-	-	-	-	-	-	-	-	0000 0000b
MACA1*	E7h	-	-	-	-	-	-	-	-	0000 0000b
EIE	E8h	1	1	1	EIE2	0	0	EX3	EX2	1110 0000b
MACRES0*	Eah	-	-	-	-	-	-	-	-	0000 0000b
MACRES1*	Ebh	-	-	-	-	-	-	-	-	0000 0000b
MACRES2*	ECh	-	-	-	-	-	-	-	-	0000 0000b
MACRES3*	EDh	-	-	-	-	-	-	-	-	0000 0000b
MACB0*	Eeh	-	-	-	-	-	-	-	-	0000 0000b
MACB1*	Efh	-	-	-	-	-	-	-	-	0000 0000b
B	F0h	-	-	-	-	-	-	-	-	0000 0000b
CONVRLO	F5h	-	-	-	-	-	-	-	-	0000 0000b
CONVRMED	F6h	-	-	-	-	-	-	-	-	0000 0000b
CONVRHI	F7h	-	-	-	-	-	-	-	-	0000 0000b
EIP	F8h	1	1	1	PEI2	0	0	PEX3	PEX2	1110 0000b
PGACTRL	F9h	DPGA6	DPGA5	DPGA4	DPGA3	DPGA2	DPGA1	DPGA0	PGAENABLE	0000 0000b
ISRC1	Fah	C1_6	C1_5	C1_4	C1_3	C1_2	C1_1	C1_0	ISRCENABLE	0000 0000b
ISRC2	FBh	C4_6	C4_5	C4_4	C4_3	C4_2	C4_1	C4_0	SV1	0000 0000b
INMUX	FCh	BGAPORDER	MUXCTRL_2	MUXCTRL_1	MUXCTRL_0	IBUFEN_3	IBUFEN_2	IBUFEN_1	IBUFEN_0	0000 0000b
OUTMUX	FDh	0	0	0	-	MUXB_2	MUXB_1	MUXB_0	TAENABLE	0000 0000b
ADCCkDIV	FEh	-	-	-	-	-	-	-	-	0000 0000b

Notes: *These registers are write only, **These registers are read only

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Peripheral Interfaces

(This section briefly describes the VERSA1 peripherals. For more detailed information, please refer to the VERSA1 User's Guide)

Dual Data Pointers

The VERSA1 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The VERSA1 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify the code to use DPTR0.

Timers/Counters

The VERSA1 includes three timer/counters (Timer 0, Timer 1, Timer 2). Timer 0 and Timer 1 can operate as either a timer with a clock rate based on the system clock, or as an event counter clocked by the T0IN (Timer 0) and T1IN (Timer 1). Timer 2 can only operate in 16bits timer mode. It can serve as serial port baud rate generator.

Each timer/counter consists of a 16-bit register that is accessible by software as two SFRs:

- **Timer 0** -TL0 and TH0
- **Timer 1** -TL1 and TH1
- **Timer2** -TL2 and TH2

Timers 0 and 1

Timers 0 and 1 each operate in four modes, as controlled through the TMOD SFR and the TCON SFR. The four modes are:

- **13-bit** timer/counter (mode 0)
- **16-bit** timer/counter (mode 1)
- **8-bit** counter with auto-reload (mode 2)
- **Two** 8-bit counters (mode 3)

Mode 0

Mode 0 operation is the same for Timer 0 and Timer 1. In mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of TL0 (or TL 1) and all 8 bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/!T bit selects the timer/counter clock source, clk or T0IN/T1IN.

When the 13-bit count increments from 1FFFh (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the T0OUT (or T1OUT) pin goes high for one clock cycle.

The upper 3 bits of TL0 (or TL1) are indeterminate in mode 0 and must be masked when the software evaluates the register.

Mode1

Mode 1 operation is the same for Timer 0 and Timer 1. In mode 1, the timer is configured as a 16-bit counter. The counter rolls over to all zeros (0000h) upon surpassing FFFFh. Otherwise, mode 1 operation is the same as mode 0.

Mode 2

Mode 2 operation is the same for Timer 0 and Timer 1. In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter and the MSB register (TH0 or TH1) stores the reload value.

The Mode 2 counter control is the same as for mode 0 and mode 1. However, in mode 2, when TLn surpasses FFh, the value stored in THn is reloaded into TLn.

Mode 3

In mode 3, Timer 0 operates as two 8-bit counters and Timer 1 stops counting and holds its value.

Timers 0, 1, 2 Rate Control

The default timer clock scheme for the VERSA1 timers is 12 *clk* cycles per increment, the same as in the standard 8051. However, applications that require fast timing can set the timers to increment every 4 *clk* cycles by setting bits in the Clock Control register CKCON.

The CKCON bits that control the timer clock rates are:

CKCON bit	Counter/Timer
5	Timer 2
4	Timer 1
3	Timer 0

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Timer 2

Timer 2 runs only in 16-bit modes and offers the following functionalities:

- 16-bit timer
- 16-bit auto-reload timer
- 16 bit precision Baud rate generator

Using Timer 2 as a baud rate generator for serial port 0, permit much more flexibility of baud rate adjustment.

Timer 2 16-bit Timer Modes

In timer modes, clocking of Timer 2 is only possible through system clock divided by 4 or by 12 depending of T2M bit value. For this reason, T2 bit must be always set to 0. There is no output pin for Timer 2. Setting TR2 bit permit to start Timer 2.

When the Timer 2 count overflows from FFFFh, the TF2 flag is set, raising a Timer 2 interrupt if enabled.

When -RL2 = 0, Timer 2 is configured for the auto-reload mode. When the count increment from FFFFh, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2 from RCAP2L and RCAP2H registers.

Timer 2 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow generates a shift clock for the serial port function. In this mode, the overflow causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation.

When operating as a baud rate generator, Timer 2 does not set the TF2 bit and the counter time base in baud rate generator mode is clk/2.

Serial Interface

The VERSA1 provides two serial ports: Serial Port 0 and Serial port 1.

Serial Port 0 has dedicated I/O pins Rx and Tx pins, while Serial port 1 share its pin with J1708 interface's JRX and JTX pins and can only be used if the RS-485/J1708 device is turned off by setting the J17ACTIVATE bit of the J1708 Control Register (SFR D7h) to 0.

Both serial ports operate in full duplex asynchronous mode. The VERSA1 buffers receive data in a holding register, enabling the UART to receive an incoming word before the software has read the previous value.

The clock source for serial port 0 can be provided by Timer 1 or Timer 2. In the case of serial port 1, only Timer 1 can be used as the clock source.

It is possible to use an external clock source to drive Timer 0 and Timer 1 through T0IN and T1IN pin respectively.

Serial port Interrupt mapping

Both serial ports 0 and serial port 1 have a dedicated interrupt line that allow the processor to be interrupted upon the completion of a byte transmission or reception. When such an interrupt takes place, the software must check the status of the RI and TI bits of the appropriate SCON register to determine the source of the interrupt (transmission end or reception)

TABLE 6: INTERRUPT VECTORS OF SERIAL PORT 0 AND SERIAL PORT 1

Interrupt	Interrupt Vector
Serial port 0 Rx & Tx	23h
Serial port 1 Rx & Tx	3Bh

Mode 1

Mode 1 provides standard asynchronous, full-duplex communication, using a total of 10 bits: 1 start bit, 8 data bits, and 1 stop bit. For receive operations, the stop bit is stored in RB8_0 (or RB8_1). Data bits are received and transmitted LSB first.

Mode 1 Baud Rate Using Timer 1

The mode 1 baud rate is a function of timer overflow. Both Serial Ports can use Timer 1 to generate baud rates. Each time the timer increments from its maximum count, a clock is sent to the baud rate circuit. The clock is then divided by 16 to generate the baud rate. When using Timer 1, the SMOD0/1 bit selects whether or not to divide the Timer 1 rollover rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{2^{\text{SMOD0/1}}}{32} \times \text{Timer 1 Overflow}$$

For serial port 0 use SMOD0 (SFR bit PCON.7)
For serial port 1 use SMOD1 (SFR bit EICON.7)

To use Timer 1 as the baud rate generator, it is best to use Timer 1 in mode 2 (8-bit counter with auto-reload), although any counter mode can be used. The Timer 1 reload value is stored in the TH 1 register, which makes the complete formulas for Timer 1. **Table 4** shows the formulas to calculate baud rate or TH1 register value when using Timer 1 in mode 2:

TABLE 7 – EQUATION TO CALCULATE BAUD-RATE OR TIMER 1 RELOAD VALUE (IN MODE 1)

For TM1 = 0 (standard mode)
$\text{Baud Rate} = \frac{2^{\text{SMOD0/1}}}{32} \times \frac{\text{clk}}{12 \times (256 - \text{TH1})}$
$\text{TH1} = 256 - \frac{2^{\text{SMOD0/1}} \times \text{clk}}{384 \times \text{Baud Rate}}$
For TM1 = 1 (Fast Mode)
$\text{Baud Rate} = \frac{2^{\text{SMOD0/1}}}{32} \times \frac{\text{clk}}{4 \times (256 - \text{TH1})}$
$\text{TH1} = 256 - \frac{2^{\text{SMOD0/1}} \times \text{clk}}{128 \times \text{Baud Rate}}$

**Where clk = system clock which is Fosc / 2 (clk divider = reset value)*

Mode 1 Baud Rate Using Timer 2

(Serial Port 0 only)

Timer 2 can be used to generate baud rates for serial port 0 only. When used as the baud rate generator Timer 2 increment rate is defined as clk/2. Each time Timer 2

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overflows a clock pulse is sent to the serial port interface. This clock is then divided by 16 to generate the baud rate.

To use Timer 1 as the baud rate generator, it is best to use Timer 2 in 16 bits auto-reload. The 16 bits Timer 2 reload value is stored in the RCAP2H and RCAP2L registers.

TABLE 8 – EQUATIONS TO CALCULATE BAUD-RATE OR TIMER 2 RELOAD VALUE

Baud Rate = $\frac{clk}{32 \times (65536 - \textbf{RCAP2H, 2L})}$
RCAP2H, 2L = $\frac{clk}{32x\ (65536 - \textbf{Baud Rate})}$

**Where clk = system clock which is Fosc / 2 (clk divider = reset value)*

Having 16 bits resolution for baud rate adjustment, permit wider baud rate adjustment for a given oscillator frequency.

Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8_0 (or TB8- 1). To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8_0 (or TB8_1).

The mode 2 baud rate is either *clk/32* or *clk/64,* as determined by the SMOD0 (or SMOD1) bit. The formula for the mode 2 baud rate is:

$$\text{Baud Rate} = \frac{2^{SMOD0} \times clk}{64}$$

**Where clk = system clock (which is Fosc / 2)*

Mode 2 operation is identical to the standard 8051.

Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first.

The mode 3 transmit and receive operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocol and mode 1 baud rate. Mode 3 operation is identical to that of the standard 8051 when Timers 1 and 2 use *clk/12* (the default).

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Analog Signal Path & A/D Converter

On the analog side, the VERSA1 provides the following features:

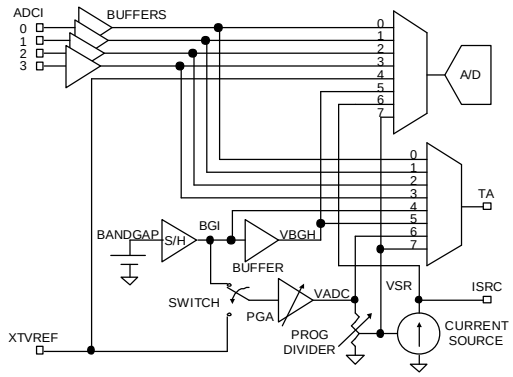
- 4 external input channels for A/D converter.
- Internal Band-Gap reference and PGA.
- Programmable current source.
- Input multiplexer.
- Multiplexed analog Output.

This permits the VERSA1 to be used as a single chip acquisition system.

Figure 7 shows the analog block of the VERSA1. The choice of an on-chip calibrated Bandgap or an external reference provides the basis for all derived on-chip voltages. These voltages are used as the reference signals for the ADC and the current source.

Four external analog inputs (ADCI) are buffered and applied to the A/D via an 8 to 1 multiplexer. The remaining four inputs of the multiplexer connect to internal derived voltages. The output multiplexer provides the ability to drive the buffered ADCI signals and the internal derived voltages outside the VERSA1 through the TA pin for applications that require external use of those voltages

FIGURE 7 ANALOG SIGNAL PATH OF THE VERSA1



The control of the internal versus external reference, the multiplexer's current source drive, ADC and their respective power downs are all done via µ-Processor control through SFR registers.

A/D Converter

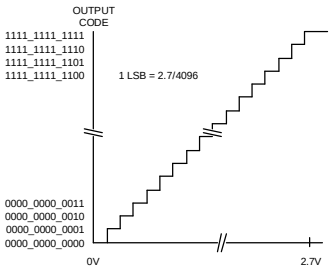
The on-chip A/D converter can be configured for a number of different operating modes to meet the specific application requirements. It supports both continuous and Single Shot modes.

The continuous Conversion mode sets the ADC to perform timed conversions of 1 or 4 channels and the single Shot conversion sets the ADC to perform one conversion of 1 or 4 channels at a given time.

When the ADC is configured to perform 4 channel conversions, the converted data will be available in a set of four 12 bits registers mapped into the processor's SFR space (ADC channels 0-3 registers). When the ADC is configured to perform the conversion on one channel only, the conversion result is always placed into the ADC channel 0 register.

The analog input voltage range for the ADC is 0 to 2.7V and the output coding is binary with 1 LSB = Full Scale/4096. The following describes the ideal transfer function for the VERSA1.

FIGURE 8 IDEAL A/D CONVERTER TRANSFER FUNCTION



Internal Bandgap reference and PGA

The VERSA1 provides an internal temperature stable Bandgap reference coupled to a programmable gain amplifier. These two units provide a reference voltage for the ADC as well as the internal programmable current source. Both Bandgap and PGA are calibrated during production. The associated calibration vectors are stored in the OTPR memory. It is also possible to use an external reference instead of using the internal Bandgap.

The following tables describe the SFR associated to the analog signal path units.

TABLE 9 ADC CONTROL REGISTER - SFR 94H

Bit	Mnemonic	Function
7	SV0	Controls switch for reference to PGA. 0 selects on-chip Bandgap. 1 selects external XTVREF input.
6	MANUAL	MANUAL = 1, the conversion on the channel whose address is defined by the value of MUXA[2:0] MAMUAL = 0,, conversion on the 4 upper/lower channels of input multiplexer depending on MUXA[2]
5	ONESHOT	When set 1 to the ADC will implement a single conversion of 1 or 4 channels.
4	ADCENABLE	When set to 0, this will power down the ADC.
3	ADCIC	When set to 1, this signal clears the ADC Interrupt.
2	ADCIE	When set to 1, this enables the ADC Interrupt to be driven to the Interrupt Control block.
1	CONT	When set to 1, this signal enables continuous ADC conversions of 1 or 4 channels.
0	BGENABLE	When set to 0, this signal powers down the on-chip Bandgap.

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TABLE 10 ADC STATUS REGISTER - SFR BCH

Bit	Mnemonic	Function
7-1	Not Used	
0	ADCINT	This signal provides the status of the ADC Interrupt and signals the end of an ADC conversion

TABLE 11 ADC CLOCK DIVIDER REGISTER - SFR FEH

Bit	Mnemonic	Function
7-0	ADCCDIV [7:0]	This 8 bit number controls the main clock that is required for the correct operation of the ADC. The user should ensure that the clock reference to the A/D is as clock to 250KHz as possible.

The user should ensure that the clock reference to the A/D is as close to 250KHz as possible using the following formula:

ADC Clk ref = (External Clock / 2) / [(2 * ADCCDIV) + 2]

For example, if the External Clock is 16MHz, then ADCCDIV should be set to 15 (0Fh).

TABLE 12 CONVERSION RATE HIGH REGISTER - SFR F7H

Bit	Mnemonic	Function
7-0	CONVRHI [7:0]	This register and the CONVRMED[7:0] & CONVRLO[7:0] registers for a 24 bit word that is used to set the time between continuous conversions of the ADC.

TABLE 13 CONVERSION RATE MED REGISTER - SFR F6H

Bit	Mnemonic	Function
7-0	CONVRMED [7:0]	This register and the CONVRHI [7:0] & CONVRLO[7:0] registers for a 24 bit word that is used to set the time between continuous conversions of the ADC.

TABLE 14 CONVERSION RATE LOW REGISTER - SFR F5H

Bit	Mnemonic	Function
7-0	CONVRLO [7:0]	This register and the CONVRHI [7:0] & CONVRMED[7:0] registers for a 24 bit word that is used to set the time between continuous conversions of the ADC.

The 24 bit CONV_RATE[23:0] register is used to set the conversion rate when in continuous conversion mode and is governed by the following formula:

Conversion Rate

register value(24bits) = [(Ext Clock / 2) / (CONV_RATE)]

TABLE 15 ADC INPUT MUX CONTROL REGISTER - SFR FCH

Bit	Mnemonic	Function
7	BGAPORDER	Controls order of on-chip Bandgap correction. When 0, correction is 1st order when 1 correction is 2nd order.
6-4	MUXA[2:0]	When in manual mode, this controls the source channel input to the A/D.
3-0	IBUFEN[3:0]	These signals each provide an active low power down for the input channel buffers.

TABLE 16 ADC CALIBRATE ADDRESS REGISTER - SFR 96H

Bit	Mnemonic	Function
7-5	Not Used	
4	CALDSBL	Skip the auto calibration phase of ADC if set to 1
3-0	CALADR[3:0]	Calibration table address register

TABLE 17 ADC CHANNEL 0 LOW REG - SFR A4H

Bit	Mnemonic	Function
7-0	ADCD0[7:0]	This provides a read back of the 8 LSBs of the ADCD0[11:0] register. Data corresponds to last ADC conversion.

TABLE 18 ADC CHANNEL 0 HIGH REG - SFR A5H

Bit	Mnemonic	Function
7-4	Not Used	
3-0	ADCD0[11:8]	This provides a read back of the 4 MSBs of the ADCD0[11:0] register. Data corresponds to last ADC conversion.

TABLE 19 ADC CHANNEL 1 LOW REG - SFR A6H

Bit	Mnemonic	Function
7-0	ADCD1LO [7:0]	This provides a read back of the 8 LSBs of the ADCD1[11:0] register. Data corresponds to last ADC conversion.

TABLE 20 ADC CHANNEL 1 HIGH REG - SFR A7H

Bit	Mnemonic	Function
7-4	Not Used	
3-0	ADCD1H1 [11:8]	This provides a read back of the 4 MSBs of the ADCD1 [11:0] register. Data corresponds to last ADC conversion.

TABLE 21 ADC CHANNEL 2 LOW REG - SFR ACH

Bit	Mnemonic	Function
7-0	ADCD2LO [7:0]	This provides a read back of the 8 LSBs of the ADCD2[11:0] register. Data corresponds to last ADC conversion.

TABLE 22 ADC CHANNEL 2 HIGH REG - SFR ADH

Bit	Mnemonic	Function
7-4	Not Used	
3-0	ADCD2HI [11:8]	This provides a read back of the 4 MSBs of the ADCD2[11:0] register. Data corresponds to last ADC conversion.

TABLE 23 ADC CHANNEL 3 LOW REG - SFR AEH

Bit	Mnemonic	Function
7-0	ADCD3LO [7:0]	This provides a read back of the 8 LSBs of the ADCD3 [11:0] register. Data corresponds to last ADC conversion.

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TABLE 24 ADC CHANNEL 3 HIGH REGISTER - SFR AFH

Bit	Mnemonic	Function
7-4	Not Used	
3-0	ADCD3HI [11:8]	This provides a read back of the 4 MSBs of the ADCD3[11:0] register. Data corresponds to last ADC conversion.

TABLE 25 BANDGAP CALIBRATE DATA REGISTER - SFR 95H

Bit	Mnemonic	Function
7-0	BGCAL	Bandgap Calibration Data

TABLE 26 ANALOG OUTPUT MUX CONTROL REGISTER - SFR FDH

Bit	Mnemonic	Function
7-4	Not Used	
3-1	MUXB[2:0]	This controls the signal that is selected to be driven out on the TA pin.
0	TAENABLE	A low on this signal disables the TA analog output.

TABLE 27 ADC CALIBRATE ADDRESS REGISTER

Bit	Mnemonic	Function
7-5	Not Used	
3-1	CALDSBL	Skip the auto calibration phase of ADC if set to 1
0	CALADR[3:0]	Calibration table address register.

TABLE 28 PGA CONTROL REGISTER - SFR F9H

Bit	Mnemonic	Function
7-1	DPGA[6:0]	Calibration data for the Programmable Gain Amplifier (PGA)
0	PGAENABLE	When set to 0, this signal powers down the PGA.

TABLE 29 CURRENT SOURCE CONTROL REGISTER 1 - SFR FAH

Bit	Mnemonic	Function
7-1	C1[6:0]	Calibration data for the programmable divider used by the 33µA current source
0	ISRCENABLE	When set to 0, this signal powers down the current source circuitry.

TABLE 30 CURRENT SOURCE CONTROL REGISTER 2 - SFR FBH

Bit	Mnemonic	Function
7-1	C4[6:0]	Calibration data for the programmable divider used by the 133µA current source
0	SV1	When set to 0, the programmable current source provides a 33µA signal and when set to 1, it provides 133µA signal.

OTPR Memory calibration Vectors

Each VERSA1 produced goes through an extensive test and calibration process during which functional tests are done on each peripheral and an individual calibration is done on the Band-Gap, the PGA and the programmable current source. These calibration parameters, called “Calibration Vectors” are stored in the OTPR memory of each VERSA1 and can be retrieved using MOVX instructions and stored in the appropriate SFRs.

When the ADC and/or ISRC are to be used in conjunction with the Internal Band-gap reference, it is recommended that these calibration vectors are retrieved and written to the appropriate SFR registers before these peripherals are used.

TABLE 31 – BAND-GAP, PGA AND ISRC CALIBRATION VECTORS LOCATION IN OTPR

Address	Parameter / Calibration Vector
B01h	Bgap cal Data
B03h	Input mux ctrl value (080h)
B05h	PGA CAL DATA
B07h	ISRC 200mV value
B09h	ISRC 800mV value

In the case where an external reference is used, it will be necessary to perform a calibration of the PGA and the current source at production time. For this purpose the TA output can be used to monitor the PGA output as well as the RESIN for current source calibration. See the Electrical parameters table for admissible values.

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SPI Interface

The VERSA1 SPI interface can operate as a master or slave device. In master mode, there are an additional 3 chip enable signals that can be used to allow 3 slave devices to share the SPI bus. The SPI interface is not affected by the clock divider. **Figure 10** describes the SPI bus timing:

FIGURE 9 SPI PIN INTERFACE

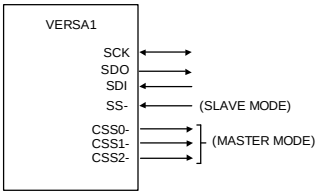
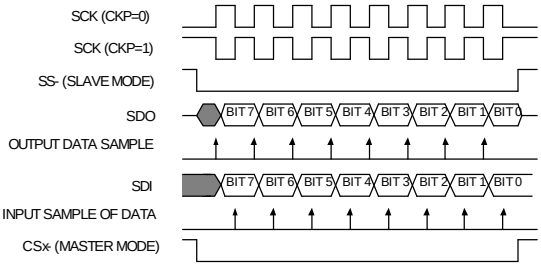


FIGURE 10 SPI SLAVE/MASTER MODE TIMING



The following describes the SFR interface to the SPI control registers.

TABLE 32 SPI CONTROL REGISTER - SFR B4H

Bit	Mnemonic	Function
7-6	Not Used	
5-4	CSSB [1:0]*	In master mode, this controls which chip enable is active during the SPI transfer. **CSSB CS2 CS1 CS0** 00b 1 1 0 01b 1 0 1 10b 0 1 1 11b 1 1 1
3-2	MCLK [1:0]	In master mode, this signal is used to select the clock speed of the SPI's clock (SCK) **MCLK [1:0] SCK (DIVIDE RATIO)** 00b External Clock ÷ 8 01b External Clock ÷ 16 10b External Clock ÷ 32 11b External Clock ÷ 64
1	SPICLKP	In slave or master mode, this signal controls the polarity of the SPI clock.
0	SPIMA_SL	When set to 0, the SPI will function as a slave device. When set to 1, the SPI will function as a master.

TABLE 33 SPI RECEIVE REGISTER - SFR B5H

Bit #	Mnemonic	Function
7-0	SPIRX [7:0]	This register is used to read the receive data from the SPI interface.

TABLE 34 SPI TRANSMIT REGISTER - SFR B6H

Bit	Mnemonic	Function
7-0	SPITX [7:0]	Data written to this register will be transmitted out to the SPI bus.

TABLE 35 SPI INTERRUPT ENABLE REGISTER - SFR B7H

Bit	Mnemonic	Function
7-3	Not Used	
2	SPIRXOVIE	When set to 1, this signal enables the receiver overrun interrupt to the processor.
1	SPIRXDAIE	When set to 1, this signal enables the receiver data available interrupt to the processor.
0	SPITXEMPIE	When set to 1, this signal enables the transmitter empty interrupt to the processor.

TABLE 36 SPI INTERRUPT STATUS REGISTER - SFR BCH

Bit	Mnemonic	Function
7-3	Not Used	
2	SPIRXOV	When set to 1, this signal indicates that the data in the SPI Receive register has been over-written.
1	SPIRXDA	When set to 1, this signal indicates that an SPI transaction has occurred and there is data available in the SPI Receive register.
0	SPITXEMP	When set to 1, this signal indicates that the SPI Transmit register is empty and is ready to receive data to be transmitted.

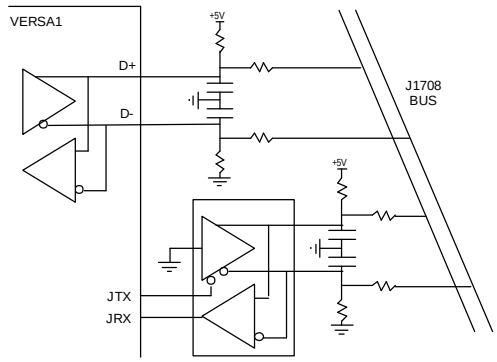
TABLE 37 SPI RECEIVER OVERRUN CLEAR - SFR BDH

Bit	Mnemonic	Function
7-0	SPIRXOVC	A write to this register will clear the SPIRXOV. Data written is a don't care.

RS-485/J1708 Circuitry

The following diagram shows the VERSA1 in a J1708 application. Both internal and external transceiver control modes are shown. External transceiver control mode is used when higher common mode rejection is required. Please note that the two transceivers cannot be used at the same time.

FIGURE 11: RS-485 / J1708 INTERFACE



The following describes the SFR interface to the J1708 control block.

TABLE 38 J1708 CONTROL REGISTER - SFR D7H

Bit	Mnemonic	Function
7	J17ACTIVATE	When set to 1, this activates the J1708
6	J17IOCTRL	When set to 0, the on-chip RS-485 transceiver is used to drive the J1708 bus. When set to 1, the J1708 external transceiver control signals are functional and the on-chip transceiver goes into power-down mode.
5	Not Used	
4	J17EOPACKT	If hardware sets to 1, the last byte received was the Start-Of-Packet (SOP) byte. Must be cleared by software.
3	J17TXERRC	If this bit is set to 0, the transmit error interrupt will be cleared.
2	J17TXEMPC	If this bit is set to 0, the transmitter buffer empty interrupt will be will be cleared.
1	J17RXOVCLR	If this bit is set to 0, the receiver overrun interrupt will be cleared.
0	J17RXDACLR	If this bit is set to 0, the receiver data available interrupt will be cleared.

TABLE 39 J1708 PRIORITY REGISTER - SFR D9H

Bit	Mnemonic	Function
7-0	J17PRIREG[7:0]	This 8-bit register is used to set the priority delay in relation to the input clock.

TABLE 40 J1708 IDLE TIME REGISTER - SFR DAH

Bit	Mnemonic	Function
7-0	J17IDLE [7:0]	This 8 bit register sets the number of delays necessary, relative to the baud clock before the idle time is reached.

TABLE 41 J1708 BAUD RATE LSB REGISTER - SFR DBH

Bit	Mnemonic	Function
7-0	J17BDLO [7:0]	Used to set the J1708 baud rate.

TABLE 42 J1708 BAUD RATE MSB REGISTER- SFR DCH

Bit	Mnemonic	Function
7-0	J17BDHI [15:8]	Used to set the J1708 baud rate.

J17BDHI and JBDLO are concatenated to create the BAUD_RATE[15:0] register which counts the number of clock ticks before a baud pulse is generated.

TABLE 43 J1708 DATA REGISTER - SFR DDH

Bit	Mnemonic	Function
7-0	J17DATA [7:0]	This 8 bit register is used to read the incoming data from the J1708 bus. Data written to this register will be sent out over the J1708 bus.

TABLE 44 J1708 INTERRUPT ENABLE REGISTER - SFR DEH

Bit	Mnemonic	Function
7-4	Not Used	
3	J17TXERRIE	Setting this bit to 1 enables the transmit error interrupt to the processor.
2	J17TXEMPIE	Setting this bit to 1 enables the transmit buffer empty interrupt to the processor.
1	J17RXOVIE	Setting this bit to 1 enables the receiver overrun error interrupt to the processor.
0	J17RXDAIE	Setting this bit to 1 enables the receiver data available interrupt to the processor.

TABLE 45 J1708 INTERRUPT STATUS REGISTER - SFR DFH

Bit	Mnemonic	Function
7-6	Not Used	
5	J17BUSRDY	When read back as 1, this signal indicates that the J1708 bus is idle and the priority slot corresponding to the value of the Priority Register is ready for transmission of data.
4	J17BUSIDLE	When read back as 1, this signal indicates that the J1708 bus is idle and ready to receive the 1st field of a data-packet (MID).
3	J17TXERR	When read back as 1, this signal indicates a transmission error (bus collision) and data will need to be re-transmitted at the next available time slot..
2	J17TXEMP	When read back as 1, this signal indicates that the transmitter is ready to send another byte of data.
1	J17RXOVR	When read back as 1, this signal indicates that the receiver has overrun and that the data has been corrupted.
0	J17RXDA	When read back as 1, this signal indicates that there is data available in the receiver.

Please note that the internal transceiver has a common-mode rejection of between –2.5-+7.5V,

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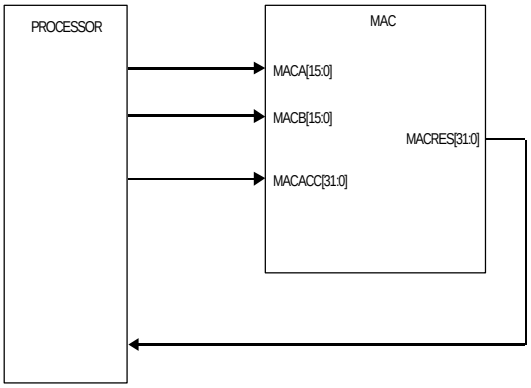
MAC

The VERSA1 includes a multiply-accumulator that can be used to significantly speed up arithmetic operations. This block allows the following calculation to be done:

(MACA * MACB) + MACACC = MACRESULT

Where MACA (multiplier), MACB (multiplicand), MACACC (accumulate) and MACRESULT (result) are 16, 16, 32 and 32 bits, respectively.

Figure 12: MAC Connection to the processor



Using the MAC

All arguments of the MAC block are all mapped into the SFR data space in byte-wise fashion, the processor must move each sub byte of each of the MACA, MACB and MACACC fields to the corresponding byte address. Once this is done, the processor can immediately read back the result in the byte fields of the MACRES.

Please note that the

- MACA, MACB and MACACC sets of registers are Write Only
- MACRESULT sets of registers are Read Only

The following tables describe the SFR interface to the MAC registers.

TABLE 46 MACA LSB REGISTER - SFR E6H

Bit	Mnemonic	Function
7-0	MACA0[7:0]	Lower 8 bits of the multiplier.

TABLE 47 MACA MSB REGISTER - SFR E7H

Bit	Mnemonic	Description
7-0	MACA1[15:8]	Upper 8 bits of the multiplier.

Note: MACA1 & MACA0 make up the full 16 bit MACA[15:0] argument.

TABLE 48 MACB LSB REGISTER - SFR EEH

Bit	Mnemonic	Function
7-0	MACB0[7:0]	Lower 8 bits of the multiplicand.

TABLE 49 MACB MSB REGISTER - SFR EFH

Bit	Mnemonic	Function
7-0	MACB1[15:8]	Upper 8 bits of the multiplicand.

Note: MACB1[7:0] & MACB0[7:0] make up the full 16 bit MACB[15:0] argument.

TABLE 50 MACACC LSB REGISTER - SFR C4H

Bit	Mnemonic	Function
7-0	MACACC0 [7:0]	Least Significant Byte of the accumulator argument.

TABLE 51 MACACC UPPER BYTE OF THE LSDW REGISTER - SFR C5H

Bit	Mnemonic	Function
7-0	MACACC1 [15:8]	Upper byte of the Least Significant Data Word of the accumulator argument.

TABLE 52 MACACC LOWER BYTE OF THE MSDW REGISTER - SFR C6H

Bit	Mnemonic	Function
7-0	MACACC2 [23:16]	Lower byte of the Most Significant Data Word of the accumulator argument.

TABLE 53 MACACC MSB REGISTER - SFR C7H

Bit	Mnemonic	Function
7-0	MACACC3 [31:24]	Most Significant Byte of the accumulator argument.

Note: MACACC3, MACACC2, MACACC1 & MACACC0 registers make up the full 32 bits of the MACACC[31:0] argument.

TABLE 54 MACRESULT LSB REGISTER - SFR EAH

Bit	Mnemonic	Function
7-0	MACRES0 [7:0]	Least Significant Byte of the result.

TABLE 55 MACRESULT UPPER BYTE OF THE LSDW REGISTER - SFR EBH

Bit	Mnemonic	Function
7-0	MACRES1 [15:8]	Upper byte of the Least Significant Data Word of the result.

TABLE 56 MACRESULT LOWER BYTE OF THE MSDW REGISTER - SFR ECH

Bit	Mnemonic	Function
7-0	MACRES2 [23:16]	Lower byte of the Most Significant Data Word of the result.

TABLE 57 MACRESULT_HI_HI REGISTER - SFR EFH

Bit	Mnemonic	Function
7-0	MACRES3 [31:24]	Most Significant Byte of the result.

Note: MACRES3, MACRES2, MACRES1 & MACRES0 make up the full 32 bits of the MACRES [31:0] argument.

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General Purpose I/O

There are 2 general purposes, digital I/Os on the VERSA1. These can be set as inputs or outputs via software control. The following describes the SFR interface to the I/O control block.

TABLE 58 I/O CONTROL REGISTER - SFR BAH

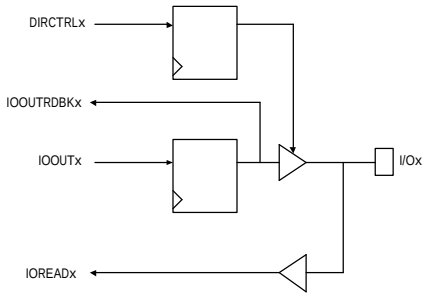
Bit	Mnemonic	Function
7-4	Not Used	
3	DIRCTRL1	When set to 1, this signal configures I/O1 as an output. If set to 0, it is configured as an input.
2	IOOUT1	When I/O1 is configured as an output, setting this bit to 1 will drive a logic high on the I/O1 pin. Setting this bit to a 0 will drive a logic 0 on the I/O1 pin.
1	DIRCTRL0	When set to 1, this signal configures I/O0 as an output. If set to 0, it is configured as an input.
0	IOOUT0	When I/O0 is configured as an output, setting this bit to 1 will drive a logic high on the I/O0 pin. Setting this bit to a 0 will drive a logic 0 on the I/O0 pin.

TABLE 59 I/O READ BACK REGISTER - SFR BBH

Bit	Mnemonic	Function
7-2	Not Used	
1	IOREAD1	This provides a read back of the logic level at pin I/O1
0	IOREAD0	This provides a read back of the logic level at pin I/O0

The following figure describes the general purposes I/O signals and their relationship with the I/O related registers.

FIGURE13 GENERAL PURPOSE I/O BLOCK DIAGRAM



I2C Bus

The I2C Bus on the VERSA1 is a slave based I2C Interface that has 2 specific functions:

- Program the on chip flash memory
- Act as a port where all on-chip peripherals (except MCU) can be accessed for tests or in cases where only the peripherals of the VERSA1 are needed.

Clock Control Circuitry

The VERSA1 clock control circuitry provides the ability to slow down or completely shut off the on-board clocks that drive all the digital logic. This is useful for applications that require low power operation. In addition to this, there is also a feature whereby if the clock have been turned off or slowed down and an interrupt occurs that is associated with specific on-board peripherals, then the clock will return to running at the full speed until the interrupt is cleared. The interrupts associated with this mechanism are:

- ADC
- SPI and J1708 interrupt (through intperiph_n)
- External INT0-
- External INT1-
- External INT2

The following describes the SFR interface to the clock control circuitry.

TABLE 60 CLOCK DIVIDER CONTROL REGISTER - SFR E5H

Bit	Mnemonic	Function
7-4	Not Used	
3-1	DIVCTL[2:0]*	This signal controls the digital logic clock speed.
0	NORMSPD	When set to 1, upon detection of an interrupt, the digital logic clock speed will return to the maximum until the associated interrupt is cleared.

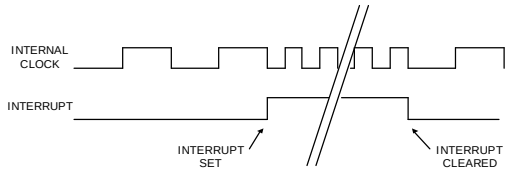
* The following table describes the relationship between the external clock frequency and the system clock that drives the internal processor and logic as controlled by DIVCTL[2:0].

TABLE 61 RESULTS OF DIVCTL SETTINGS

DIVCTL[2:0]	Internal Clock	System Clk for Ext Clock = 16MHz
000b	Ext Clock ÷ 2	8 MHz
001b	Ext Clock ÷ 4	4 MHz
010b	Ext Clock ÷ 8	2 MHz
011b	Ext Clock ÷ 16	1 MHz
100b	Ext Clock ÷ 32	500 kHz
101b	Ext Clock ÷ 64	250 kHz
110b	Ext Clock ÷ 128	125 kHz
111b	0MHz	0 Hz

The following figure describes the internal clock timing relationship when an interrupt occurs and is cleared when NORMSPD bit is set to 1..

Figure 14 Clock Timing When an Interrupt Occurs



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Interrupts

The VERSA1 is a highly integrated device incorporating a vast numbers of peripherals for which a comprehensive set of 10 interrupts sources ease systems program development. Nearly all actives peripherals in the VERSA1 are able to generate a specific interrupt that can provide a feedback to the MCU core that an event has occurred or a task is completed.

The following table summarize the interrupt sources, natural priority and associated interrupt vector

TABLE 62 INTERRUPT SOURCES, VECTORS AND NATURAL PRIORITIES.

IRQ	Description	Priority	Vector
intperiph_n	SPI and J1708 peripheral interrupt. Internal. Active low and configurable as edge-or level-sensitive. It is recommended that Intperiph_n interrupt be configured as level-sensitive, active low.	1	03h*
TF0	Timer 0 interrupt. Parts of VERSA1 MCU.	2	0Bh
INT1-	External interrupt 1, configurable as edge or level sensitive, active low.	3	13h
TF1	Timer 1 interrupt. Parts of VERSA1 MCU.	4	1Bh
TI_0 or RI_0	Serial Port 0 transmit or receive. Parts of VERSA1 MCU.	5	23h
TF2 or EXF2	Timer 2 interrupt. . Parts of VERSA1 MCU.	6	2Bh
TI_1 or RI_1	Serial Port 1 transmit or receive. Parts of VERSA1 MCU.	7	3Bh
intadc	A/D Converter interrupt	8	43h
INT0-	External interrupt 0, edge sensitive, active low	9	4Bh
INT2	External interrupt 2, edge sensitive, active high	10	63h

Figure 15 describes the VERSA1 interrupt system architecture. Note that SPI and J1708 interfaces share the Intperiph_n interrupt vector. The VERSA1 includes an interrupt priority encoder for these interrupts. Therefore upon activation of intperiph_n, the processor, in its interrupt service routine, can read from the Interrupt Source register (SFR E4h) in order to make a decision on which interrupt to deal with first.

Table 63 describes the SPI and J1708 interrupt source priority and the corresponding value read back from the Interrupt Source Register.

FIGURE 15 INTERRUPT CONNECTION DIAGRAM

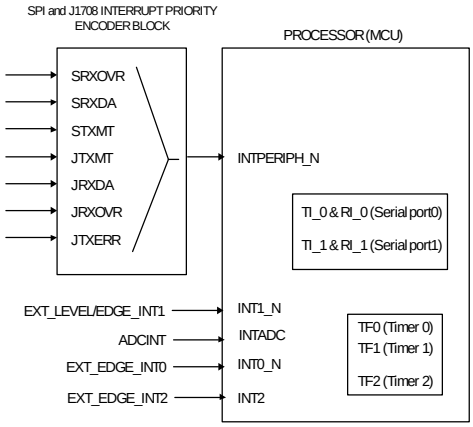

TABLE 63 PRIORITIES FOR INTPERIPH_N INTERRUPT AND INTERRUPT SOURCE REGISTER (SFR E4H) ASSOCIATED VALUE.

Interrupt Source	Priority	Value Read
SPI RX OVER RUN	1	01h
J1708 RX OVER RUN	2	02h
SPI TX EMPTY	3	03h
J1708 TX EMPTY	4	04h
SPI RX DATA AVAIL	5	05h
J1708 RX DATA AVAIL	6	06h
J1708 TX ERROR	7	07h
NO INTERRUPTS	-	00h

Reset

The VERSA1 provides two resets, *por_n* and RES-. *por_n* is the power-on reset which is generated internally by the Power-On-Reset/Brown-Out device. RES- provides the functionality of the standard 8051 RST input.

For either reset source, the VERSA1 remains in the reset state until the reset signal is removed. The internal RAM is not affected by either *por_n* or *RES-*. When the activated reset signal is removed, the VERSA1 exits the reset state and begins program execution at the standard reset vector address 0000h.

Power On Reset

The internal *por_n* input will be driven low for at least 10ms to ensure proper initialization.

Standard Reset

RES- provides the same functionality as the standard 8051 RST input, with inverse polarity. RES- must be asserted (active low) for at least 2 instruction cycles (8 system clk cycles). Shorter pulses on RES- might be ignored.

Package Information

The VERSA1 is available in the industry standard QFP-44 pins package.

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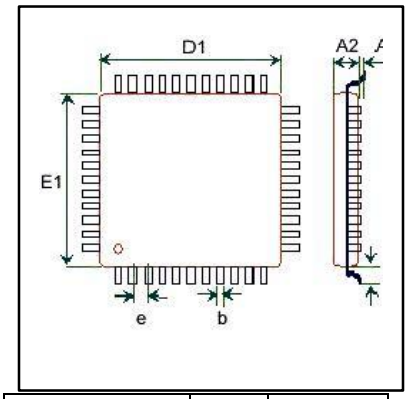
FIGURE 16 VERSA1 PACKAGE PARAMETERS



Stand-off	A1	0.17
Body thickness	A2	2.45 max
Lead length	L1	1.60
Lead width	b	0.35
Lead thickness	-	0.17
Lead pitch	e	0.8
Body size	D1	10
Body size	E1	10

Errata

The RS-485/J1708 block is currently not able to:

- Handle bus collisions correctly so the TXERRIE should be reset to '0' for proper device operation,
- Use the internal transceiver.
- Receive data correctly if it does not have 2 stop bits.

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