Product Specification

LVDS 28-bit Channel Link Receiver-85MHz

DESCRIPTION

The VX3321 receiver converts the four LVDS data streams back into 28 bits of CMOS/TTL data .

This chipset is the ideal solution to resolve EMI and cable size problems associated with high speed TTL interfaces.

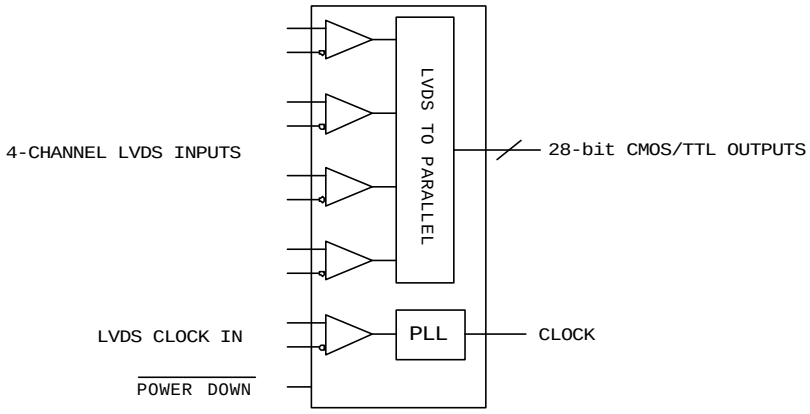
FEATURES

- Supply voltage 3.0~3.6V
- 20 to 85 MHz input clock support
- 50% duty cycle on receiver output clock
- Power-down mode < 198uW (max.)
- Narrow bus reduces cable size and cost
- +/- 1V common mode range (around + 1.2V)
- PLL requires no external components
- Rising edge data strobe
- TSSOP–56

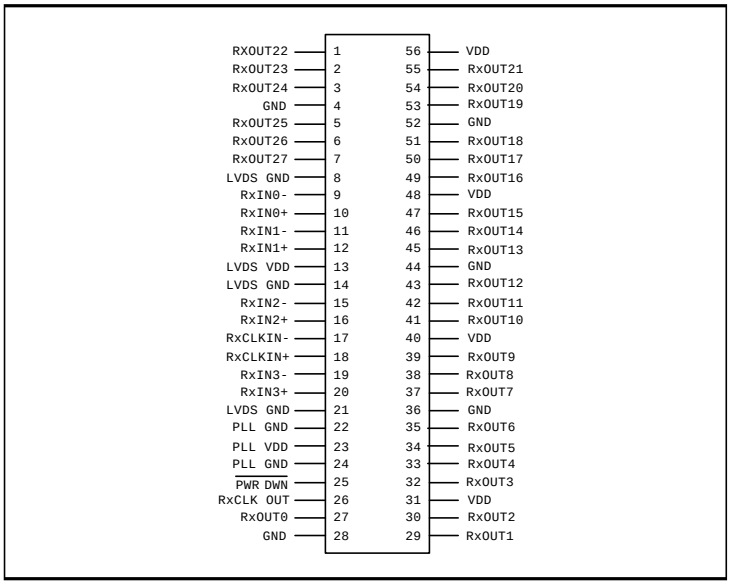
ABSOLUTE MAXIMUM RATINGS

■ Supply voltage	-0.3V to +4V
■ CMOS/TTL input voltage	-0.3V to (V_{DD}+0.3V)
■ CMOS/TTL output voltage	-0.3V to (V_{DD}+0.3V)
■ LVDS receiver input voltage	-0.3V to (V_{DD}+0.3V)
■ LVDS output short circuit duration	continuous
■ Junction temperature	+150° C
■ Storage temperature range	-65° C to +150° C
■ Lead temperature(Soldering 4sec)	+260° C

FUNCTION BLOCK DIAGRAM



PINS DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	Min	Nom	Max	Unit
Supply voltage(V_{DD})	3.0	3.3	3.6	V
Operating free air temperature(T_A)	-10	+25	+70	°C
Receiver input range	0		2.4	V

CMOS/TTL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage		2.0		V_{DD}	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	I_{OH}=-0.4mA	2.7	3.3		V
V_{OL}	Low level output voltage	I_{OL}=2mA		0.06	0.3	V
I_{IN}	Input current	V_{IN}=GND or V_{DD}		±5.1	±10	uA
I_{OS}	Short circuit output current	V_{OUT}=0V		-60	-120	mA

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TH}	Differential input high threshold	V_{OS}=+1.2V			+100	mV
V_{TL}	Differential input low threshold		-100			mV
I_{IN}	Input current	V_{IN}=+2.4V;V_{DD}=3.6V			±10	uA
		V_{IN}=0V;V_{DD}=3.6V			±10	uA
I_{DDRW}	Supply current worst case	C_L=8pF; Worst case pattern @85MHz (Fig.1, Fig.2)		96	135	mA
I_{DDRZ}	Supply current power down mode	$\overline{\text{PWRDWN}} = 0\text{V}$		10	55	uA

Note1:Typical values are given for V_{DD}=3.3V and T_A=+25°C

TIMING CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
CLHT	CMOS/TTL low to high transition time (Fig.2)			2	3.5	nS
CHLT	CMOS/TTL high to low transition time (Fig.2)			2	3.5	nS
$RSP_{OS}0$	Receiver input strobe position for bit0	85MHz (Fig.7)	0.54	0.84	1.14	nS
$RSP_{OS}1$	Receiver input strobe position for bit1		2.22	2.52	2.82	nS
$RSP_{OS}2$	Receiver input strobe position for bit2		3.9	4.2	4.5	nS
$RSP_{OS}3$	Receiver input strobe position for bit3		5.58	5.88	6.18	nS
$RSP_{OS}4$	Receiver input strobe position for bit4		7.26	7.56	7.86	nS
$RSP_{OS}5$	Receiver input strobe position for bit5		8.94	9.24	9.54	nS
$RSP_{OS}6$	Receiver input strobe position for bit6		10.62	10.92	11.22	nS
RCOP	RxCLK OUT period (Fig.3)		11.76	T	50	nS
RCOH	RxCLK OUT high time (Fig.3)	85MHz (Fig.7)	3.7	5	6.3	nS
RCOL	RxCLK OUT low time (Fig.3)		3.7	5	6.3	nS
RSKM	RxIN skew margin (note1) (Fig.8)		340			pS
RSRC	RxOUT setup to RxCLK OUT (Fig.3)		4			nS
RHRC	RxOUT hold to RxCLK OUT (Fig.3)		4			nS
RCCD	RxCLK IN to RxCLK OUT delay (note1) (Fig.6)		3.4	5	7.3	nS
RPLLS	Phase lock loop set (Fig.5)				10	mS
RPDD	Power down delay (Fig.4)				1	uS

Note1:The values are given for V_{DD}=3.3V and T_A=+25°C

TIMING DIAGRAMS

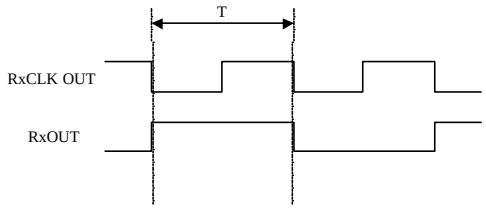


Figure 1. "Worst Case" Test Pattern

Figure 2. Receiver CMOS/TTL Output Load and Transition Times

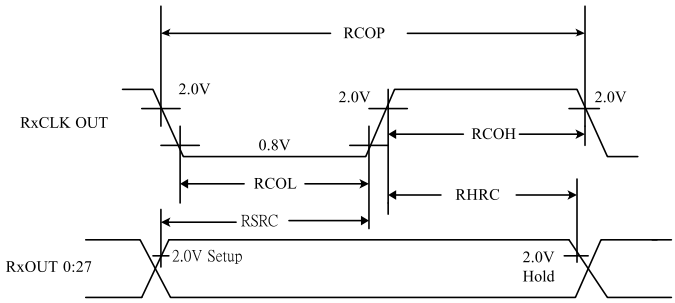


Figure 3. Receiver Setup/Hold and High/Low Times

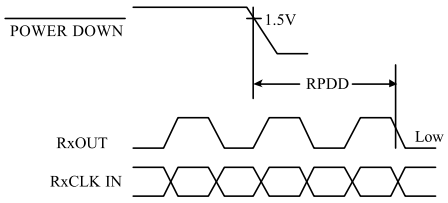


Figure 4. Rx Powerdown Delay

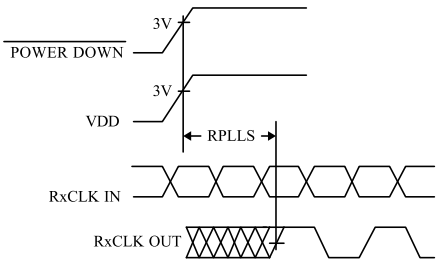


Figure 5. Rx PLL Set Time

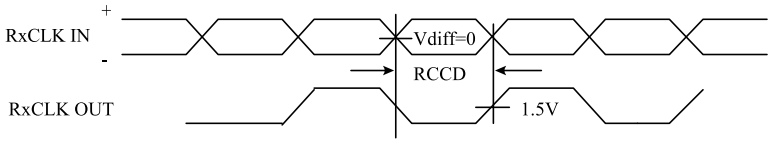


Figure 6. (Receiver) Clock IN to Clock Out Delay

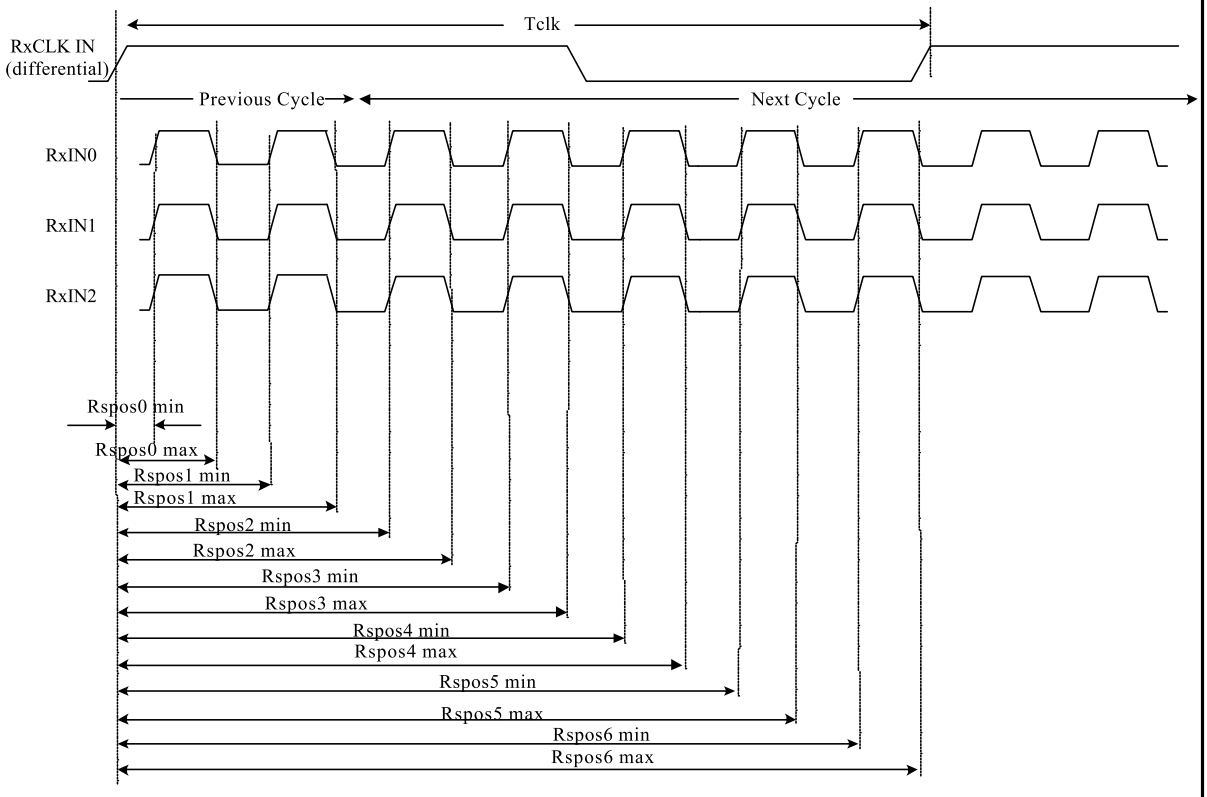


Figure 7. Receiver LVDS input Strobe Position

- C-Setup and Hold Time(Internal data Sampling Window) defined by Rspos (receiver input strobe position) min and max
- Tppos-Transmitter output pulse position (min and max)
- RSKM Cable Skew(type,length) +Source Clock Jitter (cycle to cycle)+ISI(inter-symbol interference)
- Cable skew-typically 10 ps-40 ps per foot, media dependent

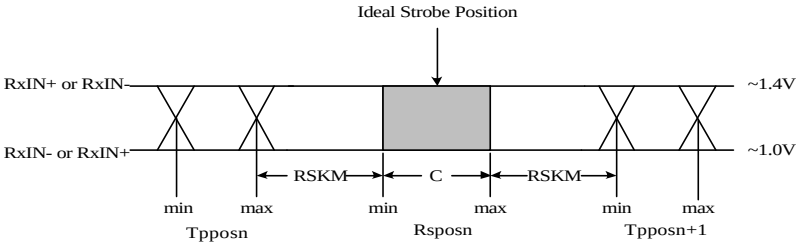
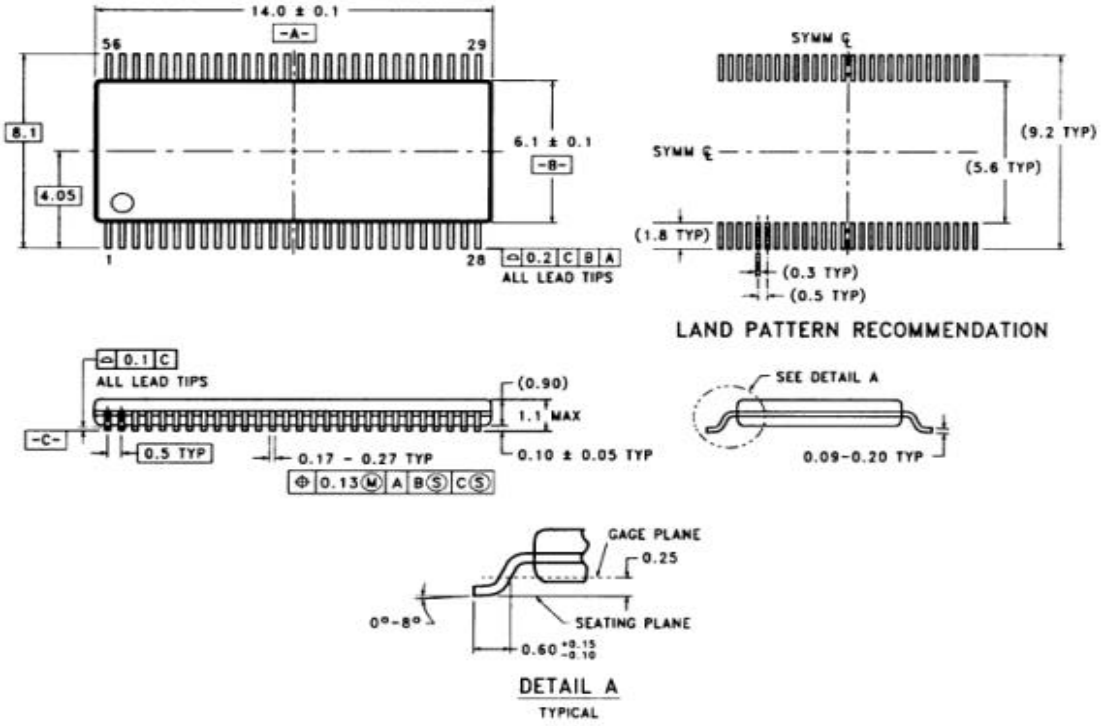


Figure8. Receiver LVDS Input Skew Margin

PIN DESCRIPTION

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock inputs.
RxCLK IN-	I	1	Negative LVDS differential clock inputs.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe.
PWRDWN	I	1	TTL level input. When asserted(low input)the receiver outputs are low.
Vdd	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL Vdd	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS Vdd	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Physical Dimensions inches (millimeters) unless otherwise noted



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