V23832-T1431-M1

Parallel Optical Link Transmitter: PAROLI® 2T Tx AC, 2.7 Gbit/s

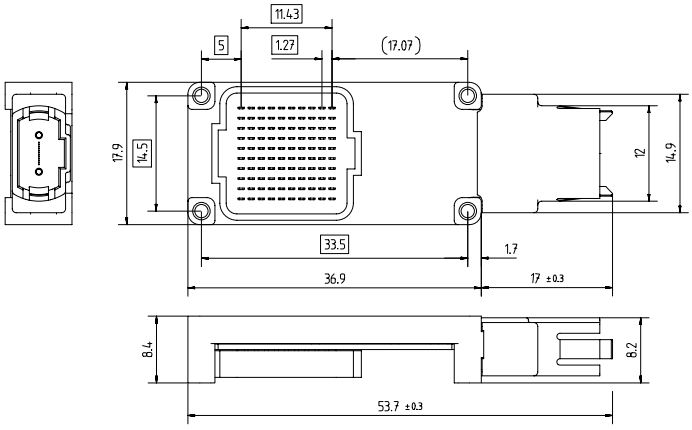
V23832-R411-M1

Parallel Optical Link Receiver: PAROLI® 2T Rx AC, 2.7 Gbit/s

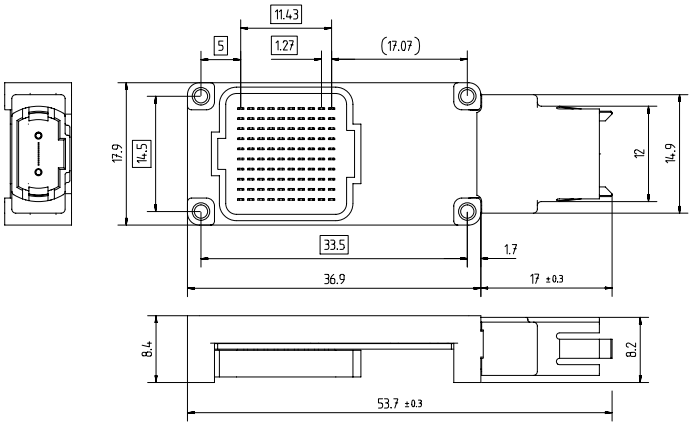
Preliminary

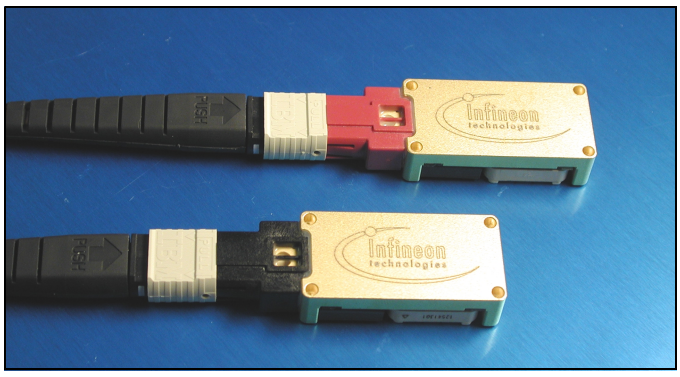
Dimensions in mm

PAROLI 2T Tx



PAROLI 2T Rx





FEATURES

- Power supply 3.3 V
- Transmitter with multistandard electrical interface
- Receiver with Infineons adjustable CML output
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Transmission data rate of up to 2700 Mbit/s per channel, total link data rate up to 32.4 Gbit/s
- 850 nm VCSEL array technology
- PIN diode array technology
- 62.5 µm graded index multimode fiber ribbon
- MT based optical port (MPO connector)
- Plug-in module
- IEC Class 1 laser safety compliant
- SONET mask compliant
- Optional EMI-shielding available

APPLICATIONS

Telecommunication

- Switching equipment
- Access network

Data Communication

- Interframe (rack-to-rack)
- Intraframe (board-to-board)
- On board (optical backplane)

Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Supply Voltage (V_{CC}–V_{EE}) ..... –0.3 V to 4.5 V
Data/Control Input Levels (V_{IN})(1) ..... –0.5 V to V_{CC}+0.5 V
Data Input Differential Voltage ($|V_{ID}|$)(2) ..... 2.0 V
Operating Case Temperature (T_{CASE})(3) ..... 0°C to 80°C
Storage Ambient Temperature (T_{STG}) ..... –20°C to 100°C
Operating Moisture ..... 20% to 85%
Storage Moisture ..... 20% to 85%
ESD Resistance (all pins to V_{EE}, human body model)(4) ..... 1 kV

Notes

1. At Data and LVCMOS inputs.
2. $|V_{ID}|$=|(input voltage of non-inverted input minus input voltage of inverted input)|.
3. Measured at case temperature reference point.
4. To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

DESCRIPTION

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module. The transmitter supports LVDS, CML and LVPECL differential signals. Two different receiver modules are available. Module V23832-R421-M1 is for LVDS electrical output only. This specification (V23832-R411-M1) describes a receiver for Infineons adjustable CML output.

Transmitter V23832-T1431-M1

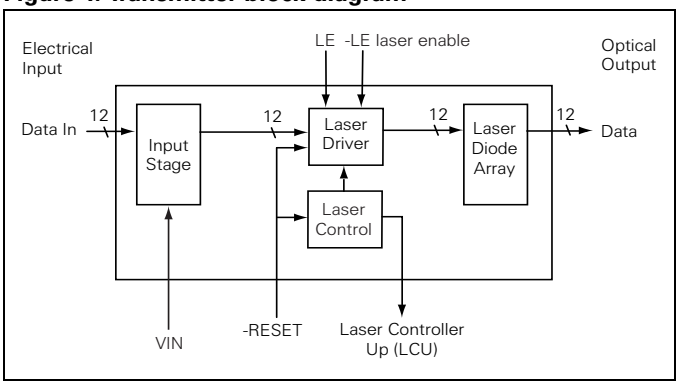
The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible; they also support LVPECL and CML because of the wide common input range). The electrical interface (LVDS, LVPECL or CML) is selected by the supply inputs V_{IN}. The data rate is up to 2700 Mbit/s for each channel. The transmitter module's min. data rate of 500 Mbit/s is specified for the CID(1) worst case pattern (disparity 72) or any pattern with a lower disparity.

A logic low level at –RESET switches all laser outputs off.
During power-up –RESET must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3.135 V level.
The Laser Controller Up (LCU) output is low if a laser fault is detected or –RESET is forced to low.
All non data signals have LVCMOS levels.
Transmission delay of the PAROLI system is ≤ 1 ns for the transmitter, ≤ 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Note

1. Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

Figure 1. Transmitter block diagram



LASER SAFETY

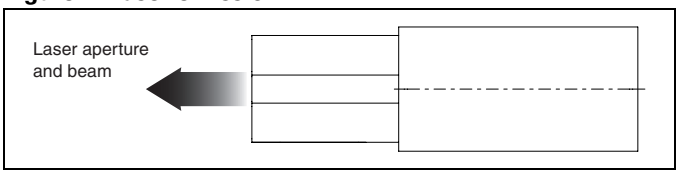
The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an IEC 60825-1 Amend. 2 Class 1 laser product. It complies with FDA performance standards (21 CFR 1040.10 and 1040.11) for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.
The PAROLI module must be operated under the specified operating conditions (supply voltage can be adjusted between 3.0 V and 3.6 V) under any circumstances to ensure laser safety.

Class 1 Laser Product

Note

Any modification of the module will be considered an act of "manufacturing", and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

Figure 2. Laser emission



Laser safety design considerations

To ensure laser safety for all input data patterns each channel is controlled internally and will be switched off if the laser safety limits are exceeded.
A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57%. The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.
The minimum alerter response time is 1 µs with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1 µs, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.
All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Recommended Operating Conditions

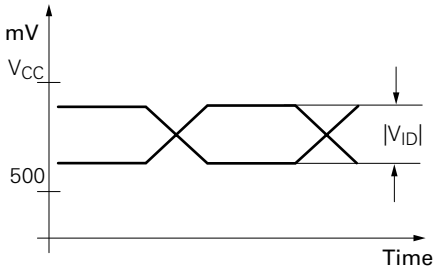
Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	3.135	3.6	V
Noise on Power Supply(1)	N_{PS1}		50	mV
Noise on Power Supply(2)	N_{PS2}		100	
Data Input Voltage Range(3,4)	V_{DATAI}	500	V_{CC}	
Data Input Differential Voltage(4,5)	$\|V_{ID}\|$	80	1000	
Data Input Skew(6)	t_{SPN}		0.5 x t_R, t_F	ps
Data Input Rise/Fall Time(7)	t_R, t_F	50	300	
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time(8)	t_R, t_F		20	ns

Notes

Voltages refer to V_{EE}=0 V.

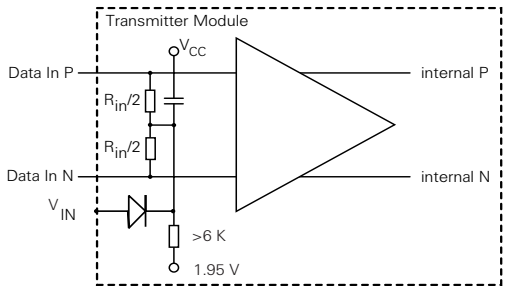
1. Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.
2. Noise frequency is > 10 MHz. Voltage is peak-to-peak value.
3. This implies that the input stage can be AC coupled.
4. Level diagram:

Figure 3. Input level diagram



5. $|V_{ID}|$=|(input voltage of non-inverted input minus input voltage of inverted input)|.
6. Skew between positive and negative inputs measured at 50% level.
7. 20%–80% level.
8. Measured between 0.8 V and 2.0 V.

Figure 4. Input stage



Transmitter Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		350	450	mA
Power Consumption	P		1.2	1.6	W
Data Rate per Channel	DR	500(1)		2700	Mbit/s
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			0.4	V
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2.5			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output Current High(2)	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low(3)	$I_{LVCMOSOL}$			4.0	
Data Differential Input Impedance(4)	R_{IN}	80		120	Ω
Data Input Differential Current	$\|I_I\|$			5.5	mA

Notes

1. Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
2. Source current.
3. Sink current.
4. Data input stage.

Transmitter Electro-Optical Characteristics

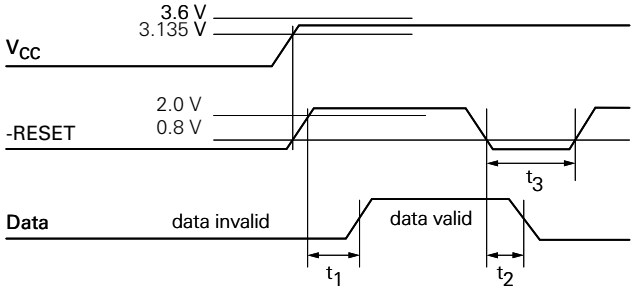
Parameter	Symbol	Min.	Typ.	Max.	Units
Optical Rise Time(1)	t_R			150	ps
Optical Fall Time(1)	t_F				
Total Jitter(2)	J_T			0.35	UI
Deterministic Jitter	J_D			0.15	
Channel-to-channel skew(3)	t_{CSK}			100	ps
Launched Average Power	P_{AVG}	–9.0	–5.0	–3.0	dBm
Launched Power Shutdown	P_{SD}			–30.0	
Center Wavelength	λ_C	830		860	nm
Spectral Width (FWHM)	$\Delta\lambda$			2	
Spectral Width (rms)	$\Delta\lambda$			0.85	
Relative Intensity Noise	RIN			–117	dB/Hz
Extinction Ratio (dynamic)	ER	6.0			dB
Optical Modulation Amplitude (OMA)(4)	OMA	0.15(5)	0.46(6)		mW
Eye mask compliance		SONET(7)			

Notes

Optical parameters valid for each channel.

1. 20%–80% level, non filtered values.
2. Measured using a filter (f_r=1.875 GHz) as defined in IEEE 802.3 (2000-edition) Gigabit Ethernet specification, section 38.6.5.
3. With input channel-to-channel skew 0 ps and a maximum data channel-to-channel average deviation and swing deviation of 5%.
4. Peak to peak values.
5. Corresponds to a minimum extinction ratio of 6 dB.
6. Corresponds to a typical extinction ratio of 8 dB.
7. Telcordia GR-253-CORE, Issue 3, Sept. 2000, sec. 4.2.4.4.

Figure 5. Timing diagram



Parameter	Symbol	Min.	Max.	Units
–RESET on Delay Time	t_1		100	ms
–RESET off Delay Time	t_2		50	µs
–RESET Low Duration(1)	t_3	10		

Note

1. Only when not used as power on reset. At any failure recovery, –RESET must be brought to low level for at least t_3.

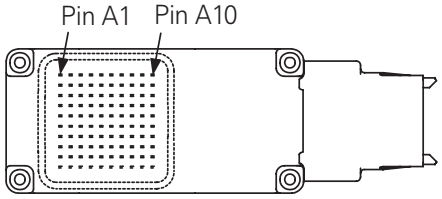
Numbering Conventions Transmitter (bottom view)

TX
Customer Board Side

	J	I	H	G	F	E	D	C	B	A
1	VEE	DI05N	DI05P	DI06N	DI06P	DI07N	DI07P	DI08N	DI08P	VEE
2	DI04P	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	DI09N
3	DI04N	VEE	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	VEE	DI09P
4	DI01P	VEE	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	VEE	DI012N
5	DI01N	VEE	VEE	VEE	t.b.l.o.	t.b.l.o.	VEE	VEE	VEE	DI012P
6	DI02P	VEE	VEE	VEE	t.b.l.o.	-LE	VEE	VEE	VEE	DI011N
7	DI02N	VEE	VEE	VEE	LCU	LE	VEE	VEE	VEE	DI011P
8	DI03P	VEE	VEE	VEE	VIN	-RESET	VEE	VEE	VEE	DI010N
9	DI03N	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VEE	DI010P
10	VEE	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VEE	VEE

Fiber Side

Pin Information



Pin Description

Pin Name	Level/Logic	Description
V_{CC}		Power supply voltage of laser driver
V_{IN}		CML: V_{IN}=Reference supply (e.g. V_{CC}) LVDS: V_{IN}=V_{EE}
V_{EE}		Ground
LCU	LVCMOS Out	Laser Controller Up. High=normal operation Low=laser fault or RESETlow.

Pin Name	Level/Logic	Description
DI0xN	Signal In	Data Input #x, inverted
DI0xP	Signal In	Data Input #x, non-inverted
–RESET	LVCMOS In	High=laser diode array is active. Low=switches laser diode array off. This input has an internal pull-down to ensure laser safety switch off in case of unconnected RESETinput.
LE		Laser ENABLE. High active. High=laser array is on if LE is also active. Low=laser array is off. This input has an internal pull-up, therefore can be left open.
–LE		Laser ENABLE. Low active. Low=laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.

DESCRIPTION

Receiver V23832-R411-M1

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, trans impedance amplifiers, and gain amplifiers. The differential data outputs are Infineons adjustable CML signals. A separate module (V23832-R421-M1) with LVDS output is also available. The output differential voltage (swing) is adjusted by an external resistor connected to the REFR module input, the output average is adjustable by external pull-up resistors.
The data rate is up to 2700 Mbit/s for each channel. The receiver module's min. data rate of 500 Mbit/s is specified for the CID(1) worst case pattern (disparity 72) or any pattern with a lower disparity.

Additional Signal Detect outputs (SD1 active high / –SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.
A logic low at Output Enable sets all data outputs to logic low. SD outputs will not be effected.
All non data signals have LVCMOS levels. Transmission delay of the PAROLI system is ≤ 1 ns for the transmitter, ≤ 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Note

1. Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

Figure 6. Receiver block diagram

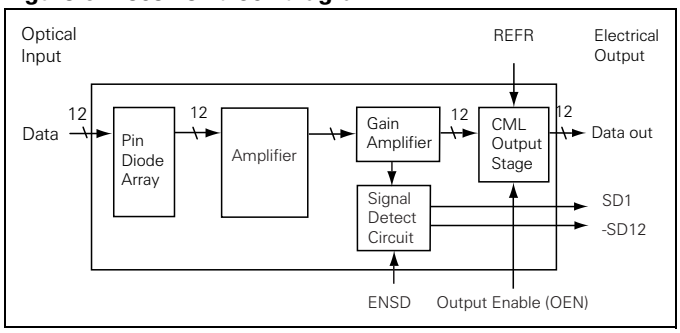
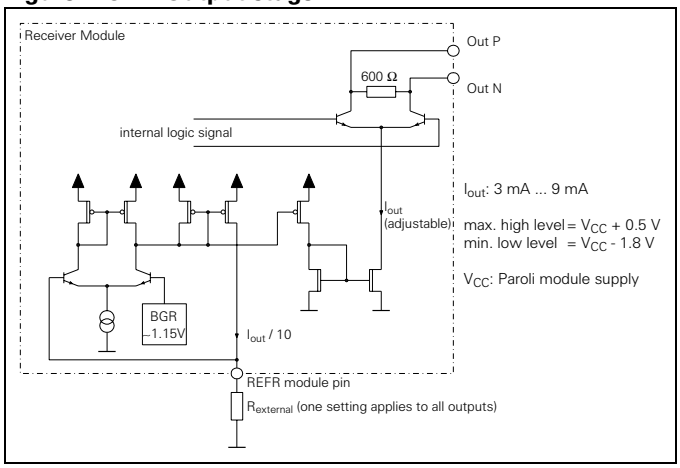


Figure 7. CML Output stage



TECHNICAL DATA

Recommended Operating Conditions

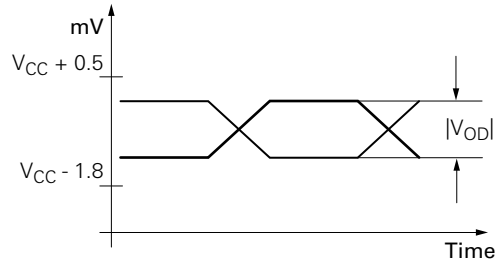
Parameter	Symbol	Min.	Max.	Units
Power Supply Voltages	V_{CC}, V_{CCO}	3.0	3.6	V
Noise on Power Supply(1)	N_{PS1}		50	mV
Noise on Power Supply(2)	N_{PS2}		100	
Output Current(3)	I_{out}	3	9	mA
Output Voltage(4)	V_{out}	V_{CC} –1.8	V_{CC} +0.5	V
Output Differential Voltage(4,5)	$\|V_{OD}\|$	80	800	mV
Output Load RC Time Constant	t_{RC}		100	ps
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time(6)	t_R, t_F		20	ns
Optical Input Rise/Fall Time(7)	t_R, t_F		185	ps
Input Extinction Ratio	ER	6.0		dB
Input Center Wavelength	λ_C	830	860	nm

Notes

Voltages refer to V_{EE}=0 V.

1. Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.
2. Noise frequency > 10 MHz. Voltage is peak-to-peak value.
3. $I_{out} \approx 10 * 1.15\ V / R_{external}$. Resistor $R_{external}$ to be connected externally between REFR and V_{EE}.
4. Level diagram:

Figure 8. Output level diagram



5. $|V_{OD}| = I_{out} * (300\ \Omega \parallel R_{LOAD})$. The output current range of 3 mA to 9 mA corresponds to $|V_{OD}|$=130 mV to 385 mV for R_{LOAD}=50 Ω. $|V_{OD}|$=|(output voltage of non-inverted output minus output voltage of inverted output)|.
6. Measured between 0.8 V and 2.0 V.
7. 20%–80% level. Non filtered values.

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		130+ 18 I_{out}	200+ 24 I_{out}	mA
Power Consumption(1)	P		0.6	1.0	W
Data Output Rise/Fall Time(2)	t_R, t_F			250	ps
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2500			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output(3) Current High	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output(4) Current Low	$I_{LVCMOSOL}$			4.0	
Total Jitter(5,6)	J_R			0.39	UI
Deterministic Jitter(5)	J_D			0.15	
Channel-to-channel skew(7)	t_{CSK}			100	ps

Notes

1. Calculated for I_{out}=3 mA.
2. Measured between 20% and 80% level.
3. Source current.
4. Sink current.
5. With no optical input jitter.
6. At sensitivity limit of 0.05 mW OMA.
7. With input channel-to-channel skew 0 ps.

Receiver Electro-Optical Characteristics

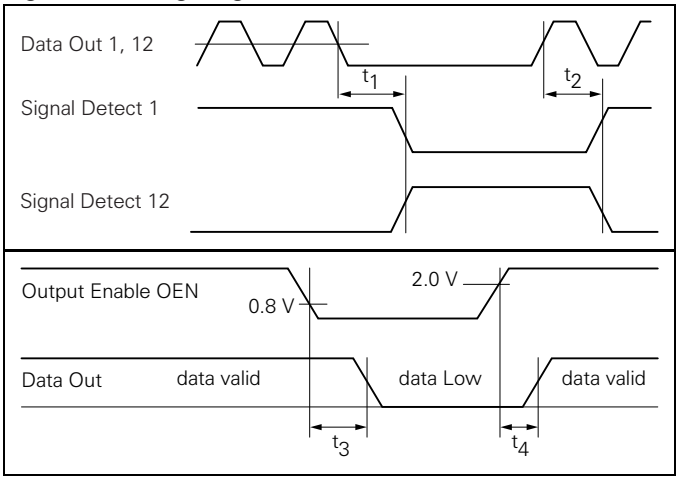
Parameter	Symbol	Min.	Max.	Units
Data Rate Per Channel	DR	500(1)	2700	Mbit/s
Sensitivity (Average Power)(2)	P_{IN}		–16.0	dBm
Optical Modulation Amplitude (OMA)(3)	OMA	0.05(4)		mW
Saturation (Average Power)	P_{SAT}	–3.0		dBm
Signal Detect Assert Level(5)	P_{SDA}		–17.0	
Signal Detect Deassert Level(5)	P_{SDD}	–29.0		
Signal Detect Hysteresis(5)	P_{SDA}– P_{SDD}	1.0	4.0	dB
Return Loss of Receiver	A_{RL}	12		

Notes

Optical parameters valid for each channel.

1. Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
2. BER=10^{-12}, Extinction ratio=infinite, Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
3. Peak to peak value.
4. Corresponds to an maximum sensitivity (average power) of –16.0 dBm at an infinite extinction ratio.
5. Extinction ratio=infinite,
   P_{SDA}: Average optical power when SD switches from inactive to active.
   P_{SDD}: Average optical power when SD switches from active to inactive.

Figure 9. Timing diagrams



Parameter	Symbol	Max.	Units
Signal Detect Deassert Time	t_1	10	µs
Signal Detect Assert Time	t_2		
Output Enable off Delay Time	t_3	20	ns
Output Enable on Delay Time	t_4		

Figure 10. Interfacing to CML

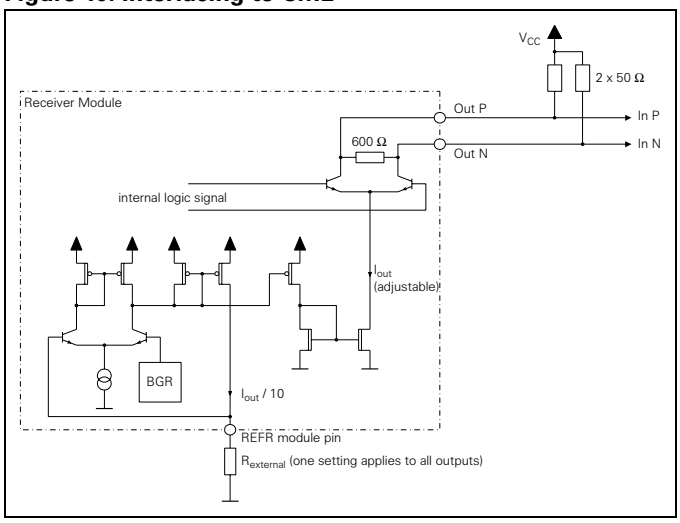
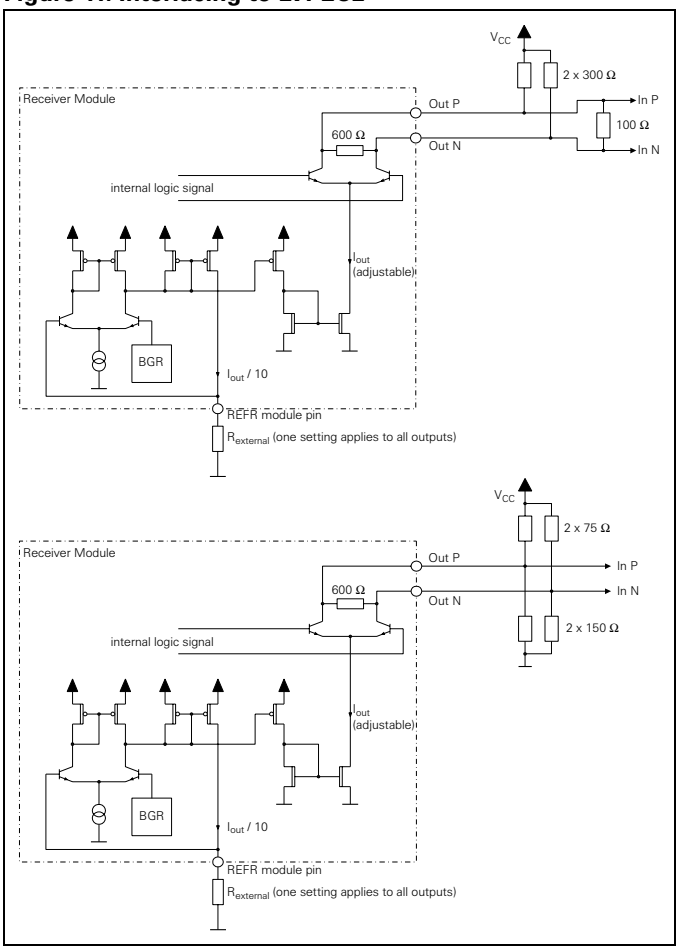


Figure 11. Interfacing to LVPECL



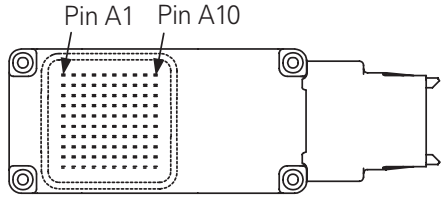
Numbering Conventions Receiver (bottom view)

RX
Customer Board Side

	J	I	H	G	F	E	D	C	B	A
1	VEE	DO05P	DO05N	DO06P	DO06N	DO07P	DO07N	DO08P	DO08N	VEE
2	DO04N	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	DO09P
3	DO04P	VEE	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	VEE	DO09N
4	DO01N	VEE	Reserved	Reserved	OEN	ENSD	Reserved	Reserved	VEE	DO012P
5	DO01P	VEE	VEE	VEE	SD01	-SD12	VEE	VEE	VEE	DO012N
6	DO02N	VEE	VEE	VEE	Reserved	REFR	VEE	VEE	VEE	DO011P
7	DO02P	VEE	VEE	VEE	VCCO	VCCO	VEE	VEE	VEE	DO011N
8	DO03N	VEE	VEE	VEE	VCCO	VCCO	VEE	VEE	VEE	DO010P
9	DO03P	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VEE	DO010N
10	VEE	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VEE	VEE

Fiber Side

Pin Information



Pin Description

Pin Name	Level/Logic	Description
V_{CC}		Power supply voltage of pre amplifier and analog circuitry
V_{CCO}		Power supply voltage of output stages
REFR		Adjustment of output current by connecting external resistor to V_{EE}
V_{EE}		Ground
OEN	LVCMOS In	Output Enable High=normal operation. Low=sets all Data Outputs to low. This input has an internal pull-up which pulls to high level when this input is left open.
ENSD		High=SD1 and –SD12 function enabled. Low=SD1 and –SD12 are set to permanent active. This input has an internal pull-up which pulls to high level when this input is left open.
SD1	LVCMOS Out	Signal Detect on fiber #1. High=signal of sufficient AC power is present on fiber #1. Low=signal on fiber #1 is insufficient.
–SD12	LVCMOS Out low active	Signal Detect on fiber #12. Low=signal of sufficient AC power is present on fiber #12. High=signal on fiber #12 is insufficient.
DO0xP	LVDS Out	Data Output #x, non-inverted
DO0xN		Data Output #x, inverted

Optical Port

- Designed for the 12 fiber MT Connector (MPO)
- Alignment pins fixed in module port
- Integrated mechanical keying

Features of the MT Connector (MPO)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Push-pull mechanism
- Ferrule bearing spring loaded

Features of the PAROLI 2T electrical connector(1)

- Module side: FCI-MEG-Array® -Plug (part no. 84512-202)
- PCB side: FCI MEG-Array® -Receptacle (part no. 84513-201)
- 100 pin positions
- Pluggable version using BGA socket
- 4 mm stack height in mated conditions
- Plug and receptacle are provided with pick-up cap
- Standard BGA process for socket assembly
- Contact area plating made from gold over nickel

Note

1. The PAROLI 2T module needs to be screwed to the customer board by using the provided holes in the module frame (see page 1) in order to provide long term reliability.

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Information

For further information on technology, delivery terms and conditions and prices please contact the Infineon Technologies offices or our Infineon Technologies Representatives worldwide - see our webpage at
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