MITEL
SEMICONDUCTOR

# VP7615

## Colour Digital Video Camera Decoder IC

Advance Information

Supersedes February 1997 edition, DS4602 - 2.4

DS4602 - 3.1 August 1997

The VP7615 iCamHost™ Processor chip can decode the signals from a variety of iVision™ compatible digital video cameras (such as Silicon Vision's iCam™) and process them for use in a host computer system. Digital cameras can offer real cost and performance gains in applications which require a digital video input, and iVision technology realises both these benefits. In a typical analog camera the digitised output from the CCD imager is normally encoded into an analog composite video signal which then has to be re-digitised at the input to the host system. By employing the iVision approach the output from the camera is maintained as a digital signal, but in a format which allows for a low cost 9-wire connection to the host. Eliminating the unnecessary conversion to an analog signal and back again not only saves cost, but also avoids any possible degradation of image quality. Other benefits include direct control of the camera from the host and the ability to power the camera from the host system so saving the cost of a separate power supply.

The VP7615 supports two software selectable CamPort™ interface ports, either of which can receive the digital video from an iVision™ compatible digital video camera. The output is a standard colour digital video signal, similar to standard composite analog-digital decoder chips such as the Philips SAA7110 and SAA7111. All iCamHost™ operating modes are controlled by the host PC via an $I^2C$ interface. Hardware I/O controls include output enable and $I^2C$ address offset.

NOTE: iCam™, CamPort™ and iCamHost™ are trademarks of Silicon Vision, Inc., Fremont, CA

### ORDERING INFORMATION

VP7615 CG FP1N

### FEATURES

- Accommodates different camera configurations based on a variety of CCD imager resolutions
- Requires only a small, low-cost 9 pin mini-DIN to connect to camera
- Receives the image signal from the camera in digital form at a frame rate determined by the host
- Decodes all necessary synchronisation and clock signals from the digital data stream
- Programmable gamma correction curve in RGB colourspace
- Programmable colour-separation matrix
- Collects image status data within user-defined rectangular gated zone of CCD sensor
- Programmable horizontal and vertical aperture correction
- Pin-strap selectable output format in 16 bit YUV 4:2:2 or 8 bit CCIR 656 YUV 4:2:2
- Test pattern generator for SMPTE colourbars
- Bypass mode to output unprocessed 8 bit CCD pixel samples in the luminance channel
- Dual iCamPort™ camera input ports, software selectable
- Completely iVision™ Compatible
- Eight general purpose I/O pins for board level configuration control and/or status
- Programmable polarity for HSYNC, VSYNC, HACT & VACT control outputs
- Chip pinout is backwards compatible with VP7610

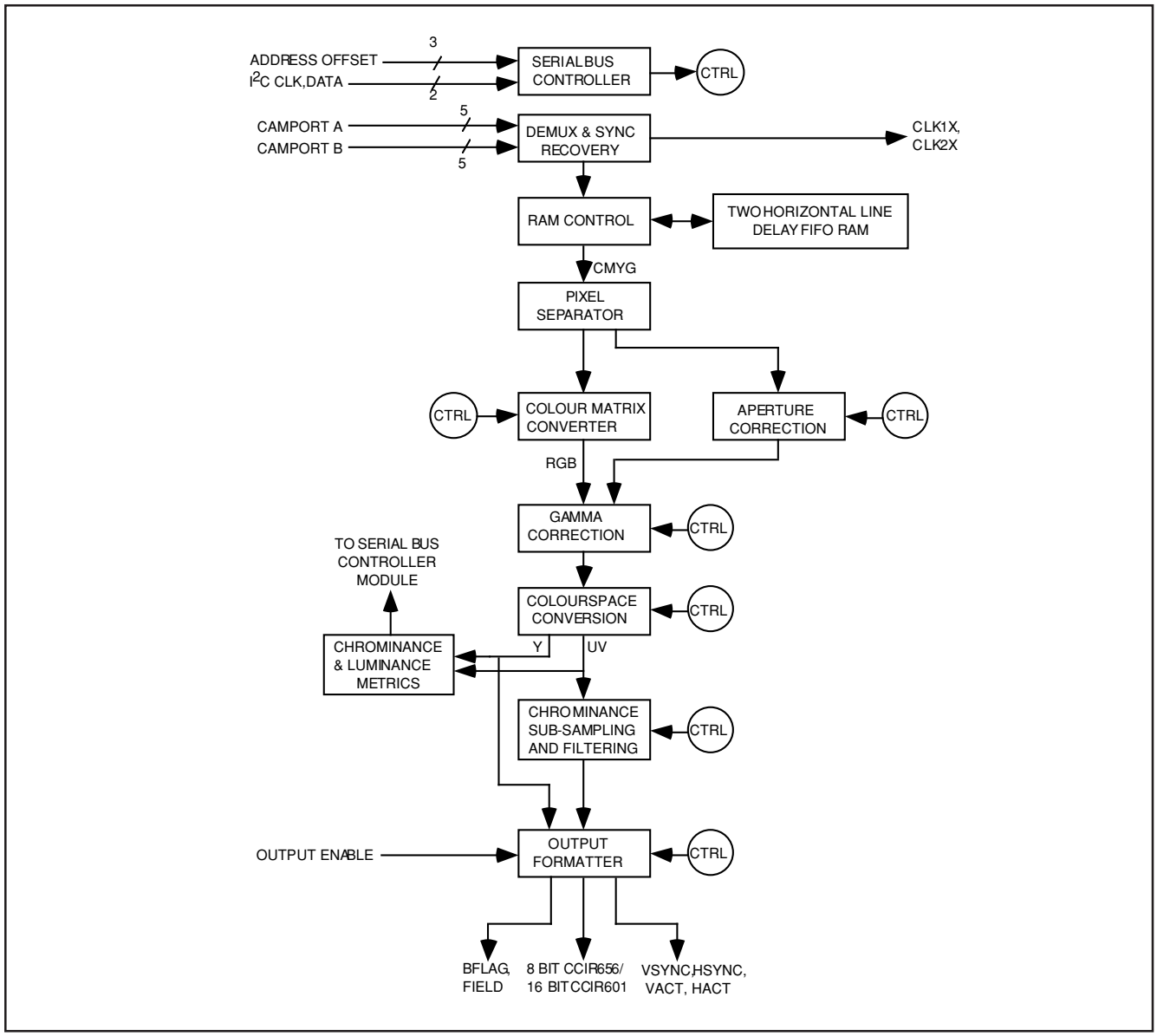



*Fig.1 Functional Block Diagram*

## THEORY OF OPERATION

**General Overview**
The VP7615 iCamHost™ is a fully synchronous real-time pipeline pixel processor for converting digitized CCD photosite samples into co-sited, colour calibrated, gamma corrected and aperture corrected digital video in an industry-conventional format similar to analog video decoders. The VP7615 supports the full iVision™ Command Set for control of camera head functions such as frame rate, resolution, exposure and colour depth via the CamPort™ Interface. Access to all registers and functions is provided by an $I^2C$ state machine.

**Demux and sync recovery**
The incoming CCD photosite bytes come in a single nibble at a time in a "big-endian" fashion from one of two CamPort™s. These nibbles are clocked in via a separate pixel clock signal. The formatting signals such as start of active video, end of active video, and start of new frame are all encoded into the nibble stream. The output is an 8 bit byte of CCD sample for each pixel clock, as well as separate horizontal and vertical sync signals.

**RAM control & 2H line delay FIFO RAM**
Since the iCamHost™ assumes an interlaced scanning CCD with a CMYG colour mosaic format, the colour content is derived from different locations around where the output video pixel is desired. Specifically, the first line from the CCD contains "red-like" colour content, alternating with the following line containing "blue-like" colour content. The third line is real-time, and the first opportunity to output properly co-sited luminance and chrominance as though the colour pixels were superimposed upon themselves, all on the second line.

**Pixel separator**
Since the colourspace converter requires the 3 most recent lines of CCD data, this block handles the shuffling of either the 2 red and 1 blue line, or 2 blue and 1 red line of data.

**Colour matrix converter**
The input to this converter is derived from the relative sums and differences of the above 3 lines of sample data, and processes them through a programmable 3x3 matrix multiplier. The output is colour-separated and calibrated RGB samples.

**Gamma corrector**
Since CRT monitors have a non-linear RGB intensity response to input signal, gamma correction must be performed in RGB space as well to prevent cross-coupling errors between luminance and chrominance. This block is a programmable 16 line-segment curve generator to provide not only gamma correction, but any arbitrary contiguous curve of positive slope, with end points at any level to adjust contrast and range.

**Colourspace converter**
Since the output of the processor is to be YUV and not RGB, a fixed-coefficient 3x3 matrix converter is used.

**Chrominance sub-sampling & filtering**
Spatial sub-sampling and filtering is performed since the output sampling format must be reduced from 4:4:4 to 4:2:2 because most video systems do not require more chrominance data for video camera input.

**Output formatter**
Devices taking digital video input such as capture, graphics and compression chips usually require the YUV to be formatted either in CCIR601 16 bit mode (YU then YV) or CCIR656 8 bit mode(U then Y then V then Y). The output mode (8 vs 16 bit) CCIR601 is pin-strap selectable. Additional control register bits may be used to swap the luma and chroma data or to swap the order of U and V data to support the video input requirements of a variety of bus master or graphics chip video interfaces without external glue logic. The polarity of VSYNC, HSYNC, VACT and HACT is also programmable. An output enable input signal may be used when "bussing" the output with other video decoders. Other useful signals such as field and colour flags are also provided. Timing diagrams illustrating the function of the video outputs at different time scales are given in figures 5 to 8.

**Aperture corrector**
Since both the luminance and chrominance are derived from spatially spread pixels and the ideal output would be as though all the pixels were superimposed upon one another, a programmable vertical and horizontal aperture correction can be applied to either "soften" or "sharpen" the image.

**Scene-sensing luminance and chrominance metrics**
There are no hard-wired closed-loop control circuits in the processor. To achieve great flexibility in control over the behavior of the camera head and processor system, a user-defined region of interest is programmed which provides statistical information about the field of video only within that region. Peak luminance, total luminance, total red chrominance and total blue chrominance are provided and updated after each field.

**Serial bus control**
To provide read-write control over the registers within the processor, a standard $I^2C$ state-machine is provided. Its address may be offset by 3 bits to preclude address conflicts.

## PERFORMANCE

| PARAMETER | MAXIMUM VALUE OR SPECIFICATION |
|---|---|
| CCD Resolution | Up to 768 pixels per line |
| Field Rate | Up to 60 fields per second |
| Video Sample Rate | 30 MHz. max. input clock rate, 15MHz. max. output clock rate |
| Video Sample Quantisation | 8 bit samples in 2 nibbles of 4 bits each |
| Control Signals | Standard $I^2C$ protocol |
| Configuration Inputs | $I^2C$ address offset, output enable |
| Gamma Correction | Programmable via 16 arbitrary connected line segments |
| Output Format | CCIR601 compliant 4:2:2 digital video, pixels per line=CCD pixels |
| Output Colourspace | YCrCb luminance & chrominance |
| Output Signals | 16 bit digital video, H & V sync, 1X & 2X clock, field ID, chroma ID |
| Power Consumption | 950mW |

## STATUS REGISTERS

| FUNCTION | SIZE | DESCRIPTION |
|---|---|---|
| Gated Luminance Sum | 32 bits | Sum of luminance values within gated zone |
| Gated Luminance Peak | 8 bits | Value of peak luminance pixel(s) within gated zone |
| Gate Red Chrominance Sum | 32 bits | Sum of red chrominance values within gated zone |
| Gated Blue Chrominance Sum | 32 bits | Sum of blue chrominance values within gated zone |

## CONTROL REGISTERS

| FUNCTION | SIZE | DESCRIPTION |
|---|---|---|
| Colour Calibration Matrix | 78 bit | 9x9 bit signed coefficients converting CMYG to RGB |
| Gating Zone Start Pixel | 16 bits | 8 bits for column # and for row #, in 4 pixel increments |
| Gating Zone End Pixel | 16 bits | 8 bits for column # and for row #, in 4 pixel increments |
| Gamma Correction | 128 bit | Locus of 16 points of 8 bits each forms many curves |
| Horiz. Aperture Correction | 4 bits | 00H = 0%, 40H = +100%, 70H = +175%, F0H= -175% |
| Vert. Aperture Correction | 4 bits | 00H = 0%, 40H = + 50%, 70H = + 87%, F0H= - 87% |
| Processor bypass | 2 bits | 0=normal, 1=pass raw 8 bit samples to Y output pins |
| CamPort™ select | 1 bit | 0=port A, 1=port B |
| Test pattern generator | 1 bits | 0=live video, 1=colourbars |

## SIGNALS & PINOUT

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 60 | In* | CPCKA | Clock - This input receives the clock from the CamPort™ camera on port A. |
| 54 | In* | CPDA3 | CamPort™ Data Bit 3 - This bus receives the data from the CamPort™ camera on port A. |
| 55 | In* | CPDA2 | CamPort™ Data Bit 2 - Port A |
| 56 | In* | CPDA1 | CamPort™ Data Bit 1 - Port A |
| 59 | In* | CPDA0 | CamPort™ Data Bit 0 - Port A |
| 88 | In* | CPCKB | CamPort™ B Clock - This input receives the clock from the CamPort™ camera on port B. |
| 84 | In* | CPDB3 | CamPort™ B Data Bit 3 - This bus receives the data from the CamPort™ camera on port B. |
| 85 | In* | CPDB2 | CamPort™ B Data Bit 2 |
| 86 | In* | CPDB1 | CamPort™ B Data Bit 1 |
| 87 | In* | CPDB0 | CamPort™ B Data Bit 0 |
| 91 | Out | CPSEL | CamPort™ Select Status - When this output is low, the data from CamPort™ A is being used, when this output is high, the data from CamPort™ B is being used. This pin is controlled by Bit 3 of the Configuration Register (sub-address = 0x00). |
| 44 | In | RSTN | Reset Not - When this Schmidtt trigger input is low, the chip is placed into a known state. When this input is high, the chip can operate. |
| 11 | Out | YY7 | Luminance Out bit 7 - When CCSEL is low this bus carries the luminance data. When CCSEL is high this bus carries multiplexed luminance and chrominance data |
| 10 | Out | YY6 | Luminance Out bit 6 |
| 9 | Out | YY5 | Luminance Out bit 5 |
| 6 | Out | YY4 | Luminance Out bit 4 |
| 5 | Out | YY3 | Luminance Out bit 3 |
| 4 | Out | YY2 | Luminance Out bit 2 |
| 3 | Out | YY1 | Luminance Out bit 1 |
| 2 | Out | YY0 | Luminance Out bit 0 |
| 23 | Out | UV7 | Chrominance Out bit 7 - When CCSEL is low this bus carries the chrominance data. When CCSEL is high this bus carries a constant value of 0x80 (128). |
| 22 | Out | UV6 | Chrominance Out bit 6 |
| 21 | Out | UV5 | Chrominance Out bit 5 |
| 20 | Out | UV4 | Chrominance Out bit 4 |
| 17 | Out | UV3 | Chrominance Out bit 3 |
| 16 | Out | UV2 | Chrominance Out bit 2 |
| 15 | Out | UV1 | Chrominance Out bit 1 |
| 14 | Out | UV0 | Chrominance Out bit 0 |
| 24 | Out | CLK2 | Clock Out 2X - This clock runs at twice the pixel rate |
| 27 | Out | CLK1 | Clock Out 1X - This clock runs at the pixel rate. |
| 34 | In | OUTEN | Output Enable - When this input is low, the signals YY[7..0], UV[7..0], HSYNC, VSYNC, CLK2, CLK1, HACT, VACT, FIELD and BFLAG are driven. When this input is high, these signals are high-impedance. |

* CamPort inputs are TTL levels. All other inputs are CMOS. See Static Electrical Characteristics table.

| | | | |
|---|---|---|---|
| 12 | Out | VSYNC | Vertical Sync - This signal goes active for 3 horizontal lines to mark the beginning of each field. In Odd fields, it starts and ends when HSYNC and HACT are low. In Even fields, it starts and ends when HSYNC and HACT are active. This signal's polarity is programmable, but defaults to active low on reset. |
| 13 | Out | HSYNC | Horizontal Sync - This signal goes active and returns inactive in the horizontal blanking interval to mark the beginning of each line. This signal's polarity is programmable, but defaults to active low on reset. |
| 28 | Out | HACT | Horizontal Active - This signal is active when there is valid video data on the luminance and chrominance busses. Data is valid only when this signal and VACT are active. HACT can be programmed to only go active on active lines (HACT = HACT AND VACT), but defaults at reset to active on all lines. This signal's polarity is also programmable, but defaults to active high on reset. |
| 29 | Out | VACT | Vertical Active - This signal is active when there is valid video data on the luminance and chrominance busses. Data is valid only when this signal and HACT are active. VACT can be programmed to only go active on active lines during active pixels (VACT = HACT AND VACT), but defaults at reset to active for entire lines only. This signal's polarity is also programmable, but defaults to active high on reset. |
| 30 | Out | FIELD | Field Flag - This signal indicates the field. When it is low, the field is odd. When it is high, the field is even. |
| 31 | Out | BFLAG | Blue Flag - This signal indicates when Blue chrominance data is on the chrominance bus. |
| 35 | In | CCSEL | CCIR 656 Select - When this input is high, the YY[7..0] bus carries multiplexed luminance and chrominance data in conformance with CCIR 656. When this signal is low, the YY[7..0] bus carries only luminance data. |
| 36 | In | RCLK | Register Clock - This input clocks the control circuitry in the chip and must be running in order to access the registers via the I²C bus. The frequency on this input should be between 10 and 33 MHz. |
| 38 | In | INVI | Inverter In - This CMOS Schmidt trigger input controls the INVO output. This inverter can be used to form an RC oscillator to drive the input RCLK. It is typically connected through a resistor to INVO and through a capacitor to GND. This oscillator has a period roughly equal to the time constant R*C. |
| 37 | Out | INVO | Inverter Out - This signal outputs the opposite level from that applied to INVI. If this inverter is used to form an RC oscillator, this pin would be connected to RCLK. |
| 42 | In | OSXI | Oscillator Crystal Input - The crystal oscillator is another way to produce a clock for the input RCLK. A crystal is connected between this input and OSXO. |
| 41 | Out | OSXO | Oscillator Crystal Output - A crystal is connected between this output and OSXI. |
| 39 | Out | OSCO | Oscillator Output - If the crystal oscillator is used to produce the register clock, this CMOS output drives the RCLK input. |
| 45 | In | IAD3 | I²C Address Select Bit 3 - The IAD[3..1] inputs select the I²C address that the chip will respond to. The address is 0x60 + 8 * IAD3 + 4 * IAD2 + 2 * IAD1. |
| 43 | In | IAD2 | I²C Address Select Bit 2 |
| 40 | In | IAD1 | I²C Address Select Bit 1 |
| 48 | In | SDAI | Serial Data In - This input is connected to the I²C Data line. It may be connected through a filter to reduce noise susceptibility. |
| 47 | Out | SDAO | Serial Data Out - This open-drain output connects directly to the I²C Data line. |
| 46 | Out | SDMN | Serial Data Monitor - This output is low when the SDAO output is driving low. This output is high when the SDAO output is high impedance. |
| 49 | In | SCLI | Serial Clock In - This input is connected to the I²C Clock line. It may be connected through a filter to reduce noise susceptibility. |

| | | | |
|---|---|---|---|
| 89 | Out | SCLOA | Serial Clock Out Port A - This output drives the level on the SCLI input when the CamPort™ A is selected. When the CamPort™ B is selected this output is driven high. This is not an open-drain output. |
| 90 | Out | SCLOB | Serial Clock Out Port B - This output drives the level on the SCLI input when the CamPort™ B is selected. When the CamPort™ A is selected this output is driven high. This is not an open-drain output. |
| 99 | Out | GPIO7 | General Purpose I/O Bit 7 - This bus represents eight general purpose I/O pins. Each bit may programmed to be an input or an ouput; on reset, all GPIO pins default to high impedance (tri-state) inputs. |
| 98 | Out | GPIO6 | General Purpose I/O Bit 6 |
| 97 | Out | GPIO5 | General Purpose I/O Bit 5 |
| 96 | Out | GPIO4 | General Purpose I/O Bit 4 |
| 95 | Out | GPIO3 | General Purpose I/O Bit 3 |
| 94 | Out | GPIO2 | General Purpose I/O Bit 2 |
| 93 | Out | GPIO1 | General Purpose I/O Bit 1 |
| 92 | Out | GPIO0 | General Purpose I/O Bit 0 |
| 52 | In | TST0 | Test Pin - This pin should be tied low. |
| 53 | In | TST1 | Test Pin - This pin should be tied low. |
| 61 | In | TST2 | Test Pin - This pin should be tied low. |
| 62 | In | TST3 | Test Pin - This pin should be tied low. |
| 63 | In | TST4 | Test Pin - This pin should be tied low. |
| 71 | In | TSTOE | Test Output Enable - This pin should be tied high. |
| 64, 65, 66, 67, 70, 72, 73, 74, 77, 78, 79, 80, 81, | Out | TOUT | Test Outputs - These pins should be unconnected. |
| 1, 7, 19, 25, 32, 51, 57, 69, 75, 82, | In | GND | Power |
| 8, 18, 26, 33, 50, 58, 68, 76, 83, 100 | In | VDD | Power |

## REGISTER DESCRIPTIONS

The VP7615 iCamHost™ processor station address is strap-configurable to any even location between 0x60 and 0x6E inclusive. Since most iCam cameras currently built use the Station Address 0x68, it is recommended that the iCamHost™ be strapped to a different address. The register addresses shown below are the sub-addresses written to the iCamHost™ immediately after the Station Address. The 7 LSBs of the sub-address must match the specified address. The MSB of the sub-address controls the auto-increment feature of the iCamHost™. If the MSB of the sub-address is a '1', (sub-addresses 0x80 through 0xFF), the sub-address register in the iCamHost™ is incremented to the next address immediately after the data register is read or written. If the MSB of the sub-address is a '0', (sub-addresses 0x00 through 0x7F), the sub-address register in the iCamHost™ remains constant regardless of any reads or writes to the data register. All registers default to 0x00 following chip reset unless otherwise noted.

**Address 0x00 Configuration Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Cfg3 | Cfg2 | Cfg1 | Cfg0 |

Bits 7 - 4 Always read as '0'

Bit 3 Cfg3 - Camera Input Port Enable
'1' CamPort™ 'B' is source
'0' CamPort™ 'A' is source

Bit 2 Cfg2 - Colour Bar Enable
'1' Colour Bar Test Pattern Output
'0' Normal Video Output

Bit 1 Cfg1 - RGB to YUV Converter Bypass
'1' Green + BnR Pattern Output
'0' Normal YUV Output

Bit 0 Cfg0 - Separator Bypass
'1' Sum = CCD Data, Diff = 0
'0' Normal Separator Output

**Address 0x01 RESERVED**

**Address 0x02 Peak Luma Filter Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | PLF2 | PLF1 | PLF0 |

Bits 7 - 3 Always read as '0'

Bits 2 - 0 Peak Luma Filter Control
'000' - PLF K = 1, No Luma Filter
'001' - PLF K = 1/2, Fast Luma Filter
'010' - PLF K = 1/4, Med Fast Luma Filter
'011' - PLF K = 1/8, Med Slow Luma Filter
'1XX' - PLF K = 1/16, Slow Luma Filter

**Address 0x03 RESERVED**

**Address 0x04 Horizontal Start Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HStrt7 | HStrt6 | HStrt5 | HStrt4 | HStrt3 | HStrt2 | HStrt1 | HStrt0 |

Bits 7 - 0 Horizontal Start Register
Four times the value of this register is the
Horizontal starting pixel for the Metrics window.

**Address 0x05 Horizontal Stop Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HStop7 | HStop6 | HStop5 | HStop4 | HStop3 | HStop2 | HStop1 | HStop0 |

Bits 7 - 0 Horizontal Stop Register
Four times the value of this register is the
Horizontal ending pixel for the Metrics window.

**Address 0x06 Vertical Start Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VStrt7 | VStrt6 | VStrt5 | VStrt4 | VStrt3 | VStrt2 | VStrt1 | VStrt0 |

Bits 7 - 0 Vertical Start Register
Four times the value of this register is the
Vertical starting line (in the frame) for the
Metrics window (two times in the field).

**Address 0x07 Vertical Stop Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VStop7 | VStop6 | VStop5 | VStop4 | VStop3 | VStop2 | VStop1 | VStop0 |

Bits 7 - 0 Vertical Stop Register
Four times the value of this register is the
Vertical ending line (in the frame) for the
Metrics window (two times in the field).

**Address 0x08 Horizontal Aperture Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HApt7 | HApt6 | HApt5 | HApt4 | 0 | 0 | 0 | 0 |

Bits 7 Horizontal Aperture Sign Bit
‘1’ Correction is negative (blurring)
‘0’ Correction is positive (sharpening)

Bits 6 - 4 Horizontal Aperture Control Value
‘000’ - No Aperture Correction
|
‘111’ - Maximum Aperture Correction

Bits 3 - 0 Always read as ‘0’

**Address 0x09 Vertical Aperture Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VApt7 | VApt6 | VApt5 | VApt4 | 0 | 0 | 0 | 0 |

Bits 7 Vertical Aperture Sign Bit
‘1’ Correction is negative (blurring)
‘0’ Correction is positive (sharpening)

Bits 6 - 4 Vertical Aperture Control Value
‘000’ - No Aperture Correction
|
‘111’ - Maximum Aperture Correction

Bits 3 - 0 Always read as ‘0’

**Address 0x0A GPIO Output Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GPOE7 | GPOE6 | GPOE5 | GPOE4 | GPOE3 | GPOE2 | GPOE1 | GPOE0 |

Bit 7 GPIO7 Output Enable
Bit 6 GPIO6 Output Enable
Bit 5 GPIO5 Output Enable
Bit 4 GPIO4 Output Enable
Bit 3 GPIO3 Output Enable
Bit 2 GPIO2 Output Enable
Bit 1 GPIO1 Output Enable
Bit 0 GPIO0 Output Enable

'0' = Corresponding GPIO pin is tristated/not driven.
'1' = Corresponding GPIO pin is driven to level of corresponding bit in GPIO Output Register.

**Address 0x0B GPIO Output Register** **Write Only**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GPO7 | GPO6 | GPO5 | GPO4 | GPO3 | GPO2 | GPO1 | GPO0 |

Bit 7 GPIO7 Output Level
Bit 6 GPIO6 Output Level
Bit 5 GPIO5 Output Level
Bit 4 GPIO4 Output Level
Bit 3 GPIO3 Output Level
Bit 2 GPIO2 Output Level
Bit 1 GPIO1 Output Level
Bit 0 GPIO0 Output Level

'0' = If corresponding GPIO Output Enable bit is '1', then drive the appropriate GPIO pin to '0'
'1' = If corresponding GPIO Output Enable bit is '1', then drive the appropriate GPIO pin to '1'
'X' = If the corresponding GPIO Output Enable bit it '0', then tri-state the appropriate GPIO pin.

**Address 0x0B GPIO Input Register** **Read Only**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GPI7 | GPI6 | GPI5 | GPI4 | GPI3 | GPI2 | GPI1 | GPI0 |

Bits 7 - 0 GPIO Input Register
This register represents the level on the corresponding GPIO pins.

**Address 0x0C Output Sense Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SWPYUV | SWPUV | VAG | HAG | VAS | HAS | VSS | HSS |

Bit 7 SWPYUV - YY and UV Swap
- '0' = Normal: YY and UV are in proper positions
  CCIR601 output mode: YY data on YY bus; UV data on UV bus CCIR656 output mode: UYVY
- '1' = Swapped: YY and UV in each other's positions
  CCIR601 output mode: UV data on YY bus; YY data on UV bus CCIR656 output mode: YUYV .

Bit 6 SWPUV - UV Swap
- '0' = Normal: U and V are in position for CCIR601/656: U before V
- '1' = Swapped: U and V are swapped in time: V before U

Bit 5 VAG - VACT Gate
- '1' = Gated: VACT active gated by HACT
- '0' = Normal: VACT active during Active Lines

Bit 4 HAG - HACT Gate
- '1' = Gated: HACT active gated by VACT
- '0' = Normal: HACT active during Active Pixels

Bit 3 VAS - VACT Sense
- '1' = Active High: VACT = 1 during Active Lines
- '0' = Active Low: VACT = 0 during Active Lines

Bit 2 HAS - HACT Sense
- '1' = Active High: HACT = 1 during Active Pixels
- '0' = Active Low: HACT = 0 during Active Pixels

Bit 1 VSS - VSYNC Sense
- '1' = Active High: VSYNC = 1 during Vertical Sync
- '0' = Active Low: VSYNC = 0 during Vertical Sync

Bit 0 HSS - HSYNC Sense
- '1' = Active High: HSYNC = 1 during Horizontal Sync
- '0' = Active Low: HSYNC = 0 during Horizontal Sync

This register defaults on chip reset to 0x0C.

**Address 0x0D VACT Control Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VAFIX | 0 | VFCnt5 | VFCnt4 | VFCnt3 | VFCnt2 | VFCnt1 | VFCnt0 |

Bit 7 VAFIX - VACT Control
This bit provides backward compatibility for certain iCam cameras.
- '0' = Disabled: VACT controlled by camera timing
- '1' = Enabled: VACT is inactive during a fixed number of lines during Vertical Blanking. This only effects the end, and not the beginning, of Vertical Blanking.

Bit 6 Always read as '0'

Bits 5 - 0 VFCnt5 - VFCnt0
This field modifies the end of Vertical Blanking if VAFIX is '1' by setting the number of lines that VACT will be inactive during Vertical Blanking.

This register defaults on chip reset to 0x3F.

**Address 0x0E Hardware Version Register** **Read Only**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HVer7 | HVer6 | HVer5 | HVer4 | HVer3 | HVer2 | HVer1 | HVer0 |

Bits 7 - 0 Hardware Version Register
0x10 - VP7600
0x11 - VP7610
0x12 - VP7615

**Address 0x0F Timing Status Register** **Read Only**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FCnt5 | FCnt4 | FCnt3 | FCnt2 | FCnt1 | FCnt0 | Fld | VBlk |

Bits 7 - 2 Field Count
A number between 0 and 63 which increments at the beginning of every Vertical Blanking Interval

Bit 1 Field Bit
'1' Even Field - Digital Field 2
'0' Odd Field - Digital Field 1

Bit 0 Vertical Blanking
'1' Vertical Blanking Interval
'0' Vertical Active Interval

**Address 0x10 Lower Byte Red Chroma Register** **Read Only**
This register contains Bits 07 - 00 of the Sum of the Red Chrominance of the pixels within the Metrics window.

**Address 0x11 Lower Middle Byte Red Chroma Register** **Read Only**
This register contains Bits 15 - 08 of the Sum of the Red Chrominance of the pixels within the Metrics window.

**Address 0x12 Upper Middle Byte Red Chroma Register** **Read Only**
This register contains Bits 23 - 16 of the Sum of the Red Chrominance of the pixels within the Metrics window.

**Address 0x13 Upper Byte Red Chroma Register** **Read Only**
This register contains Bits 31 - 24 of the Sum of the Red Chrominance of the pixels within the Metrics window.

**Address 0x14 Lower Byte Blue Chroma Register** **Read Only**
This register contains Bits 07 - 00 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

**Address 0x15 Lower Middle Byte Blue Chroma Register** **Read Only**
This register contains Bits 15 - 08 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

**Address 0x16 Upper Middle Byte Blue Chroma Register** **Read Only**
This register contains Bits 23 - 16 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

**Address 0x17 Upper Byte Blue Chroma Register** **Read Only**
This register contains Bits 31 - 24 of the Sum of the Blue Chrominance of the pixels within the Metrics window.

**Address 0x18 Lower Byte Luminance Register** **Read Only**
This register contains Bits 07 - 00 of the Sum of the Luminance of the pixels within the Metrics window.

**Address 0x19 Lower Middle Byte Luminance Register** **Read Only**
This register contains Bits 15 - 08 of the Sum of the Luminance of the pixels within the Metrics window.

**Address 0x1A Upper Middle Byte Luminance Register** **Read Only**
This register contains Bits 23 - 16 of the Sum of the Luminance of the pixels within the Metrics window.

**Address 0x1B Upper Byte Luminance Register** **Read Only**
This register contains Bits 31 - 24 of the Sum of the Luminance of the pixels within the Metrics window.

**Address 0x1C Peak Luminance Register** **Read Only**
This register contains the peak value of the filtered Luminance of the pixels within the Metrics window.

**Address 0x20 Sum to Red Coefficient Register** **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the Sum signal.

**Address 0x21 AmB to Red Coefficient Register** **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the AmB signal.

**Address 0x22 CmD to Red Coefficient Register** **Read/Write**
This register contains the magnitude of the Coefficient which determines the contribution to the Red signal from the CmD signal.

**Address 0x23 Red Coefficients Sign Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | RCmD | RAmB |

Bit 1 Sign for CmD to Red Coefficient
Bit 0 Sign for AmB to Red Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

**Address 0x24 Sum to Green Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the Sum signal.

**Address 0x25 AmB to Green Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the AmB signal.

**Address 0x26 CmD to Green Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Green signal from the CmD signal.

**Address 0x27 Green Coefficients Sign Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | GCmD | GAmB |

Bit 1 Sign for CmD to Green Coefficient
Bit 0 Sign for AmB to Green Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

**Address 0x28 Sum to Blue Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the Sum signal.

**Address 0x29 AmB to Blue Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the AmB signal.

**Address 0x2A CmD to Blue Coefficient Register** **Read/Write**

This register contains the magnitude of the Coefficient which determines the contribution to the Blue signal from the CmD signal.

**Address 0x2B Blue Coefficients Sign Register** **Read/Write**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | BCmD | BAmB |

Bit 1 Sign for CmD to Blue Coefficient
Bit 0 Sign for AmB to Blue Coefficient
'1' Coefficient is negative
'0' Coefficient is positive

**Addresses 0x30 - 0x3F Gamma Values Write Register** **Write**

The 16 values that are written to these registers determine the breakpoints in the Gamma correction circuit. The lower four bits of the address are ignored on writes, and the data values are pushed on to an internal shift register. The writes should start with the lowest value and end with the highest value. The last 16 values written generate the Gamma curve, so all 16 values must be written. It is recommended that all 16 writes occur to address 0x30 with auto-increment disabled.

All sixteen Gamma registers default on chip reset to 0x00.

**Addresses 0x30 - 0x3F Gamma Values Read Register** **Read**

The breakpoints in the Gamma correction circuit are read from these registers.

### Signal Timing

The clock source for the VP7615 is the clock input of the selected CamPort. Since there are two CamPort inputs, the selected clock is brought out as an output, namely CLK2. Since the frequency of this clock is twice the pixel rate, another output, CLK1, is provided which runs at the pixel rate.

It is anticipated that the VP7615 user would use one or both of these clocks to clock the data and timing outputs into another device. In order to assure hold times into any device, the clock outputs CLK1 and CLK2 were inverted inside the VP7615 so that the data and timing outputs would change near the falling edge of these clocks, and would be stable at their rising edges.

The timing specifications characterize the delay from the falling edges of CLK1 and CLK2 to the edges of the data and timing outputs. It is left to the system designer to calculate the available setup and hold times based on these timing specifications, the period of CLK1 and CLK2 and their duty cycles.

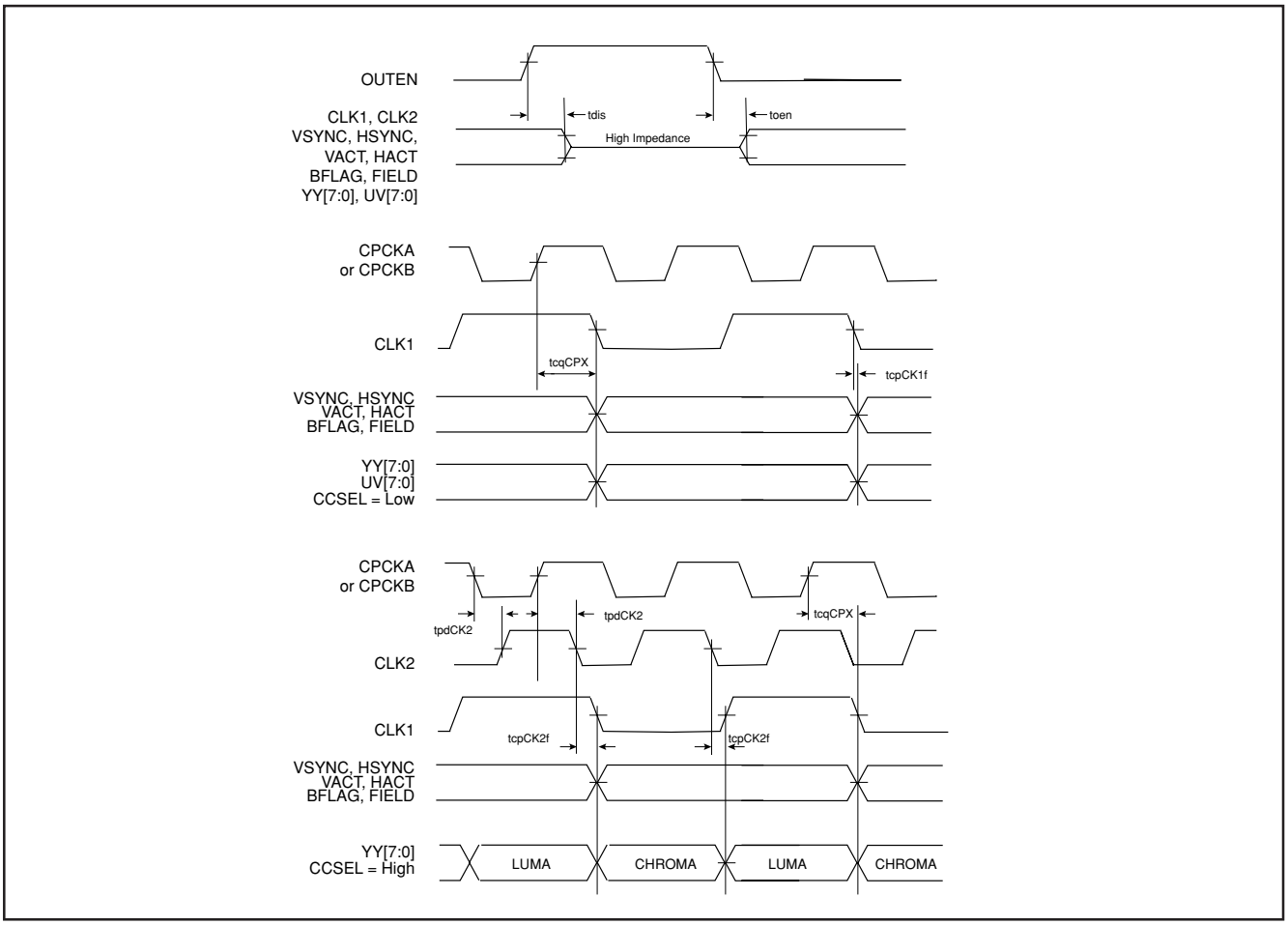



*Fig.2 Video Interface Timing Diagram*

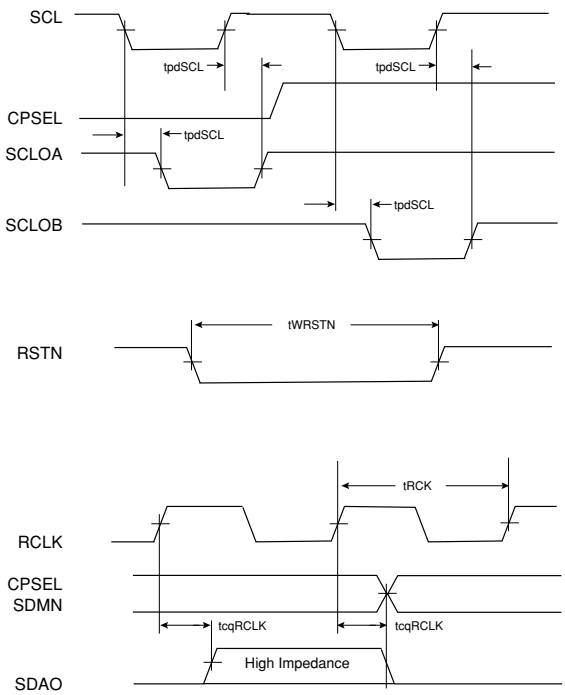



*Fig.3 I²C Timing Diagram*

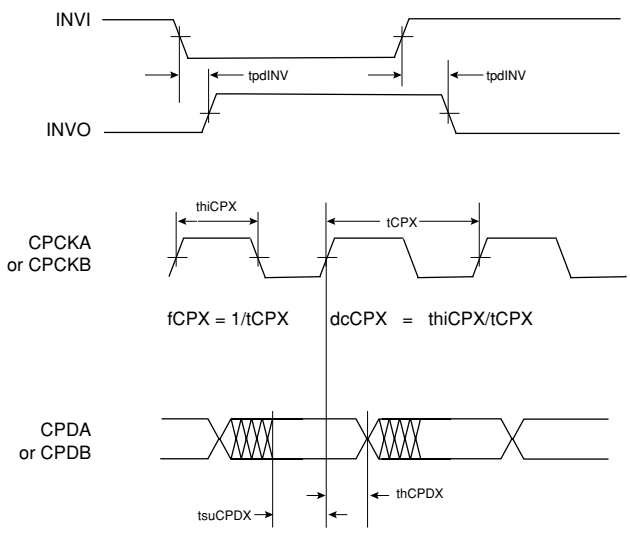



*Fig.4 Clock Timing Diagram*

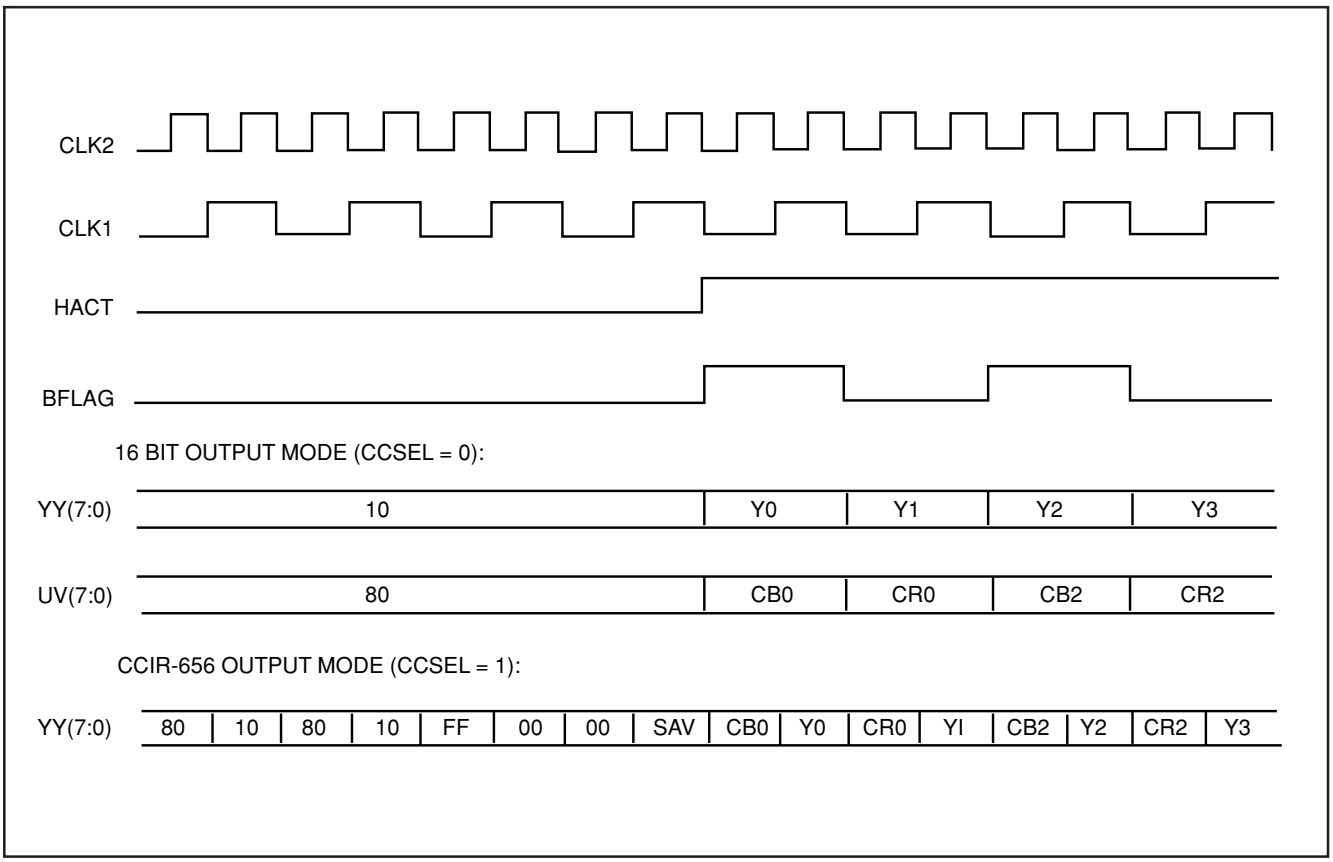



*Fig.5 Start of Active Video*

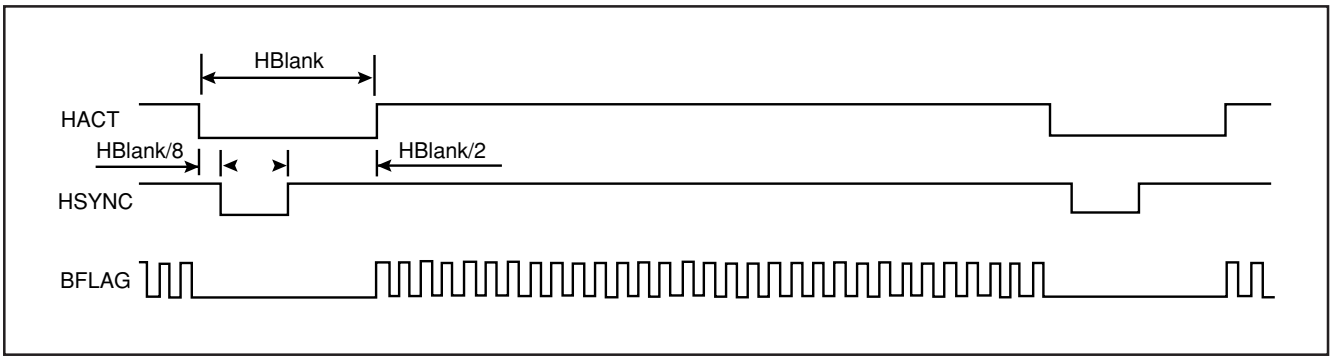



*Fig.6 Horizontal Sync Timing*

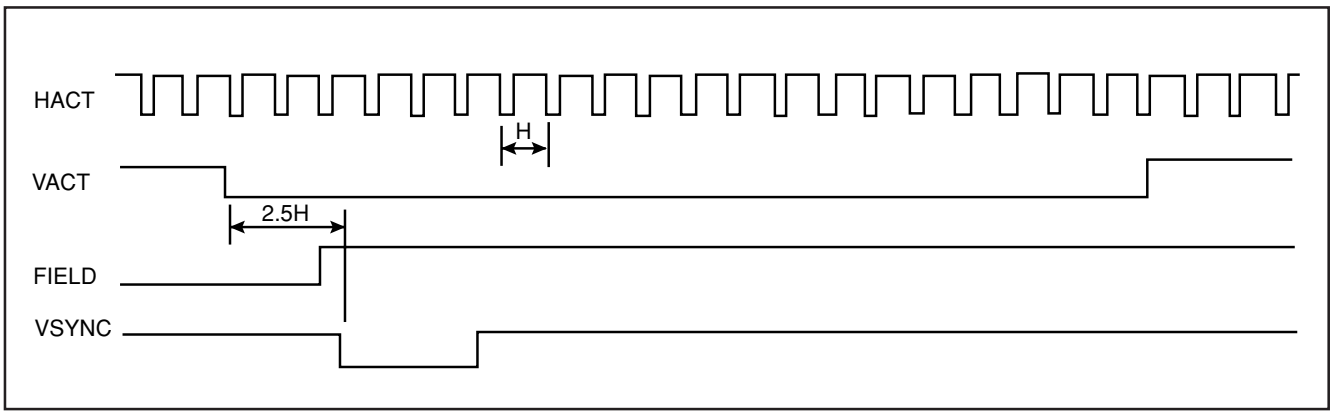



*Fig.7 Even Field Timing*

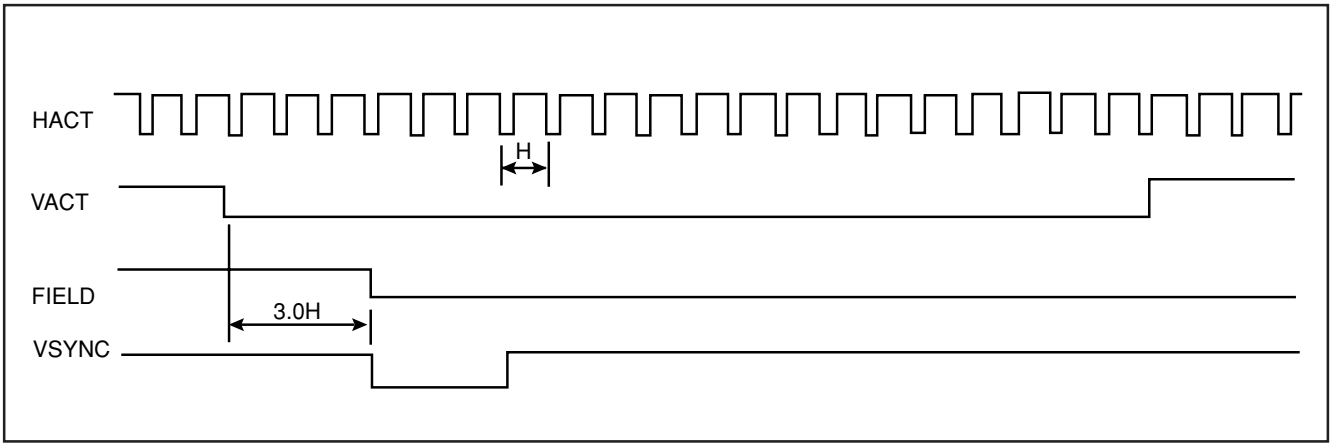



*Fig.8 Odd Field Timing*

**TIMING REQUIREMENTS**

| Name | Description | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| fCPX | frequency CPCKA or CPCKB | 0 | 30 | MHz |
| tCPX | period CPCKA or CPCKB | 33 | - | ns |
| dcCPX | duty cycle CPCKA or CPCKB | 40 | 60 | % |
| tsuCPDX | setup time, CPDA [3..0] to CPCKA or CPDB [3..0] to CPCKB | 4 | | ns |
| thCPDX | hold time, CPDA [3..0] to CPCKA or CPDB [3..0] to CPCKB | 4 | | ns |
| fRCK | frequency RCLK | 10 | 33 | MHz |
| twRSTN | pulse width of RSTN | 110 | | ns |

**TIMING CHARACTERISTICS**

| Name | Description | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| tcqRCLK | RCLK to output (CPSEL, SDAO, SDMN) | | 20 | ns |
| tcpCPX | rising edge of CPCKA or CPCKB to output (YY[7..0], UV[7..0], CLK1, VSYNC, HSYNC,VACT, HACT, BFLAG) | | 21 | ns |
| tcqCK2f | falling edge of CLK2 to output (YY[7..0], UV[7..0], CLK1, VSYNC, HSYNC, VACT, HACT, BFLAG) | -2 | 7 | ns |
| tcpCK1f | falling edge of CLK1 to output (YY[7..0], UV[7..0],VSYNC, HSYNC, VACT, HACT, BFLAG) | -3 | 5 | ns |
| tpdCK2 | propagation delay from CPCKA or CPCKB to CK2 | | 12 | ns |
| tpdINV | propagation delay from INVI to INVO | | 11 | ns |
| tpdSCL | propagation delay from SCLI to SCLOA or SCLOB | | 15 | ns |
| tdis | rising edge of OUTEN to outputs tri-state (CLK1, CLK2, VSYNC, HSYNC, VACT, HACT, BFLAG, FIELD, YY[7:0], UV[7:0]) | | 30 | ns |
| toen | falling edge of OUTEN to outputs (CLK1, CLK2, VSYNC, HSYNC, VACT, HACT, BFLAG, FIELD, YY[7:0], UV[7:0]) | | 30 | ns |

## ABSOLUTE MAXIMUM RATINGS [See Notes]

| | |
|---|---|
| Supply voltage VDD | -0.5V to 7.0V |
| Input voltage $V_{IN}$ | -0.5V to VDD + 0.5V |
| Output voltage $V_{OUT}$ | -0.5V to VDD + 0.5V |
| Clamp diode current per pin $I_K$ (see note 2) | 18mA |
| Static discharge voltage (HBM) | 500V |
| Storage temperature $T_S$ | -55°C to 150°C |
| Ambient temperature with power applied $T_{AMB}$ | 0°C to 70°C |
| Junction temperature | 125°C |
| Package power dissipation | 1000mW |

### NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation for 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

## STATIC ELECTRICAL CHARACTERISTICS

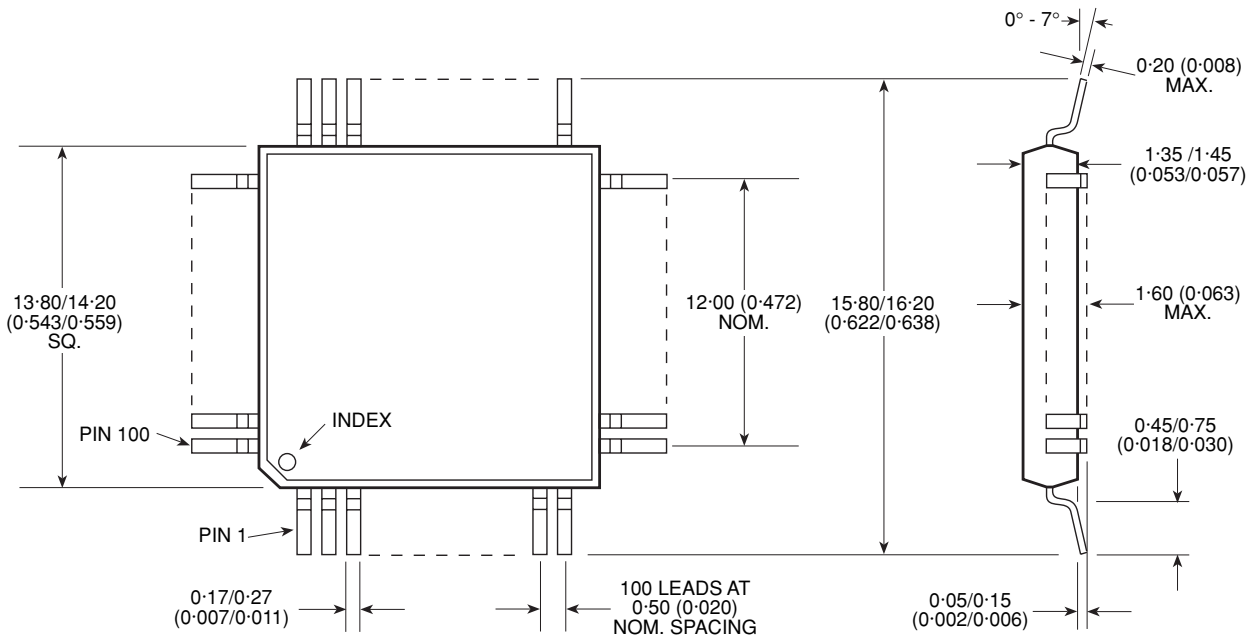
**Operating Conditions (unless otherwise stated)**

$T_{amb}$ = 0°C to +70°C $V_{DD}$ = 5.0v ± 10%

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | $0.8V_{DD}$ | | - | V | $I_{OH}$ = 4mA |
| Output low voltage | $V_{OL}$ | - | | 0.4 | V | $I_{OL}$ = -4mA |
| Input high voltage (CMOS input) | $V_{IHC}$ | $0.7V_{DD}$ | | - | V | |
| Input low voltage (CMOS input) | $V_{ILC}$ | | | $0.2V_{DD}$ | V | |
| Input high voltage (TTL input) | $V_{IHT}$ | 2.0 | | - | V | |
| Input low voltage (TTL input) | $V_{ILT}$ | | | 0.8 | V | |
| Input leakage current | $I_{IN}$ | -1 | | +1 | µA | GND < $V_{IN}$ < $V_{DD}$ |
| Input capacitance | $C_{IN}$ | | 10 | | pF | |
| Output leakage current | $I_{OZ}$ | -1 | | +1 | µA | GND < $V_{OUT}$ < $V_{DD}$ |
| Output S/C current | $I_{SC}$ | 10 | | 300 | mA | $V_{DD}$ = Max |

## PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.




NOTES
1. Controlling dimensions are millimetres.
2. Pin 1 indicator may be a corner chamfer, dot or both.
3. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

**100-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FPD100**

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