Preliminary

Product Summary

Zeus™ 36 x 36, 2.5Gb/s (STS-48/STS-48c/STM-16) with OC-192 Support SONET/SDH STS-1 Grooming Switch

GENERAL DESCRIPTION

The VC2001 SONET/SDH Grooming Switch accepts 36 STS-48 input streams and generates 36 STS-48 output streams (or 9 STS-192 streams that have been de-multiplexed 1:4). It allows each STS-1 component of each input stream to be directed to an arbitrary STS-1 slot in an arbitrary output stream. In effect, it is a 1728 x 1728 STS-1 switch. The VC2001 also supports STS-192c mode.

The VC2001 utilizes Velio's high-speed Gigacores (SERializer and DESerializer cores) for its 2.488Gb/s serial I/O signals. The user-selectable features of each GigaCore address Inter-Symbol Interference (ISI), and help ensure signal integrity at multi-gigabit speeds. Most importantly, the integrated 2.488Gb/s Gigacores enable the VC2001 to drive electrical backplanes directly, without the need for external transceivers.

Table 1: VC2001 Features and Benefits

FEATURES	BENEFITS
36x36 STS-48/STS-48c (2.488 Gb/s) or 9x9 STS-192/STS-192c (9.95 Gb/s de-multiplexed 1:4) Cross-Connect	High Bandwidth, Intelligent Switching Capability: 90 Gb/s In, 90 Gb/s Out STS-1 Level Grooming Capability
11W Power Consumption	Reduces overall system power requirements
Cross-Connect Switching at STS-1 Granularity (1728 x 1728)	Non-blocking for unicast, dualcast and multicast traffic
SONET/SDH Input Processing per channel - 2.5 GHz on-chip Clock Recovery/Demultiplexer - Frame detection, byte monitoring	Standard SONET/SDH processing
SONET/SDH Output Processing per channel - 2.5 GHz On-Chip Clock Generation/Multiplexer - Single Byte Insertion within a frame for diagnostics	Standard SONET/SDH processing
CML High-Speed Serial I/O with Programmable Output Voltage Swing	Serial Output Signal can be tailored to specific system conditions on a per-channel basis
Adjustable Transmit Pre-Emphasis on Serial Outputs	Reduces Inter-Symbol-Interference, enables serial transmission over longer distances
Optional Receiver Equalization on Serial Inputs	Reduces Inter-Symbol-Interference, enables serial transmission over longer distances
37.5 mm x 37.5 mm BGA	Thermally enhanced package

APPLICATIONS

- **SONET/SDH Broadband Cross Connect** (STS-48(c)/STS-192(c)/STM-16/STM-48)
- **SONET/SDH Broadband Add/Drop Multiplexer** (STS-48/STS-192/STM-16/STM-64)

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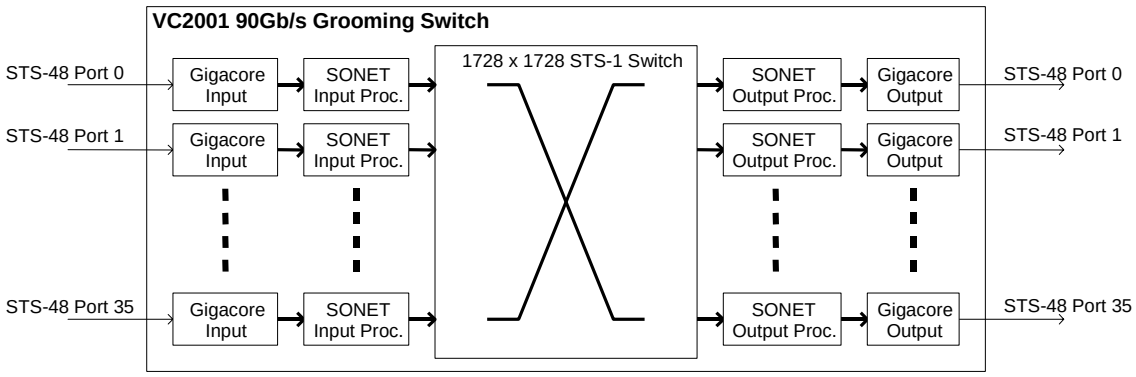

Figure 1: VC2001 Block Diagram

Configurable Serial Outputs for Signal Integrity

The VC2001 utilizes a programmable SERializer and DESerializer core for high-speed serial I/O signals. The user-selectable features uniquely address Inter-Symbol Interference (ISI), and help ensure signal integrity at multi-gigabit speeds.

Programmable Pre-Emphasis

To counteract the effects of ISI, the VC2001 serial output signal has an optional pre-emphasis component. This results in a detectable data signal over longer trace lengths.

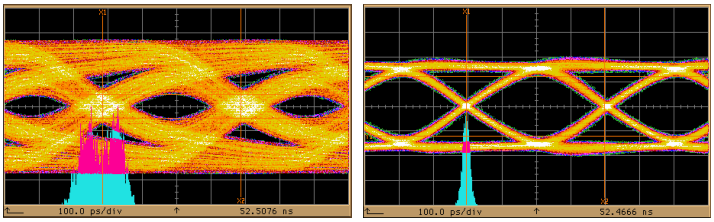

Figure 2: Pre-emphasis effects on Signal Integrity; a 2.488 Gbps signal through 40" of FR4: disabled (left), and enabled (right)