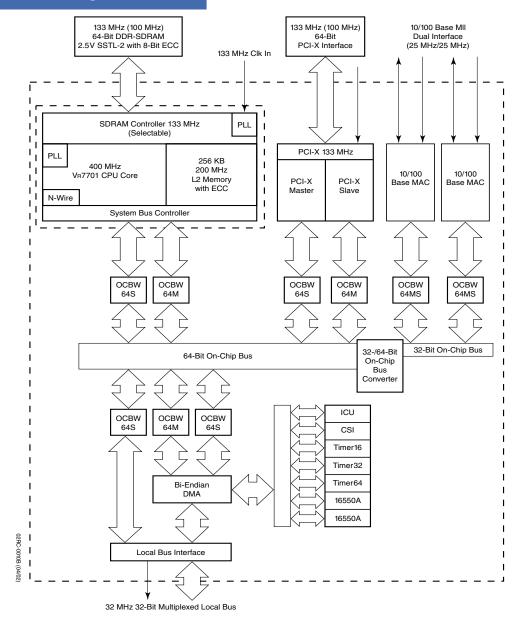
# VR Series



### Description

The 64-bit VR7701<sup>™</sup> (µPD30771) MIPS<sup>®</sup> microprocessor is particularly suited for designs requiring a high-performance embedded system processor. Features include a 133 MHz double data rate (DDR) SDRAM controller, 133 MHz PCI-X interface, an on-chip L2 cache, two 10/100 Base Ethernet media access controllers (MACs), and a variety of other peripherals. The execution pipeline selects two of 16 fetched instructions in out-of-order manner and dispatches them to the appropriate integer unit, floating-point unit, branch prediction unit, or load/store unit.

## **Block Diagram**



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#### **CPU Core**

- 64-bit RISC VR5500 CPU core
- MIPS64-compatible instruction set
- Ten-stage superscalar pipeline with out-oforder execution
- 400 MHz pipeline clock
- 48 double-entry translation lookaside buffer (TLB)
- 36-bit physical and 40-bit virtual address space
- Floating-point unit (FPU)
- Primary cache memory
  - 32 Kb instruction and 32 Kb data
  - Two-way set associative
    - Line locking
- N-wire on-chip debugging interface
- Phase-locked loops with multiple clock modes supplied by internal clock derived from external source

#### On Chip Secondary Cache (L2) Memory

- 256 Kb; 4-way set associative
- Cache line locking
- Secondary cache operating frequency 200 MHz
- Error detection and correction protection

#### **DRAM Controller**

- 64-bit data bus with or without SEC/DED ECC
- 100 MHz or 133 MHz SDR/DDR memory
- Maximum 1 Gb x 8-, x16-, x32-bit width DRAM
- Maximum 4 Gb memory space divided into as many as 4 banks
- SSTL\_2, LVTTL level interface

#### **PCI-X** Interface

- Configurable for PCI-X at 133 MHz, 100 MHz, 66 MHz or PCI: 33 MHz
- 64-bit PCI-X rev.1.0; 64-bit PCI rev 2.2
- Host bridge allowing bidirectional control
- Asynchronous operation with CPU clock

#### Process

• 0.13 µm, 6AL process

#### Local Bus Interface

- 32-bit address/data 33 MHz multiplexed bus
- Configurable 8-, 16-, 32-bit bus sizing
- 128 MB address space
- Bi-endian
- Five chip select pins
- Four-channel DMA
- LVTTL interface

#### **Ethernet MAC Interface**

- 10/100 Base MAC with Media Independent Interface (MII)
- Two channels

#### Serial Interface

- Two-channel 16550-compatible UART controller
- One-channel synchronous interface (CSI)
  master mode

#### **Other Peripherals**

- Six-channel 16-bit interval timer
- Two-channel 32-bit interval timer
- One-channel 64-bit interval timer
- Eight-channel external interrupt input
- 16-level interrupt controller
- JTAG interface for NEC N-wire debugging (in-circuit emulator)

#### **Operating Temperature**

• Tc (case temperature) = 0°C - 85°C

#### Supply voltage

- Core: 1.5 V
- DRAM I/O: 2.5V
- Other I/O: 3.3V
- Low-power standby mode

#### Package

• 500-pin PBGA package (40 mm x 40 mm)

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