

# VSC8184

VITESSE

## 11.5-12.5Gb/s 1:16 Demultiplexer with Clock Recovery



### BENEFITS:

- ▶ Provides High-speed Integrated Clock and Data Recovery from 11.5 to 12.5Gb/s
- ▶ Provides Lowest Power Solution in its Performance Class
- ▶ Pin-compatible Path to 9.9 - 10.7Gb/s Product (VSC8174)
- ▶ Thermal Expansion of TBGA Package is Matched to the PC Board for High Reliability
- ▶ Data Polarity Invert and Bit Order Swap for Ease of Layout
- ▶ Loss-of-Lock and No Reference Clock to Assist in Monitoring Device Operation
- ▶ Parity Bit Calculation
- ▶ Integrated Clock and Data Recovery

### FEATURES:

- ▶ Continuous 11.5 to 12.5Gb/s Lock-Range
- ▶ Low Power 1.6W (Typ)
- ▶ +3.3V Single Supply
- ▶ Single-End and Differential Data Input
- ▶ 10 mV Input Sensitivity (Min)
- ▶ Slicing Threshold Voltage Offset Control
- ▶ LVDS Outputs
- ▶ 22-24, 180-195 or 719-781 MHz Reference Clock
- ▶ Reliable 90-Ball BGA Package
- ▶ On Chip Termination for all LVDS Inputs
- ▶ Up to 85°C Case Temperature

### APPLICATIONS:

- ▶ Advanced Forward Error Correction (FEC)
- ▶ Return-to-Zero Transmission Applications
- ▶ Re-Timing Laser Drivers
- ▶ Ultra-Long Haul Systems
- ▶ SONET/SDH Networking
- ▶ DWDM Systems
- ▶ Telecommunications Transmission Systems
- ▶ Test Equipment

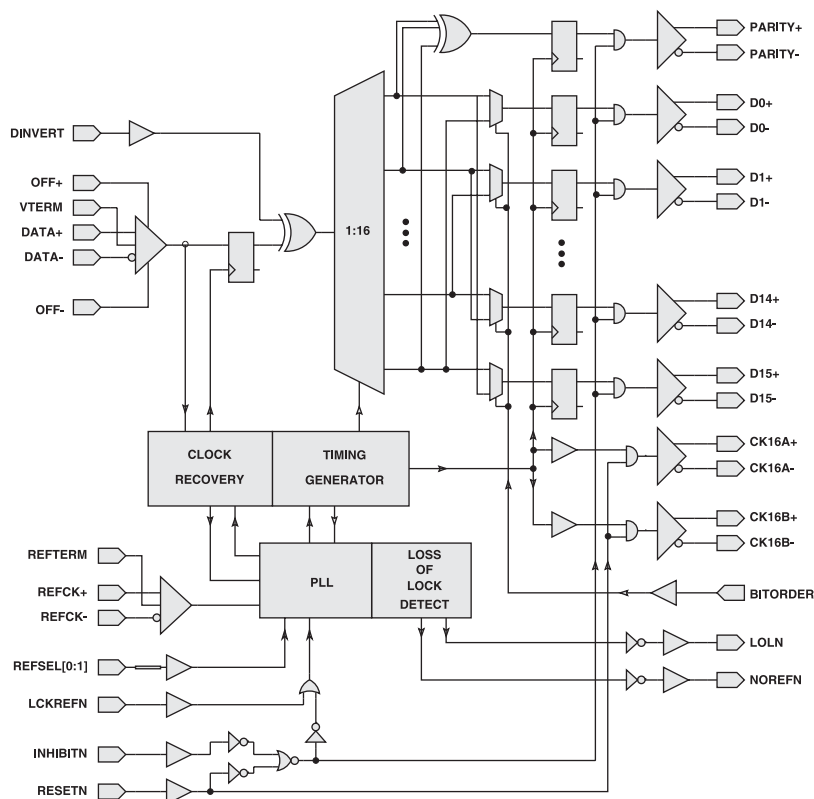
## 11.5-12.5Gb/s 1:16 Demultiplexer with Clock Recovery

### GENERAL DESCRIPTION:



The VSC8184 combines a clock recovery unit and data retiming with a 1:16 Demultiplexer on a single chip to directly generate 16-bit wide data from an incoming 11.5Gb/s to 12.5Gb/s data stream, for use in SONET STS-192/SDH STM-64 systems. An on-chip Phase Locked Loop (PLL) with Voltage Controlled Oscillator (VCO) generates a 11.5GHz to 12.5GHz clock, which remains phase locked to the incoming data. The incoming data is retimed and Demultiplexed into 16 parallel outputs. It features a highly flexible reference clock input scheme. The user can select between 22-24 MHz, 180-195MHz or 719-781MHz LVPECL reference clock inputs. The input serial data sampling point voltage threshold can be adjusted. Additional features include a parity bit (PARITY±) that is clocked out with the 16 parallel data, Bit Order Swap (BITORDER) and Data Polarity Invert (DINVERT). To assist in monitoring device operation a Loss-of-Lock (LOLN) alarm and no reference clock (NOREFN) alarm are provided. The device is packaged in a modified 90-ball, Ball Grid Array (BGA).

### VSC8184 BLOCK DIAGRAM:



### SPECIFICATIONS:

- ▶ 11.5 to 12.5 Gb/s Continuous Lock-Range Operation
- ▶ 10 mV Input Sensitivity
- ▶ Supply Voltage: 3.3V (Typ)
- ▶ Total Power Dissipation: 1.6W (Typ)
- ▶ 15x15mm Low Profile 90 Ball TBGA (Taped BGA) Package
- ▶ Operating Temperature Range: 0°C to +85°C (case)

### Your Partner for Success.

For more information on Vitesse Products visit the Vitesse web site at [www.vitesse.com](http://www.vitesse.com) or contact Vitesse Sales at (800) VITESSE or [sales@vitesse.com](mailto:sales@vitesse.com)

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