PHYSICAL LAYER PRODUCTS

VSC8185

VITESSE

11.5-12.5Gb/s 16:1 Multiplexer and Clock Generator with High-Speed Clock Output

BENEFITS:

- Provides High-speed Output Clock for RZ and Re-timed Laser Driver Applications
- Provides Lowest Power Solution in its Performance Class
- Pin-compatible Path to 9.9 to 10.7Gb/s Product (VSC8175)
- Integrated PLL Based Clock Generator
- True LVDS Parallel Data Interface
- Thermal Expansion of TBGA Package is Matched to the PC Board for High Reliability
- Input FIFO to Simplify Parallel Interface Timing
- Data Polarity Invert and Bit Order Swap for Ease of Layout

FEATURES:

- High Speed Operation Up to 12.5Gb/s with Integrated Clock Multiplier Unit
- High-Speed Output Clock
- Narrow Clock-to-Data Skew Range
- Superior Data Output Eyes
- Low Power 2W
- +3.3V Single Supply
- Continuous Tuning Operation from 11.5 to 12.5Gb/s Rates
- 180/195 or 719/781 MHz Reference Clock Input
- Reliable 90-Ball TBGA Package
- Up to 85°C Case Temperature

APPLICATIONS:

- Advanced Forward Error Correction (FEC)
- Return-to-Zero Transmission Applications
- Re-Timing Laser Drivers
- Ultra-Long Haul Systems
- SONET/SDH Networking
- DWDM Systems
- Telecommunications Transmission Systems
- Test Equipment

VSC8185

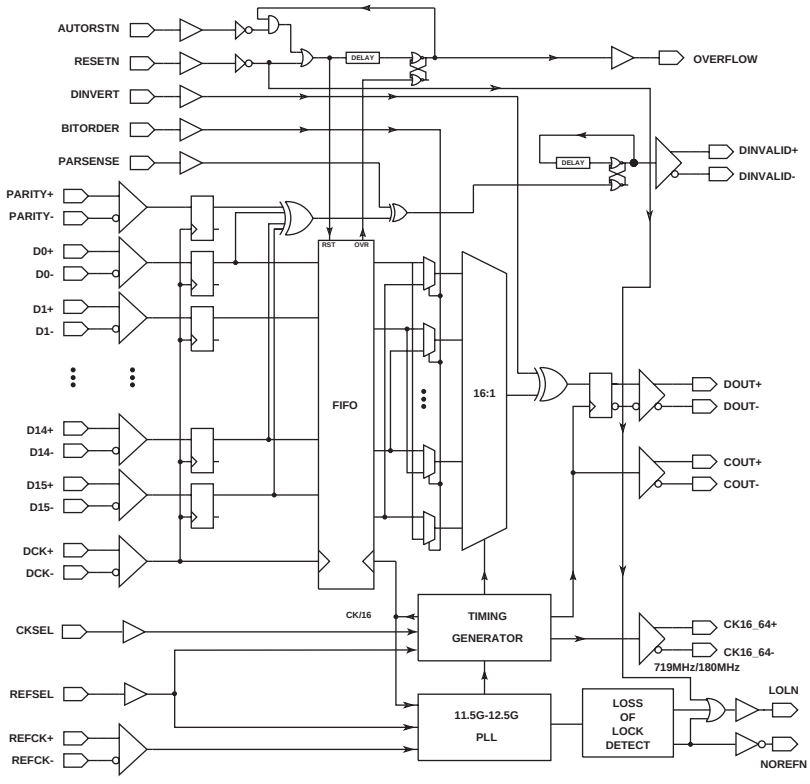
VITESSE

11.5-12.5Gb/s 16:1 Multiplexer and Clock Generator with High-Speed Clock Output

GENERAL DESCRIPTION:

The VSC8185 consists of a 16:1 Multiplexer and a clock generator for use in SONET STS-192/SDH STM-64 systems. The 16:1 Multiplexer accepts 16 parallel low voltage differential swing (LVDS) inputs (D[0:15]±) and (PARITY±) at a data rate of 718.8 to 781.3 Mb/s. This parallel data stream is then serialized into a 11.5Gb/s to 12.5Gb/s output (DOUT±). The clock generator creates the 11.5GHz to 12.5GHz clock signal used to re-time the transmitted serialized data. The clock generator requires a 180-195MHz or 719-781MHz LVPECL reference clock input (REFCK±). To ease timing constraints on the parallel interface, a 16 bit wide FIFO is included. A high speed clock output (COUT±) is provided that is synchronized to the high speed serial data output. A divide-by-16 or divide-by-64 LVDS clock output (CK16_64±) is available for use as a clock input to the data source of the parallel inputs (D[0:15]±) and (PARITY±). Additional features include parity bit (PARITY±) that is clocked in with the 16-bit parallel data. Bit Order Swap (BITORDER) and Data Polarity Invert (DINVERT). To assist in monitoring device operation a Loss-of-Lock (LOLN) alarm and internal temperature diode are included. The device is packaged in a modified 90-ball, Ball Grid Array (BGA).

VSC8185 BLOCK DIAGRAM:



SPECIFICATIONS:

- 11.5 to 12.5Gb/s Continuous Operation
- Data Output Voltage Swing: 500 mV (min)
- Data Output Rise/Fall: 25 ps (Typ)
- High Speed Clock Voltage Swing: 500 mV (min)
- +/- 15 ps Clock-to-Data Skew Range Over Temperature
- Supply Voltage: 3.3V (Typ)
- Operating Temperature Range: 0°C to +85°C (case)
- 15x15mm Low Profile 90 Ball TBGA (Taped BGA) Package
- Total Power Dissipation: 2W

Your Partner for Success.

For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com or contact Vitesse Sales at (800) VITESSE or sales@vitesse.com

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