10 Gb/s Multi-rate Bi-directional High Gain FEC Device With Performance Monitoring



FEATURES:

- Advanced High Gain Forward Error Correction with 15.7% Overhead
- ▶ Greater than 10dB of Raw Coding Gain, 9.5dB of Net Electrical Coding Gain
- ▶ Converts an Input BER of ~7x10⁻³ to an Output BER of 1x10⁻15
- ▶ Bi-directional Transceiver Architecture
- ▶ Regenerator and Transceiver Modes
- ▶ Flags Uncorrectable Codewords
- ▶ Provides Counts of Correctable 0's and 1's that are in Error
- ▶ OCh Overhead Performance Monitoring via Overhead Access Ports
- SONET/SDH Performance Monitoring Operation at OC-48 and OC-192 Rates
- ▶ Optional Scrambler/Descrambler on the OTN Side
- ▶ Error injection capability
- ▶ Differential Encode / Decode
- ▶ SFI-4 Compliant Client Interfaces
- ▶ Bypass Capability for FEC and PM

BENEFITS:

- Sophisticated Forward Error Correction Techniques to Deliver the Highest Performance in Error Detection and Correction
- Transparent Error Detection and Correction for any Client Signal Regardless of Protocol or Rate up to 10.4Gb/s
- Bi-directional Architecture Enables Independent FEC Encode and Decode Operation
- ▶ Regenerator Mode Allows the Device to be used as an FEC Link Regenerator (Decode, then Encode) for Repeater Applications

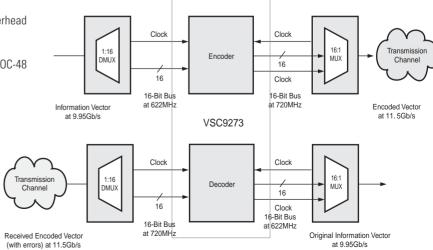
MARKETS:

- ▶ Long Haul Transmission Products
- ▶ Ultra Long Haul Transmission Products

APPLICATIONS:

- ▶ Line Cards
- ▶ Transponders
- ▶ Digital Cross Connects
- ▶ OADM
- ▶ Regenerators

BI-DIRECTIONAL FUNCTIONALITY:



Multi-rate 16-Bit Transceiver with Integrated CMU and CDR

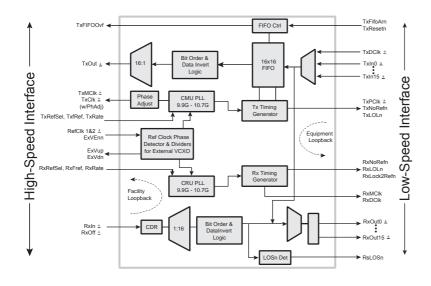
GENERAL DESCRIPTION:



The VSC8373 is a fully integrated 16:1 mux and 1:16 demux transceiver with integrated clock multiplication and clock and data recovery. The VSC8373 supports programmable rates of operation including OC-48, OC-48FEC, OC-192, 10GE and OC-192FEC (G.975/G.709). A full feature set supports the required clocks and modes of operation for 300 pin MSA

transponder module applications. Low speed transmit and receive clocks can be rate programmed to comply with MSA requirements. The user can select between 155MHz to 168MHz or 622MHz to 670MHz reference clocks. Integrated circuitry is provided to facilitate reference clock jitter clean-up using an external VCO and loop filter. The parallel input can either use a selectable data locked loop to provide a clockless interface or a direct clocking mode. A phase programmable, high-speed output clock (with enable/disable) is provided for re-timing and RZ applications. Equipment (parallel-to-parallel), facility (serial-to-serial) and split (simultaneous) loopback modes are supported. Single 3.3V supply operation is supported with programmable power/feature configurations. The VSC8373 is packaged in a compact 17 x 17 mm ball grid array package and operates from 0 to 90°C case temperature.

VSC8373 BLOCK DIAGRAM:



SPECIFICATIONS:

- ▶ Multirate OC-48/192/10GE/FEC Support
- ▶ 9.953Gb/s to 10.709Gb/s Continuous Lock-Range
- ▶ Limiting Amp with 10mV Input Sensitivity
- ▶ 500mV Data and Clock Outputs
- ▶ Supply Voltage: +3.3V (Typ) Optional +2.5V / +3.3V
- ▶ Total Power Dissipation: 2.2W (Typ) in Low Power Mode
- ▶ Operating Temperature Range: 0°C to +90°C (Case)

Your Partner for Success.

For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com or contact Vitesse Sales at (800) VITESSE or sales@vitesse.com



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