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Interfacing MCF5307 ColdFire™ to the PCI Bus using V360EPC from V3 Semiconductor

Application Note

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Preliminary Application Note:

Interfacing Motorola's MCF5307 ColdFire™ Processor to the PCI Bus

1. Objective

This application note describes how to interface Motorola's MPC5307 ColdFire™ processor to the PCI bus via V360EPC Enhanced PCI Controller (EPC) from V3 Semiconductor. The V360EPC will act as a PCI Host bridge between the PCI Bus, the MPC5307 processor and the local memory.

Throughout this document, references will be made to the operation of the V360EPC and MPC5307 components. Basic familiarity with these devices is assumed. This is a preliminary application note and V3 reserves the right to change the document without notice.

2. Overview

The V360EPC uses a generic synchronous bus protocol which can also be adapted for the 32 bit MPC5307. The required glue logic for interfacing the V360EPC to MPC5307 is a simple protocol translator. Also, the glue logic generates the addresses for accessing the external memory so that V360EPC can perform master cycles targeting the external local memory. This section will describe the main protocol differences and similarities between the MPC5307 bus and V360EPC bus.

Main Protocol Similarities

- Synchronous buses that generate and sample all signals on the rising edge of the clock ($\overline{AS}$ is not being used for interfacing purpose here).
- $\overline{TA}$ (MPC5307) acts like a $\overline{RDY}$ (EPC) to indicate that data is ready on that clock.
- R/$\overline{W}$ (MPC5307) acts like a R/$\overline{W}$ (EPC) Read/Write indication.
- BWE/BE[3:0] act the same in both devices.
- The functional operation of the address and data buses are the same.

Main Protocol Differences

- MPC5307 uses SIZ1:0 to indicate burst length at the beginning of a cycle. EPC determine burst size with the $\overline{BURST}$ signal.
- Bursts in the MPC5307 protocol are modulo 4 words while both V360EPC and PCI bursts are sequential.
- Bus arbitration on the MPC5307 uses 3 signals ($\overline{BR}$, $\overline{BG}$ and $\overline{BD}$) and not the two

signals used by the V360EPC. The $\overline{BD}$ signal (Bus Drive) is asserted in the same way that $\overline{TIP}$ (Transfer In Progress, which is an optional pin on MPC5307).

Conversion between protocols requires a relatively small and inexpensive programmable logic device. Due to the fact that the SDRAM control signals are not tri-stated while another bus master gains access, and also in order to minimize the glue logic, the internal integrated Synchronous Asynchronous DRAM Controller (SADRAMC) of MPC5307 is used for memory accesses requested from PCI. Furthermore, due to the mismatching burst protocols, only single accesses are supported from PCI for this version of the application note. However, the MPC5307 can issue single or burst PCI request via V360EPC.

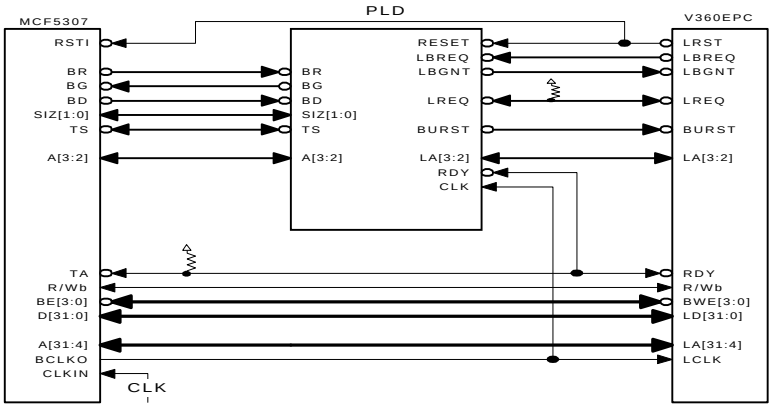
3. Functional Description

In this section, the interface between MPC5307, with external SDRAM modules, and V360EPC are described. Basically, the interface can be categorized in two modes:

- **MPC5307 master mode**, where the processor performs single/burst read/write cycles targeted towards PCI agents, and
- **MPC5307 slave mode**, where a PCI agent will access the local memory via MPC5307's integrated SADRAMC memory controller.

Figure-1 illustrates the interconnection.

Figure 1 - EMIF interface to SDRAM and PCI



MPC5307's input clock (CLKIN) can vary between 16-45MHz. The V360EPC Rev A0 series of Enhanced PCI Controllers from V3 Semiconductor can run up to 50MHz local speeds at 5V and up to 33MHz under 3.3V supply voltages. For this application note, the three test mode pins (pins 134, 135 and 153 as described in Table-4 of the V360EPC data sheet) must be pulled to GND, Vdd and Vdd respectively.

Figure-1 illustrates a "normal" reset scenario initiated from PCI. For a "master" reset case, the HIZ input of the processor will also be connected to LRST. The PLD performs conversion of the control signals to/from PCI as well as providing bus arbitration for the local master. These operations are further explained as follow.

3.1 BUS ARBITRATION

A simple bus arbitration scheme is implemented. Preemption and M-bus arbitration are not considered here to keep the process simple. The BR (bus request), BG (bus grant) and BD (bus drive) signals are used for handshaking with the external arbiter. On the other hand, V360EPC (or V360EPC) only uses two signals, namely, LBREQ and LBGNT. Initially the bus will be granted to the processor which has a higher priority. The processor may de-assert it's BR however the bus can be granted to V360EPC only after BD is de-asserted. V360EPC will own the bus until it's LBREQ request signal is de-asserted.

3.2 ACCESSING THE PCI BUS

MPC5307 can perform both single and burst read/write cycles through V360EPC to access other PCI resources.

The chip select module of MPC5307 provides four byte/byte-write enable (BE/BWE[3:0]) signals. As a result, the PLD will not duplicate generating byte enable signals from SIZ[1:0] and A[1:0].

The burst functionality of MPC5307 is similar to that of M680x0 series. The processor asserts SIZ[1:0] at the beginning of a bus cycle to indicate the transfer length. For a burst cycle, where SIZ[1:0]="11", V360EPC's BURST signal is asserted with TS. A 2-bit counter is loaded also at TS and decremented on every TA. When the count is about to expire, BURST will be de-asserted.

Another burst related issue to be aware of is the fact that the MPC5307 will wrap a burst on a 4-word modulo boundary. That is, if a burst of 4 words begins on an address in which bits A[3:2] are non-zero, the burst address will go from 0xnnnnnnnC back to 0xnnnnnnn0 where nnnnnnn are the upper 28 bits of the address. The approach used in this application note with the V360EPC is to break any burst that could wrap a modulo boundary by de-asserting burst when A[3:2] is "11".

Burst generation is accomplished by generating the signal "LAST" that is true when it is the end of a burst. BURST is then active whenever LAST is inactive. LAST is always asserted for non-burst access (SIZ[1:0] != "11"). When a burst is performed by the MPC5307, it is always 4 long words in length. However, the V360EPC will only see it as a burst of 4 when the burst is aligned so that A[3:2] = "00". Otherwise it will cross a modulo boundary and must be restarted. The PLD guarantees generation of proper values on LA[3:2] address lines of the V360EPC to ensure true operation in case of a non-aligned burst. Table-1 demonstrates the operation in details.

Table 1 Burst Generation

Start Address A3:2		Cycle 0	Cycle 1	Cycle 2	Cycle 3
00	Burst Address Sequence	00	01	10	11
	LAST Sequence	0	0	0	1
01	Burst Address Sequence	01	10	11	00
	LAST Sequence	0	0	1	1
10	Burst Address Sequence	10	11	00	01
	LAST Sequence	0	1	0	1
11	Burst Address Sequence	11	00	01	10
	LAST Sequence	1	0	0	1

The $\overline{\text{LREQ}}$ signal can be generated from either $\overline{\text{TIP}}$ or $\overline{\text{BD}}$ signals. Furthermore, V360EPC's R/$\overline{\text{W}}$ and $\overline{\text{RDY}}$ signals can be directly connected to the processors $\overline{\text{TA}}$ and R/$\overline{\text{W}}$ signals.

3.3 PCI ACCESS TO THE LOCAL BUS

The integrated SADRAMC memory controller of MPC5307 will be used to access synchronous or asynchronous memory modules on the local bus by other PCI agents via V360EPC. However, due to the incompatible burst protocols, only single accesses from PCI are supported here. To perform burst cycles, it will be necessary to provide external memory controlling logic and bypass the internal SADRAMC.

4. Conclusion

In this preliminary application note, the interface between MPC5307's and V360EPC were briefly described. V360EPC provides an efficient and cost-effective solution for interfacing MPC5307 ColdFire processor to the PCI bus.

For availability, samples and pricing please contact "v3info@vcubed.com".

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