

Description

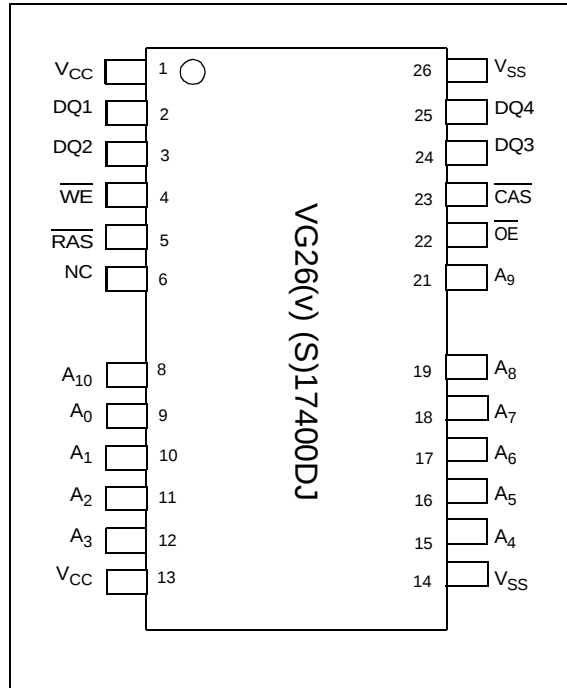
The device is CMOS Dynamic RAM organized as 4,194,304 words x 4 bits. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. A new refresh feature called " self-refresh " is supported and very slow CBR cycles are being performed. It is packaged in JEDEC standard 26/24 - pin plastic SOJ or TSOP (II).

Features

- Single 5V ($\pm 10\%$) or 3.3V ($\pm 10\%$) only power supply
- High speed t_{RAC} access time : 50/60 ns
- Low power dissipation
 - Active mode : 5V version 605/550 mW (Max.)
3.3V version 396/360 mW (Max.)
 - Standby mode : 5V version 1.375 mW (Max.)
3.3V version 0.54 mW (Max.)
- Fast Page Mode access
- I/O level : TTL compatible ($V_{CC} = 5V$)
LVTTL compatible ($V_{CC} = 3.3V$)
- 2048 refresh cycles in 32 ms (Std) or 128ms (S - version)
- 4 refresh mode :
 - $\overline{RAS}$ only refresh
 - $\overline{CAS}$ -before- $\overline{RAS}$ refresh
 - Hidden refresh
 - Self - refresh (S - version)

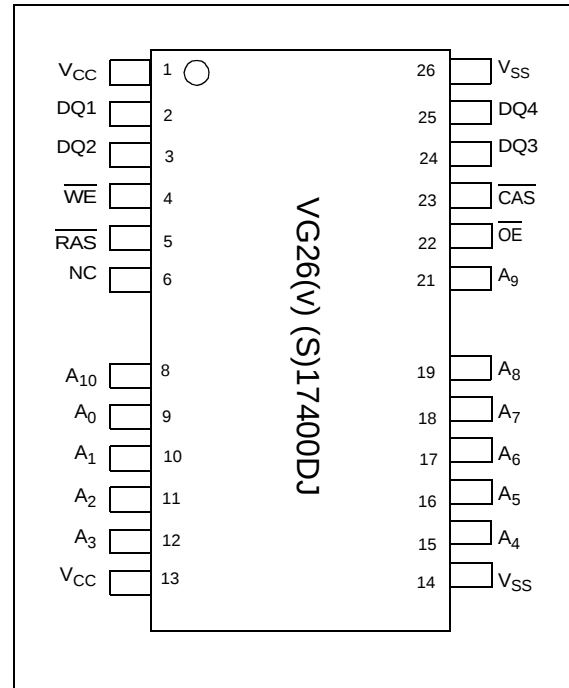
Pin configuration

26/24 - PIN 300mil Plastic SOP



Pin configuration

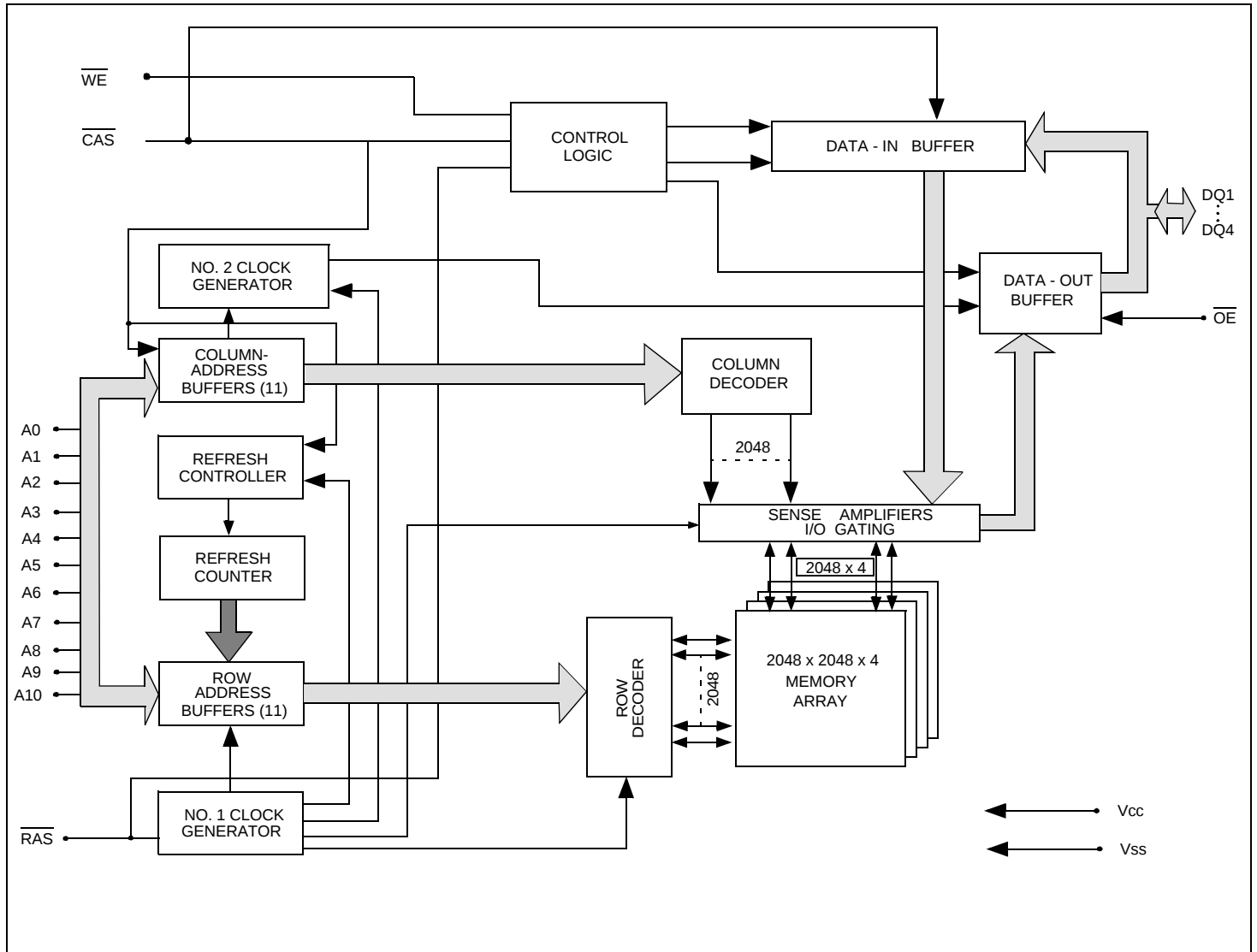
26/24 - PIN 300mil Plastic TSOP (II)



Pin Description

Pin Name	Function
A0 - A10	Address inputs - Row address A0 - A10 - Column address A0 - A10 - Refresh address A0 - A10
DQ1 ~ DQ4	Data - in/data - out
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
OE	Output enable
V _{CC}	Power (+ 5V or + 3.3V)
V _{SS}	Ground

Block Diagram



Truth Table

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQs	Notes
						ROW	COL		
STANDBY		H	H → X	X	X	X	X	High - Z	
READ		L	L	H	L	ROW	COL	Data - Out	
WRITE : (EARLY WRITE)		L	L	L	X	ROW	COL	Data - In	
READ WRITE		L	L	H → L	L → H	ROW	COL	Data - Out, Data - In	
PAGE - MODE READ	1st Cycle	L	H → L	H	L	ROW	COL	Data - Out	
	2st Cycle	L	H → L	H	L	n/a	COL	Data - Out	
PAGE - MODE WRITE	1st Cycle	L	H → L	L	X	ROW	COL	Data - In	
	2st Cycle	L	H → L	L	X	n/a	COL	Data - In	
PAGE - MODE READ - WRITE	1st Cycle	L	H → L	H → L	L → H	ROW	COL	Data - Out, Data - In	
	2st Cycle	L	H → L	H → L	L → H	n/a	COL	Data - Out, Data - In	
HIDDEN REFRESH	READ	L → H → L	L	H	L	ROW	COL	Data - Out	
	WRITE	L → H → L	L	L	X	ROW	COL	Data - In	1
RAS - ONLY REFRESH		L	H	X	X	ROW	n/a	High - Z	
CBR REFRESH		H → L	L	H	X	X	X	High - Z	

Notes : 1. EARLY WRITE only.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss 5V 3.3V	V_T	-1.0 to + 7.0 -0.5 to + 4.6	V
Supply voltage relative to Vss 5V 3.3V	V_{CC}	-1.0 to + 7.0 -0.5 to + 4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to + 70	°C
Storage temperature	T_{STG}	-55 to + 125	°C

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5 Volt Version			3.3 Volt Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.4	-	$V_{CC} + 1.0$	2.0	-	$V_{CC} + 0.3$	V
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

Ta = 25°C, V_{CC} = 5V±10% or 3.3V±10 %, f = 1MHz

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	-	5	pF	1
Input capacitance (RAS, CAS, OE, WE)	C_{I2}	-	7	pF	1
Output capacitance (Data - in, Data - out)	$C_{I/O}$	-	7	pF	1,2

Note : 1. Capacitance measured with effective capacitance measuring method.
2. CAS = V_{IH} to disable Dout.

DC Characteristics; 5 - Volt verion

(T_a = 0 to 70°C, V_{CC} = + 5V±10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I _{CC1}	RAS cycling CAS cycling t _{RC} = min.	-	110	-	100	mA	1, 2
Standby Current	Low power S - version	I _{CC2}	TTL interface RAS, CAS = V _{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface RAS, CAS ≥ V _{CC} - 0.2V Dout = high - Z	-	0.25	-	0.25	mA	
	Standard power version		TTL interface RAS, CAS = V _{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface RAS, CAS ≥ V _{CC} - 0.2V Dout = high - Z	-	1	-	1	mA	
RAS - only refresh current		I _{CC3}	RAS cycling, CAS = V _{IH} t _{RC} = min.	-	110	-	100	mA	1, 2
Fast page mode current		I _{CC4}	t _{PC} = min.	-	80	-	70	mA	1,3
CAS - before - RAS refresh current		I _{CC5}	t _{RC} = min. RAS, CAS cycling	-	110	-	100	mA	1, 2
Self - refresh currant (S - Version)		I _{CC8}	t _{RASS} ≥ 100μS	-	350	-	350	μA	
CAS - before - RAS long refresh current (S - Version)		I _{CC9}	Standby : V _{CC} - 0.2V ≤ RAS CAS before RAS refresh : 2048 cycles/128ms RAS, RAS : 0V ≤ V _{IL} ≤ 0.2V V _{CC} - 0.2V ≤ V _{IH} ≤ V _{IH} (Max) Dout = high - Z, t _{RAS} ≤ 300ns	-	500	-	500	μA	

DC Characteristics ; 5 - Volt Version (cont.)

($T_a = 0$ to 70°C , $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I _{LI}	0V ≤ Vin ≤ V _{CC} + 0.5V	-5	5	-5	5	μA	
Output leakage current	I _{LO}	0V ≤ Vout ≤ V _{CC} + 0.5V Dout = Disable	-5	5	-5	5	μA	
Output high voltage	V _{OH}	I _{OH} = -5mA	2.4	-	2.4	-	V	
Output low voltage	V _{OL}	I _{OL} = + 4.2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. For I_{CC4} , address can be changed once or less within one Fast page mode cycle time.

DC Characteristics ; 3.3 - Volt Verion

(T_a = 0 to 70°C, V_{CC} = + 3.3V±10%, V_{SS} = 0V)

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I _{CC1}	$\overline{\text{RAS}}$ cycling CAS cycling t _{RC} = min.	-	110	-	100	mA	1, 2
Standby Current	Low power S - version	I _{CC2}	LVTTL interface RAS, $\overline{\text{CAS}} = V_{IH}$ Dout = high - Z	-	0.5	-	0.5	mA	
			CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2V$ Dout = high - Z	-	0.25	-	0.25	mA	
	Standard power version		LVTTL interface RAS, $\overline{\text{CAS}} = V_{IH}$ Dout = high - Z	-	2	-	2	mA	
			CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2V$ Dout = high - Z	-	0.5	-	0.5	mA	
RAS - only refresh current		I _{CC3}	RAS cycling, $\overline{\text{CAS}} = V_{IH}$ t _{RC} = min.	-	110	-	100	mA	1, 2
Fast page mode current		I _{CC4}	t _{PC} = min.	-	80	-	70	mA	1,3
CAS - before - RAS refresh current		I _{CC5}	t _{RC} = min. RAS, CAS cycling	-	110	-	100	mA	1, 2
Self - refresh currant (S - Version)		I _{CC8}	t _{RASS} ≥ 100μS	-	250	-	250	μA	
CAS - before - RAS long refresh current (S - Version)		I _{CC9}	Standby : $V_{CC} - 0.2V \leq \overline{\text{RAS}}$ CAS before RAS refresh : 2048 cycles/128ms $\overline{\text{RAS}}, \text{RAS} : 0V \leq V_{IL} \leq 0.2V$ $V_{CC} - 0.2V \leq V_{IH} \leq V_{IH}$ (Max) Dout = high - Z, t _{RAS} ≤ 300ns	-	300	-	300	μA	

DC Characteristics ; 3.3 - Volt Version (cont.)

($T_a = 0$ to 70°C , $V_{CC} = +3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I _{LI}	0V ≤ Vin ≤ V _{CC} + 0.3V	-5	5	-5	5	μA	
Output leakage current	I _{LO}	0V ≤ Vout ≤ V _{CC} + 0.3V Dout = Disable	-5	5	-5	5	μA	
Output high voltage	V _{OH}	I _{OH} = -2mA	2.4	-	2.4	-	V	
Output low voltage	V _{OL}	I _{OL} = + 2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. For I_{CC4} , address can be changed once or less within one Fast page mode cycle time.

AC Characteristics

(Ta = 0 to + 70°C, V_{CC} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V) * 1, * 2, * 3, * 4

Test conditions

- Output load : two TTL Loads and 100pF(V_{CC} = 5.0V ±10%)
one TTL Load and 100pF(V_{CC} = 3.3V ±10%)
- Input timing reference levels :
V_{IH} = 2.4V, V_{IL} = 0.8V (V_{CC} = 5.0V ±10%); V_{IH} = 2.0V, V_{IL} = 0.8V (V_{CC} = 3.3V ±10%)
- Output timing reference levels :
V_{OH} = 2.0V, V_{OL} = 0.8V (V_{CC} = 5V ±10%, 3.3V ±10%)

Read, Write, Read - Modify - Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90	-	110	-	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	30	-	40	-	ns	
CAS precharge time in normal mode	t _{CPN}	10	-	10	-	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10000	60	10000	ns	5
CAS pulse width	t _{CAS}	12	10000	15	10000	ns	6
Row address setup time	t _{ASR}	0	-	0	-	ns	
Row address hold time	t _{RAH}	8	-	10	-	ns	
Column address setup time	t _{ASC}	0	-	0	-	ns	7
Column address hold time	t _{CAH}	8	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	12	37	14	45	ns	8
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	10	25	12	30	ns	9
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25	-	30	-	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13	-	15	-	ns	
CAS hold time	t _{CSH}	50	-	60	-	ns	
CAS to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	-	5	-	ns	10
OE to Din delay time	t _{OED}	12	-	15	-	ns	
Transition time (rise and fall)	t _T	1	50	1	50	ns	11
Refresh period	t _{REF}	-	32	-	32	ms	
Refresh period (S - Version)	t _{REF}	-	128	-	128	ms	
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0	-	0	-	ns	
CAS delay time from Din	t _{DZC}	0	-	0	-	ns	
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	-	50	-	60	ns	12
Access time from $\overline{\text{CAS}}$	t_{CAC}	-	13	-	15	ns	13,14
Access time from column address	t_{AA}	-	25	-	30	ns	14,15
Access time from $\overline{\text{OE}}$	t_{OEA}	-	13	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	7
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	-	0	-	ns	10,16
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	-	0	-	ns	16
Output buffer turn-off time	t_{OFF}	0	13	0	15	ns	17
Output buffer turn-off time from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	17

Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	-	0	-	ns	7,18
Write command hold time	t _{WCH}	8	-	10	-	ns	
Write command pulse width	t _{WP}	8	-	10	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13	-	15	-	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	8	-	10	-	ns	
Data-in setup time	t _{DS}	0	-	0	-	ns	19
Data-in hold time	t _{DH}	8	-	10	-	ns	19

Read - Modify - Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Read - modify - write cycle time	t _{RWC}	125	-	150	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	65	-	80	-	ns	18
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	30	-	35	-	ns	18
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	40	-	50	-	ns	18
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OEH}	8	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
$\overline{\text{CAS}}$ setup time (CBR refresh)	t_{CSR}	10	-	10	-	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh)	t_{CHR}	10	-	10	-	ns	10
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	5	-	5	-	ns	7
$\overline{\text{RAS}}$ pulse width (self refresh)	t_{RASS}	100	-	100	-	μs	
$\overline{\text{RAS}}$ precharge time (self refresh)	t_{RPS}	90	-	110	-	ns	
$\overline{\text{CAS}}$ hold time (CBR self refresh)	t_{CHS}	-50	-	-50	-	ns	
$\overline{\text{WE}}$ setup time	t_{WSR}	0	-	0	-	ns	
$\overline{\text{WE}}$ hold time	t_{WHR}	10	-	10	-	ns	

Fast Page Mode Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	35	-	40	-	ns	
Fast page mode $\overline{\text{CAS}}$ Precharge time	t _{CP}	10	-	10	-	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	50	10 ⁵	60	10 ⁵	ns	20
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	-	30	-	35	ns	10,14
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	30	-	35	-	ns	

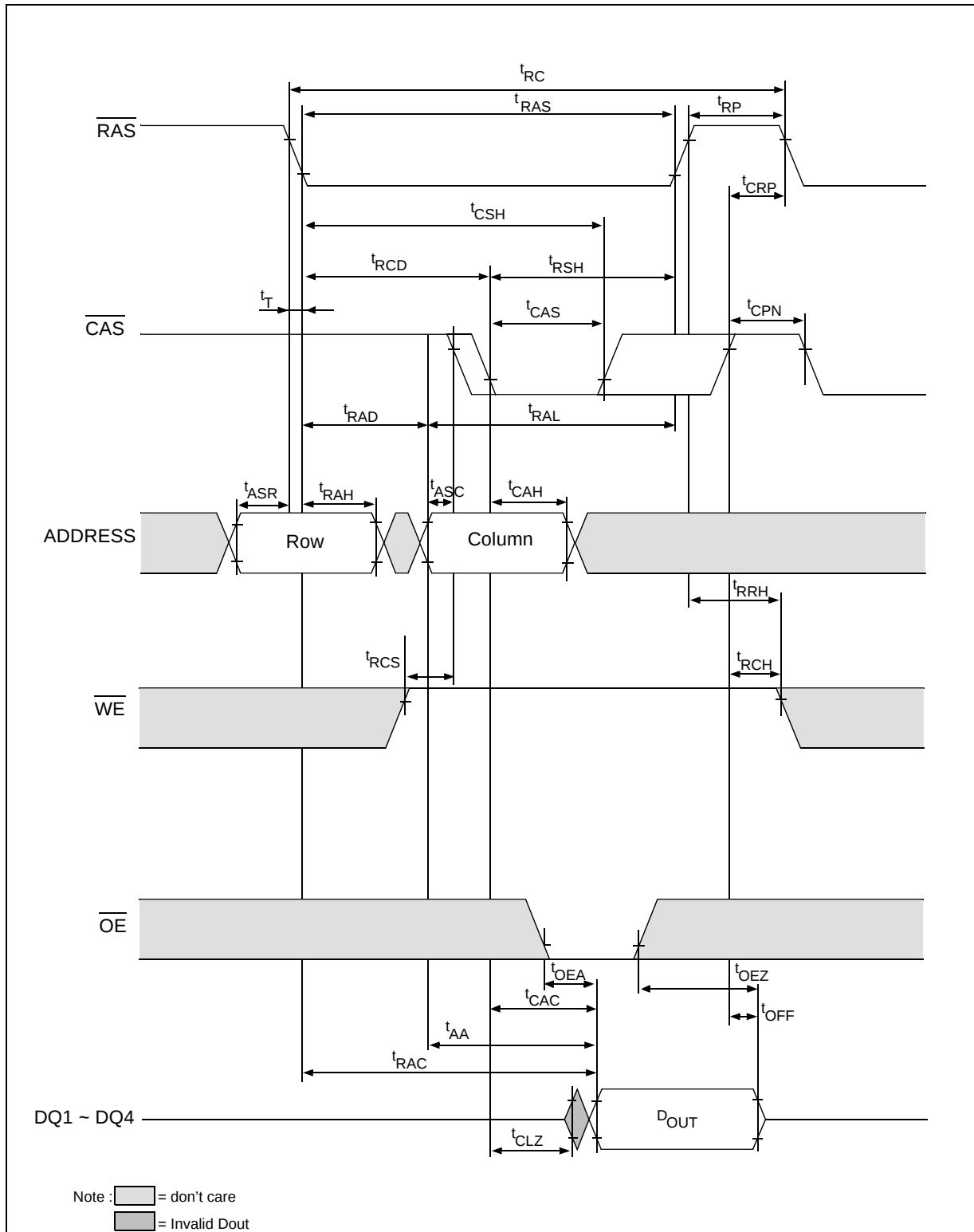
Fast Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode read - modify - write cycle CAS precharge to WE delay time	t _{CPW}	45	-	55	-	ns	11
Fast page mode read - modify - write cycle time	t _{PRWC}	70	-	80	-	ns	

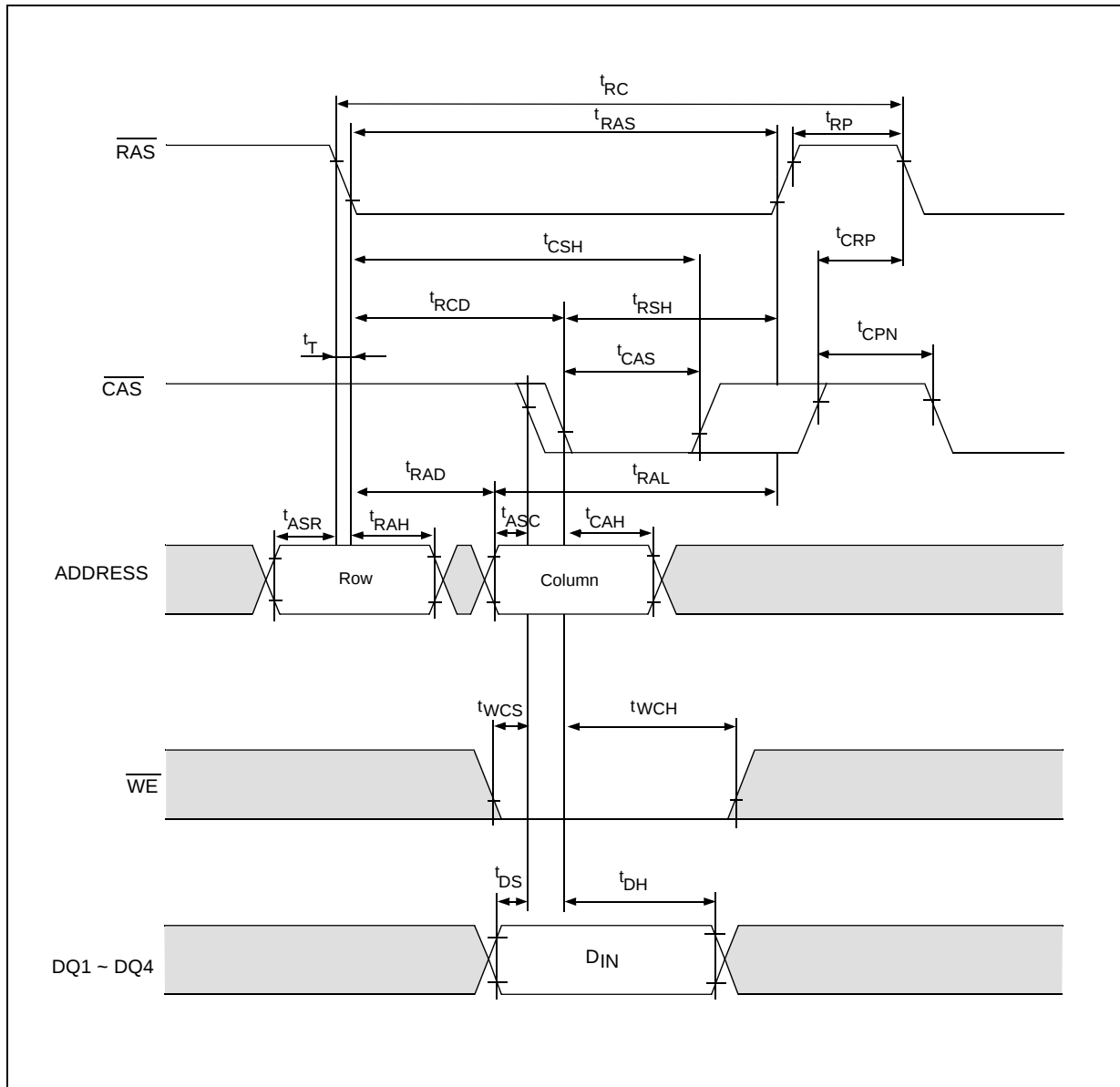
Notes :

1. AC measurements assume $t_T = 5\text{ns}$.
2. An initial pause of $100\ \mu\text{s}$ is required after power up, and it followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
4. All the V_{CC} and V_{SS} pins shall be supplied with the same voltage.
5. $t_{\text{RAS}}(\text{min}) = t_{\text{RWD}}(\text{min}) + t_{\text{RWL}}(\text{min}) + t_T$ in read - modify-write cycle.
6. $t_{\text{CAS}}(\text{min}) = t_{\text{CWD}}(\text{min}) + t_{\text{CWL}}(\text{min}) + t_T$ in read - modify-write cycle.
7. $t_{\text{ASC}}(\text{min})$, $t_{\text{RCS}}(\text{min})$, $t_{\text{WCS}}(\text{min})$ and t_{RPC} are determined by the falling edge of $\overline{\text{CAS}}$.
8. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, and $t_{\text{RAC}}(\text{max})$ can be met with the $t_{\text{RCD}}(\text{max})$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{CAC} if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit.
9. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, and $t_{\text{RAC}}(\text{max})$ can be met with the $t_{\text{RAD}}(\text{max})$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{AA} if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit.
10. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the rising edge of $\overline{\text{CAS}}$.
11. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing or input signals. Therefore, transition time is measured between V_{IH} and V_{IL} .
12. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
13. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
14. Access time is determined by the maximum among t_{AA} , t_{CAC} , t_{CPA} .
15. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition (high impedance).
18. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain open circuit (high impedance) throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
19. These parameters are referenced to $\overline{\text{CAS}}$ in an early write cycle and to $\overline{\text{WE}}$ edge in a delayed write or a read-modify-write cycle.
20. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in Fast page mode cycles.

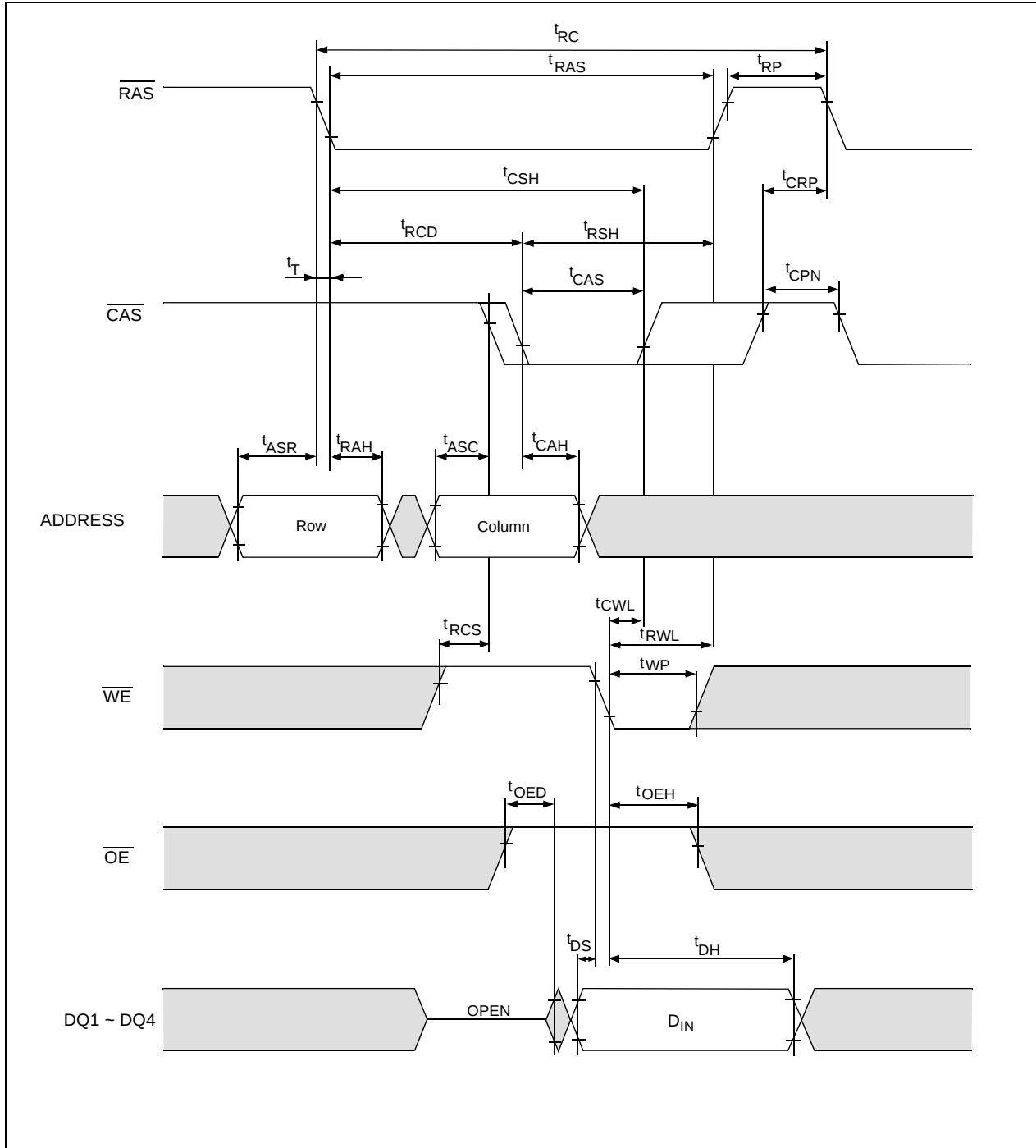
Timing Waveforms • Read Cycle



•Early Write Cycle



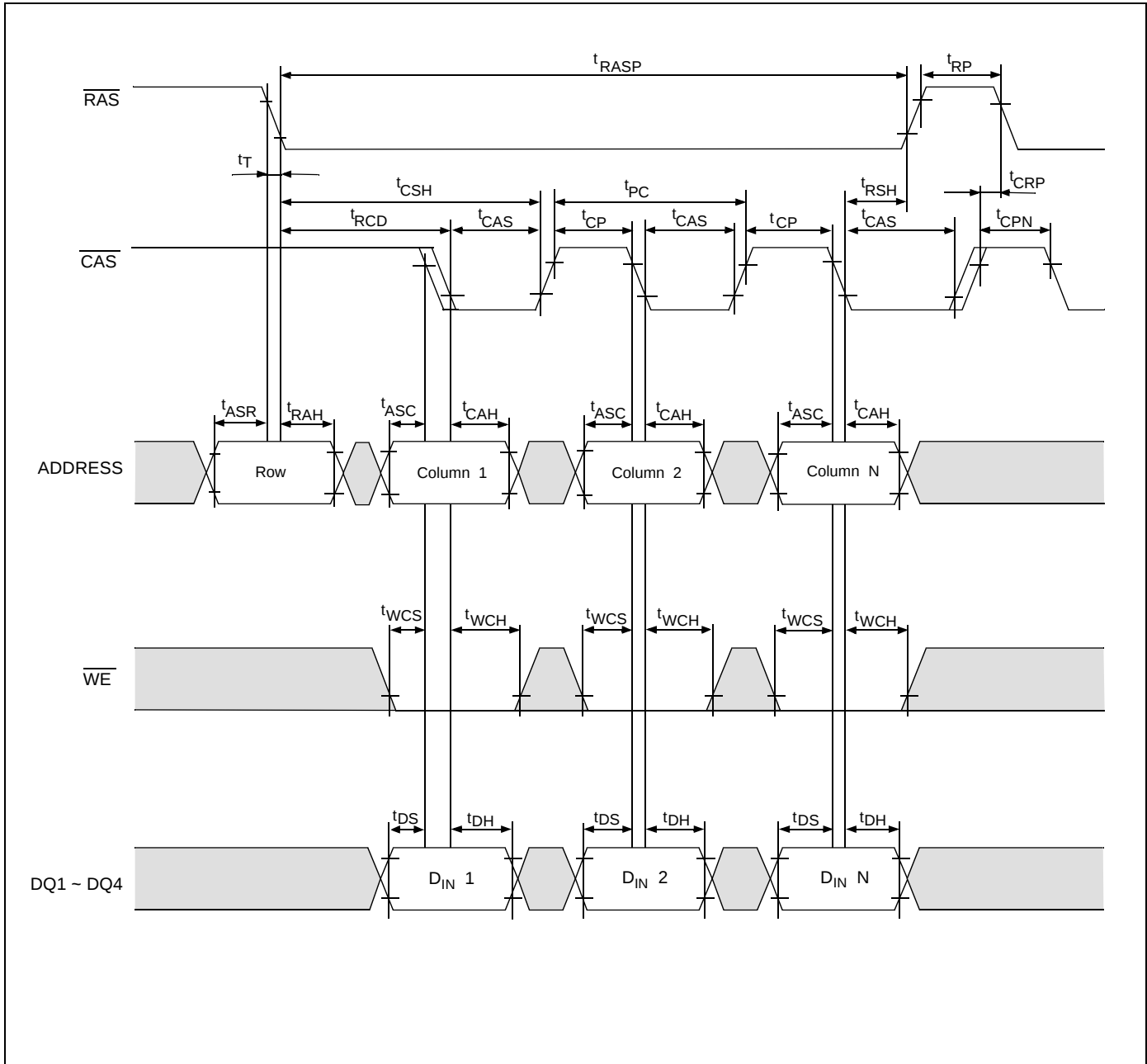
• Delayed Write Cycle



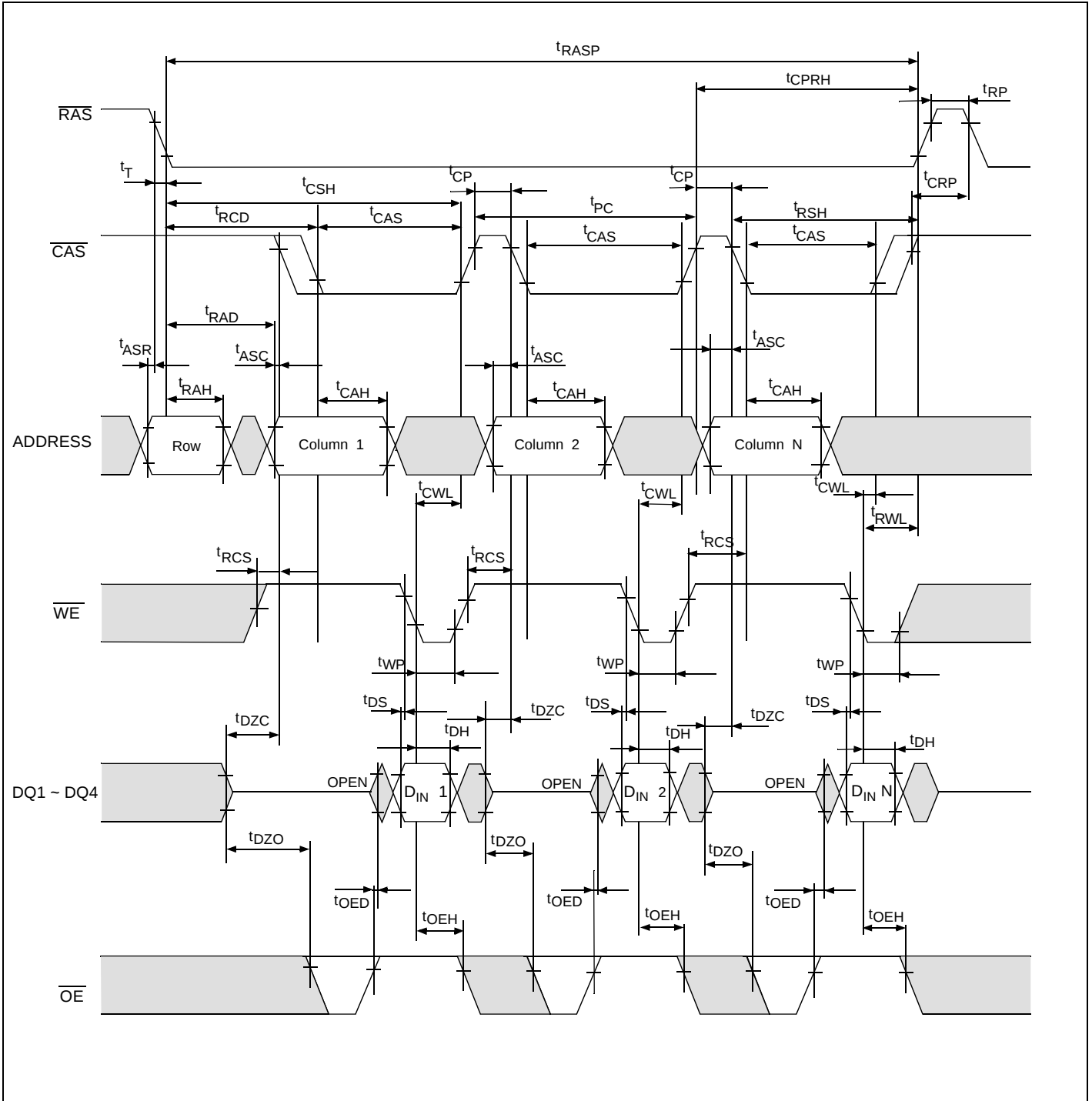
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• Fast Page Mode Early Write Cycle



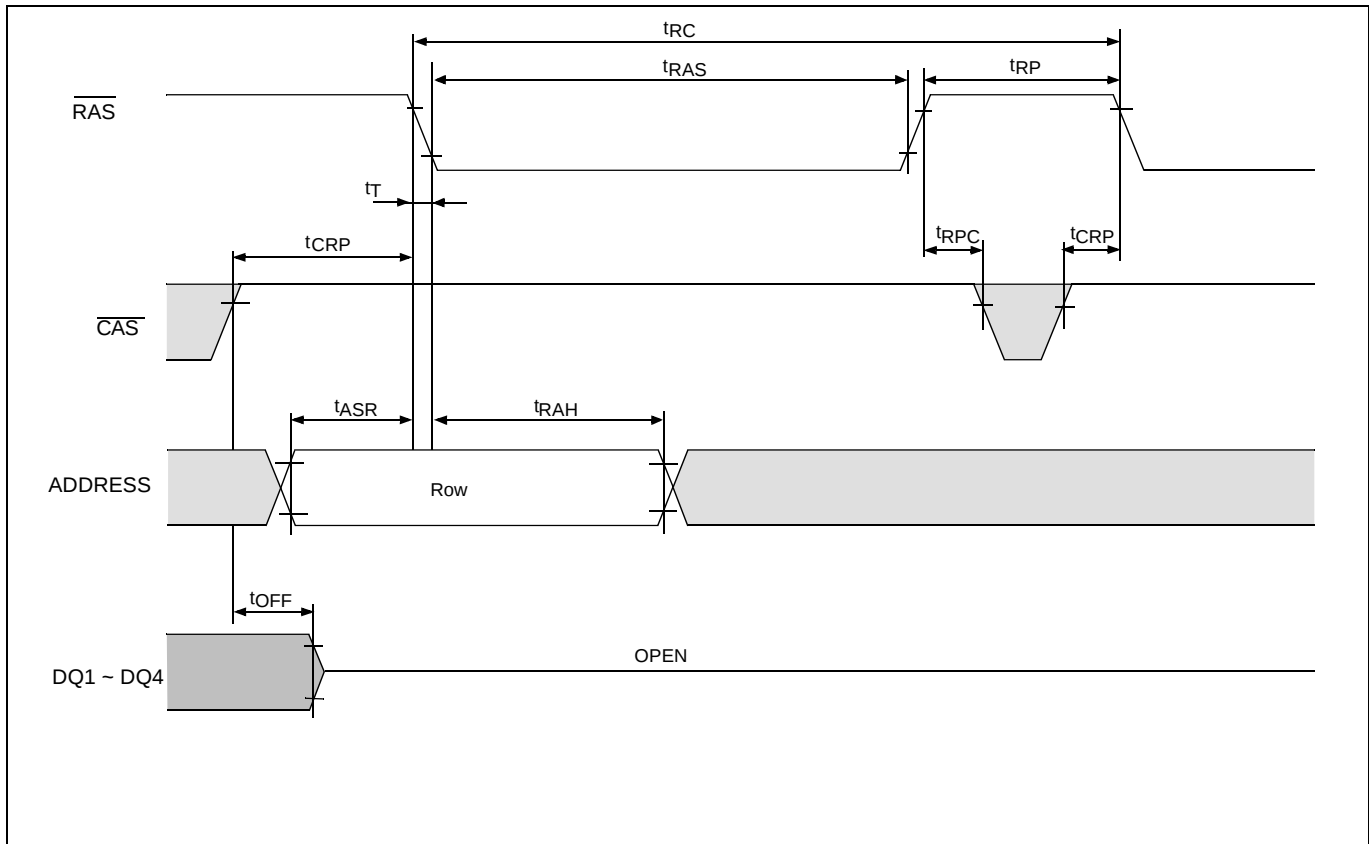
• Fast Page Mode Delayed Write Cycle



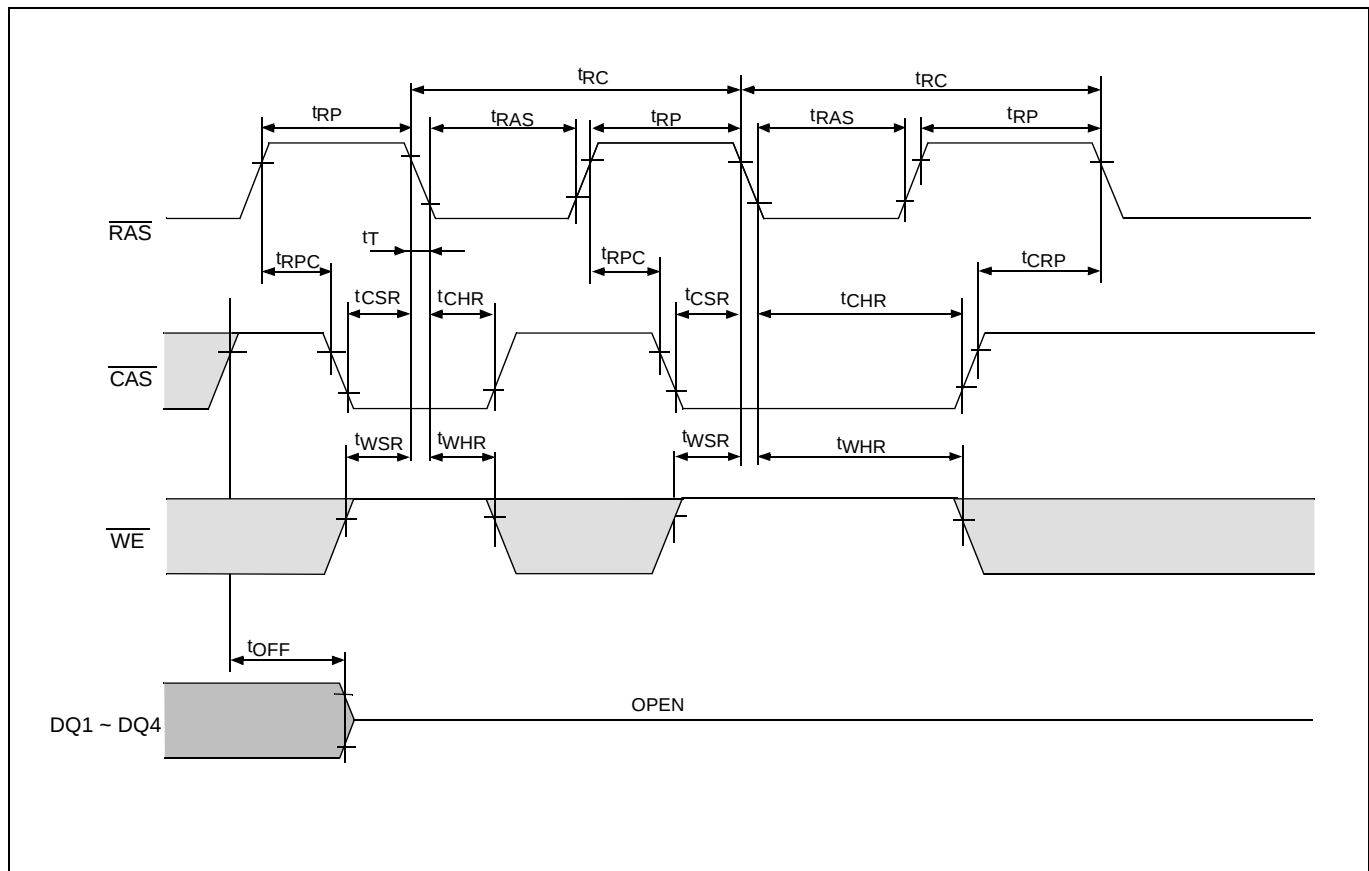
The diagram illustrates the timing relationships for a memory device. The signals shown are RAS, CAS, ADDRESS, WE, DQ1 ~ DQ4, and OE. The timing parameters are defined as follows:

- t_{RAS} : RAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{CP} : CAS to RAS delay
- t_{PRWC} : Precharge to RAS delay
- t_{CPRH} : Precharge to RAS delay
- t_{RP} : RAS pulse width
- t_{CRP} : RAS to CAS delay
- t_{RAD} : RAS to Address delay
- t_{ASC} : Address to CAS delay
- t_{CAH} : Address to CAS delay
- t_{RAH} : RAS to Address delay
- t_{ASR} : Address to RAS delay
- t_{RWD} : RAS to Write Data delay
- t_{AWD} : Address to Write Data delay
- t_{CWD} : CAS to Write Data delay
- t_{RCS} : RAS to Column Select delay
- t_{WP} : Write Pulse width
- t_{DZC} : Data Z-bus delay
- t_{DS} : Data Setup delay
- t_{DH} : Data Hold delay
- t_{DZO} : Data Z-bus delay
- t_{OED} : Output Enable delay
- t_{CPA} : Column Pulse width
- t_{OEH} : Output Enable delay
- t_{OEA} : Output Enable delay
- t_{AA} : Address to Address delay
- t_{CAC} : Address to Address delay
- t_{CLZ} : Address to Address delay
- t_{OEZ} : Output Enable delay
- t_{DOUT1} : Data Output 1 delay
- t_{DOUT2} : Data Output 2 delay
- t_{DOUTN} : Data Output N delay

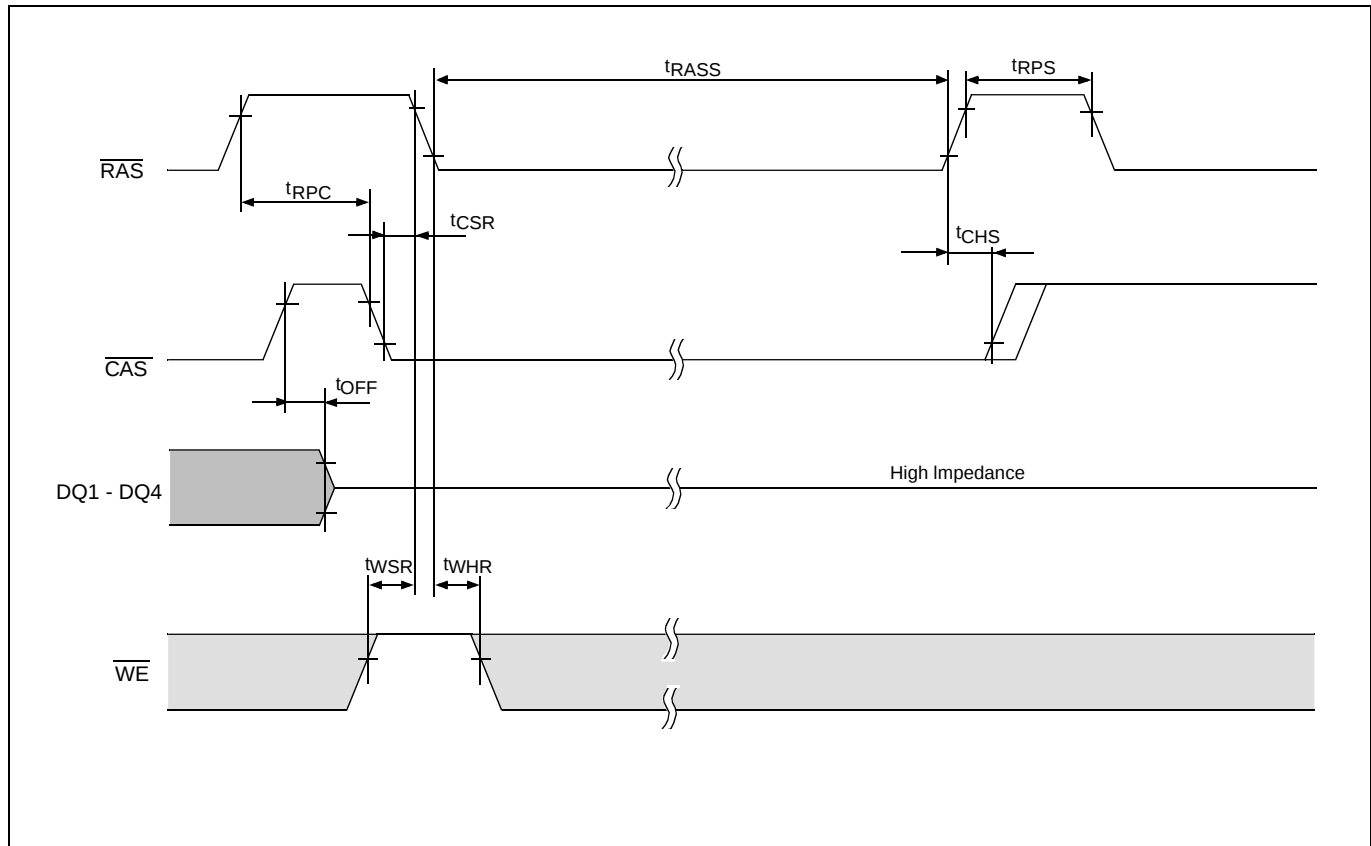
$\overline{\text{RAS}}$ - Only Refresh Cycle



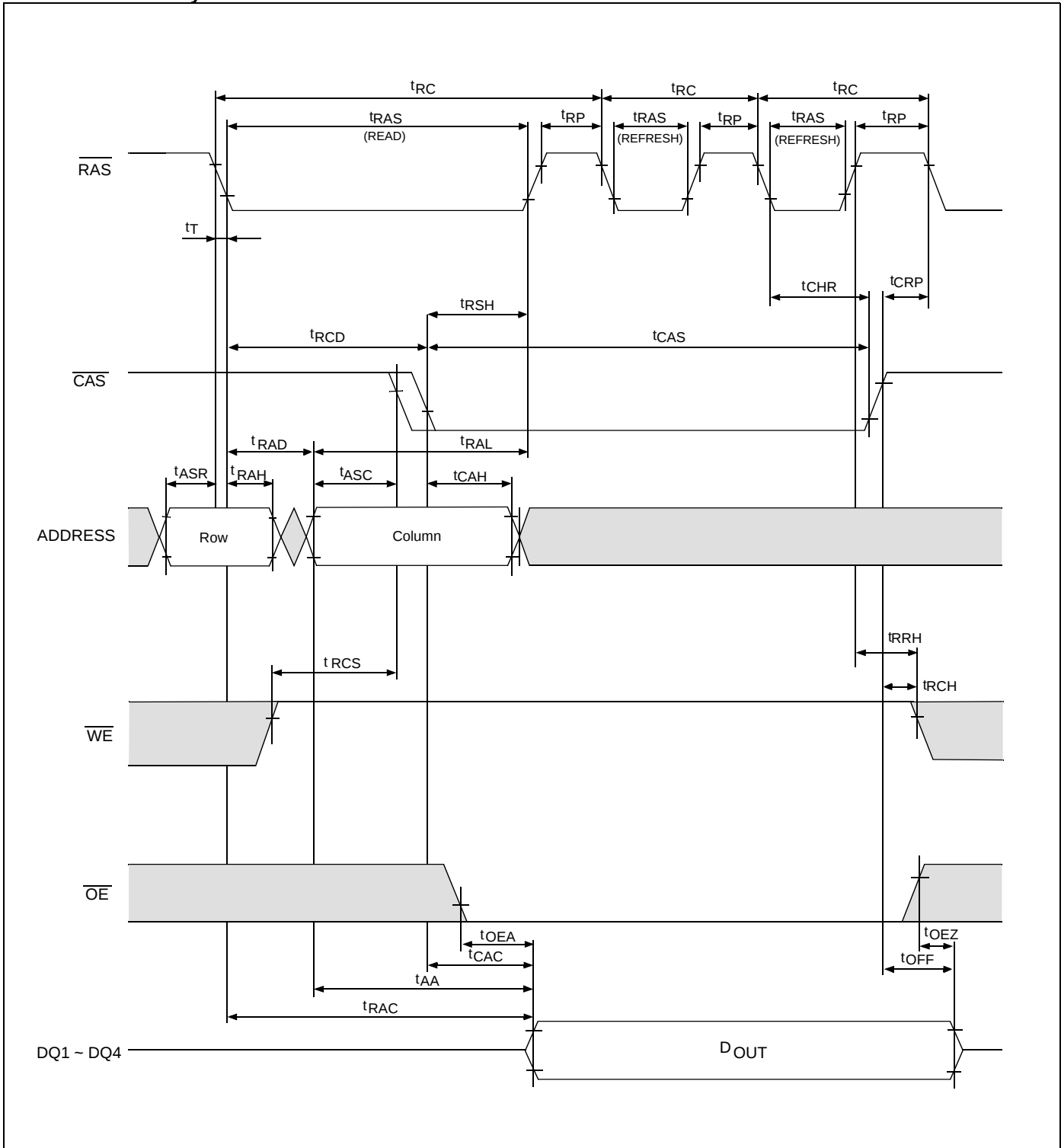
$\overline{\text{CAS}}$ - Before - $\overline{\text{RAS}}$ Refresh Cycle



CBR Self - Refresh Cycle



• Hidden Refresh Cycle



Ordering information

Part Number	Access Time	Package
VG26 (V) (S) 17400DJ - 5	50 ns	300mil 26/24 - Pin
VG26 (V) (S) 17400DJ - 6	60 ns	Plastic SOJ

VG26 (V) (S) 17400DJ - 5

- VG → • VIS Memory Product
- 26 → • Technology
- V → • 3.3V version
- S → • Self refresh
- 17400 → • Device Type and Configuration
- D → • Revision
- J → • Package Type (J : SOJ , T : TSOJ II)
- 5 → • Speed (5 : 50 ns, 6 : 60 ns)

Packaging information

- 300 mil, 26/24-Pin Plastic SOJ

