V96SSC Rev B1

HIGH-INTEGRATION SYSTEM CONTROLLER

FOR i960®Jx/Sx and PowerPC™401Gx PROCESSORS

Block diagram inputs (i960 Processor Interface):
A[31,26:16]
AD[15:0]
BE[1:0]
ADS
BLAST
W/R
BTYPE[1:0]
HLDA
HOLD
INT
RSTOUT
RESET
CLK2

i960 Processor Interface — BUS Watch

DRAM Control outputs:
MA[11:0]
RAS[1:0]
CAS[3:0]
WE
OE[1:0]
LE

I/O MUX: I/O[15:0]

Two Channel DMA:
DREQ0
DACK0
DREQ1
DACK1

System Heartbeat/Watchdog Timers

32-bit Timers (2)

Serial Comm. Unit

Chip Select Strobe Logic
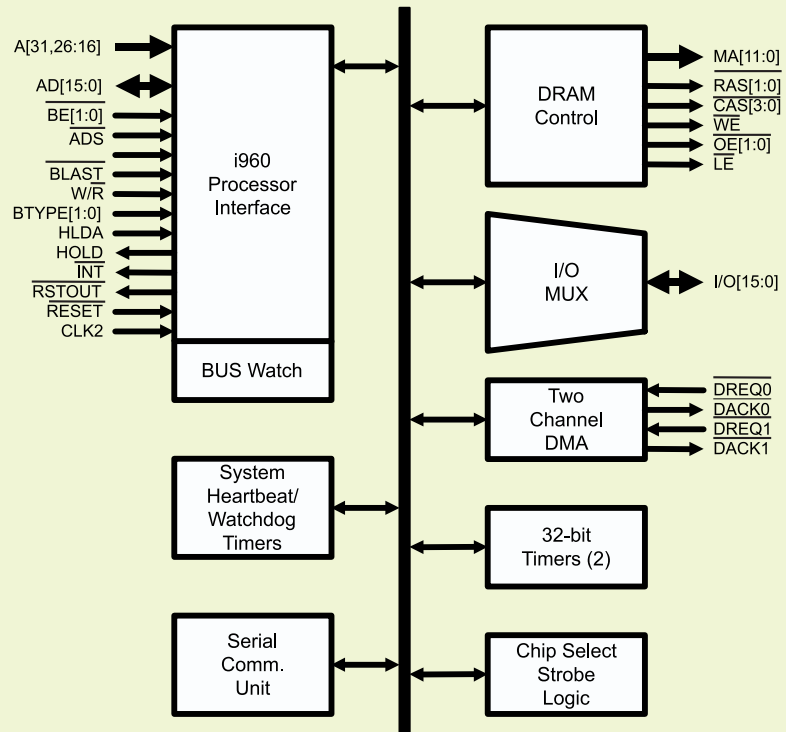
BLOCK DIAGRAM

- Glueless interface between Intel's i960Jx and i960Sx series processors, DRAM arrays, and peripheral devices (Fast time-to-market)

- High-performance burst DRAM controller with DRAM page cache management

- Support for 32-bit bus masters and extended burst transactions

- Two-channel fly-by DMA controller

- Synchronous/asynchronous serial communications unit

- Programmable chip select/peripheral device strobe generation

- Industrial Temperature Grade Design -40°C to +85°C

- Support for boot PROM devices

- System heartbeat and watchdog timers

- Two 32-bit general purpose timers with pulse width modulation capability

- 16 general purpose I/Os

- Interrupt control unit

- Local bus speeds up to 33MHz

- Available in a low-cost 100-pin EIAJ plastic quad flat pack (PQFP)

- Also supports 3.3Volt DRAM modules

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TYPICAL APPLICATIONS

HIGH-PERFORMANCE NETWORK ADAPTER CARD
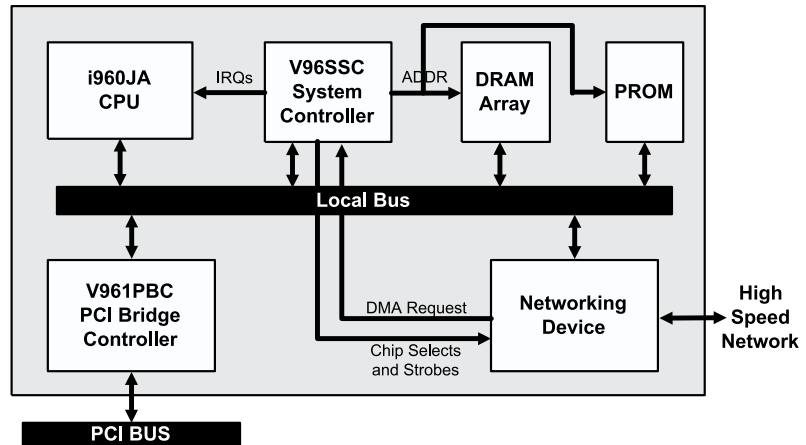
The V96SSC High-Integration System Controller simplifies the design of systems based on Intel's i960Jx and i960Sx microprocessors. By using the V96SSC, system designers can replace many lower integration support components with a single, high-integration device; saving design time, board area, and manufacturing cost.

The integrated DRAM Controller directly connects the i960Sx or i960Jx processor to DRAM arrays, from 128KByte to 128MByte. The fully programmable DRAM controller allows the use of a wide range of DRAM speeds and configurations. Burst accesses are supported up to 64 bytes in length, allowing for the use of high-performance, bus-mastering peripherals.

The two channel fly-by DMA Controller makes it easy to use less expensive, non-mastering peripherals in your system. To further aid in connecting the i960 processor, the V96SSC's I/O Controller performs address decoding and chip-select/strobe generation. In addition, the I/O lines can be used as simple I/O ports on a bit-by-bit basis. The Serial Communications Unit connects to either RS-232 or synchronous serial devices.

The two general purpose 32-bit timers can be individually configured as a pulse width modulator, or they can be used in other modes such as retriggering or one-shot. The bus watch timer prevents system hangs during accesses to unpopulated memory.

Interrupts for a real time OS can be easily generated by the system heartbeat timer. A watchdog timer is also provided for graceful recovery from catastrophic program failures.

Interrupt requests for all on-chip peripherals are managed by the Interrupt Control Unit. Additionally, off-chip interrupts can be routed to the Interrupt Control Unit via the I/O multiplexer.

The V96SSC is packaged in a low-cost 100 pin EIAJ Plastic Quad Flat Pack (PQFP), and is available in 33MHz speed grade.

ABOUT V3 SEMICONDUCTOR

V3 Semiconductor has been providing embedded systems designers with innovative products since 1987. V3 products are supported throughout North America, Europe, the Middle East and the Far East by a network of distributors and manufacturers' representatives.

For more information on the V96SSC, or our other i960® and PowerPC™ processors support components, please contact:

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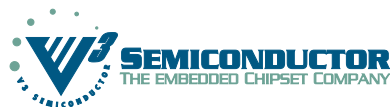
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