VLSI Technology

VWS23112 VEGA™ VMAX™

Combining Power and DECT Flexibility

OVERVIEW

Wireless Technology is revolutionizing the world of communications, and, as a leader in the fast-growing wireless market, VLSI is enabling a new generation of innovative wireless equipment with the Vega™ family of leading-edge DECT processors.

The VWS23112 Vega™ VMax™ DECT processor, the second member of the Vega family, is an advanced digital processing subsystem, optimized for demanding applications such as DECT Wireless Local Loop (WLL) systems and PBXs. Building on VLSI Technology's DECT integration expertise, Vega VMax integrates a powerful DECT burst-mode logic with a 32-bit ARM RISC microcontroller, dedicated high-speed data support, and versatile interfaces, providing the power and flexibility needed to deliver a new generation of telecommunications services over DECT.

This Product Overview outlines the functionality of the Vega VMax device. A data sheet is available which provides more detailed information.

FEATURES

- Single-chip System-Level-Silicon™ DECT baseband processor for base stations, repeaters and multi-user terminals
- ARM7TDMI™ "Thumb™" RISC microprocessor
- Integrated Reed-Solomon coding/decoding and error correction hardware for LU7 64 kbps data support on all channels
- 2 Mbps multi-channel PCM/ADPCM interface: 2Mbps PCM/ADPCM, 1.5 Mbps PCM/ADPCM, IOM-2 TE, IOM-2 NT modes
- Four-channel G.721 32 kbps ADPCM transcoder
- DECT core supports half-, full- and double-slot
- Core handles E/U-MUX and T-MUX for every slot
- Integrated data slicer for easier radio interfacing
- Advanced data recovery circuit for improved performance
- Support for antenna diversity and multiple synthesizers
- Fast antenna selection on prolonged preamble
- Lower MAC layer source code provided for PP and FP (RAP and GAP compliant)
- 2.7-3.3V operation (5V support on IOM-2 interface and radio interface)
- Low power consumption for WLL terminals
- PWT support for US PCS applications
- Hardware and software commonality with other Vega-family devices

AVAILABILITY

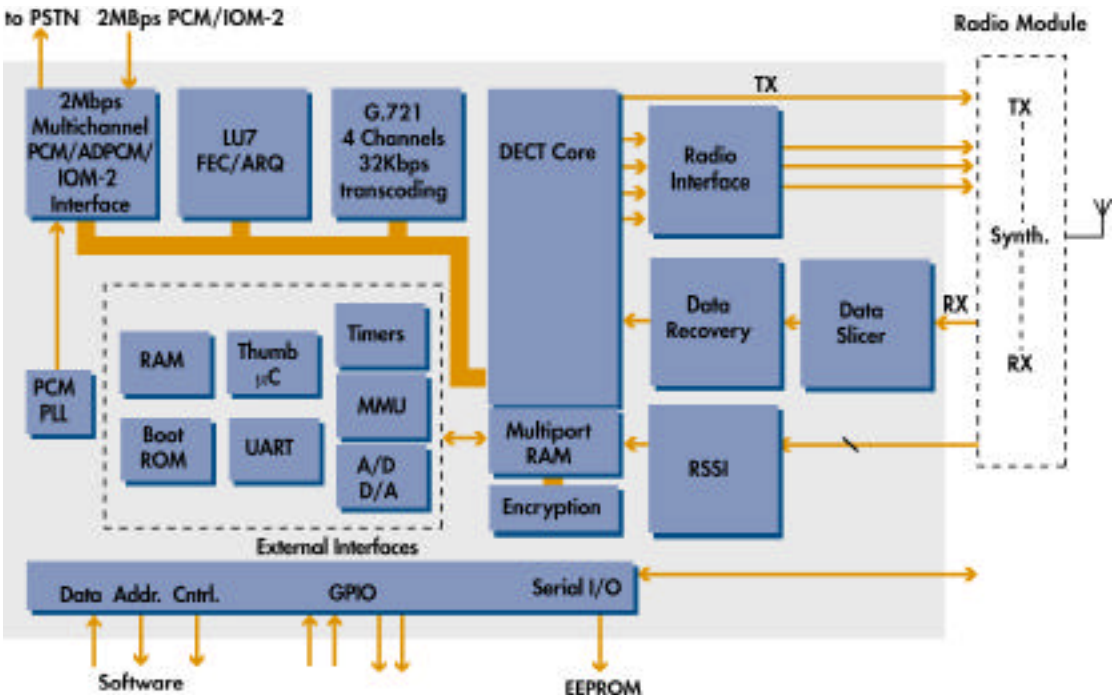
VWS23112 Vega VMax samples are already available, with production following in 1Q98. Development tools and boards aid customers in system prototyping, while the commonality with other Vega-family devices speeds development.

KEY BLOCKS

Physical Layer Processor

The Vega VMax, in common with other members of the Vega family, is based around VLSI's advanced DECT core or Physical Layer

Block Diagram



Processor. The core supports fully programmable B-field sizes, permitting half-, full- and double-slot operation, as well as allowing mixed slot sizes within a single TDMA frame. This flexibility allows manufacturers to implement powerful data features, including 64 kbps data support. In the Vega VMax device this 64 kbps support is enhanced by the inclusion of a Reed-Solomon coder supporting the ETSI-defined LU7 64 kbps data profile, thus allowing ISDN signals to be sent seamlessly over DECT.

The powerful Slot Control Block structure within the Physical Layer Processor provides slot-by-slot control of key functions such as encryption, muting, interrupts and radio interface signals. The hardware also implements the DECT T-MUX algorithm to reduce the load on the microcontroller, allowing it to be placed in standby mode during communication.

Microcontroller

Vega VMax's on-chip ARM7TDMI RISC microcontroller, in conjunction with the powerful Physical Layer Processor, provides the performance needed for simultaneous voice and/or data communications on all DECT channels. The "Thumb" is a small, powerful 32-bit core with a 16-bit instruction mode allowing efficient performance with 8- or 16-bit-wide memory. The device also incorporates an external 8/16-bit data bus.

PCM/ADPCM/IOM-2 Interface

The Vega VMax incorporates a versatile 2 Mbps interface which supports both IOM-2 and PCM frame structures and provides both 64 kbps and 32 kbps data rates with programmable buffer lengths for both voice and data applications. Three parallel highway interfaces are provided, with individual timing alignment in slave mode. The interface supports long and short frame sync signals, and master or slave operation.

Reed-Solomon Coder for LU7 Data Service

The Vega VMax integrates a Forward Error Correction and Automatic Repeat Request circuit which provides the data processing needed for the DECT LU7 64 kbps protected data service (Reed-Solomon encoding and CRC generation on transmission, and Reed-Solomon decoding and CRC checking on reception). The circuit is capable of supporting six full-duplex LU7 connections simultaneously and is used in ISDN applications.

ADPCM Transcoder

The Vega VMax incorporates a four-channel ADPCM/PCM transcoder compliant with CCITT G.726 for 32 kbps data compression. Eliminating the need for external transcoding circuitry in terminal applications, the transcoder also provides DTMF tone generation and call progress tone generation in the TX and RX direction.

Radio Interface

Designed to minimize radio power consumption by allowing precise timing of radio control signals, the software-programmable Radio Interface allows use of a wide range of radio architectures without the need for additional radio interface logic between baseband and RF modules. A variable synthesizer programming word length supports most synthesizers with 3-wire serial interfaces. The device supports antenna diversity with antenna selection based on prolonged preamble.The A/D converter provides five inputs, allowing it to be used to measure battery voltage, temperature or other system parameters in addition to RSSI.

Data Recovery

Vega VMax's advanced Data Recovery circuit is designed to cope with the complex radio environment faced by new-generation DECT systems. To enhance recovery performance in the presence of interference, the device dynamically controls the data extraction and Fast Slice comparator during the preamble and sync phase of every slot. This ensures that all data recovery parameters are fine-tuned before the packet information is received.

Power Management

For battery-powered applications, in the Idle-Locked state, the device may be placed in suspend mode, maintaining system synchronization with minimal software involvement. A timing measurement and correction mechanism minimizes reference timing drift. In the Active state, the DECT core handles all normal call processing.

Versatile Interfaces

Vega VMax incorporates a series of interfaces to ease system implementation. In addition to a two-wire serial interfaces for connection of devices such as EEPROM, Vega VMax integrates 16 bits of general-purpose I/O and three interrupt inputs.

Clocking Options

Vega VMax supports master input clock frequencies of 10.368 MHz or 13.824 MHz; the internal Thumb microprocessor is clocked at 27.648 MHz.

MAC layer software

Along with training and support, VLSI provides qualified Vega VMax customers with the source code of the lower MAC layer software in order to save software development time and ease porting.

PWT support

Vega VMax is designed to support the PWT standard for PCS equipment in the United States.

PACKAGE

Vega VMax is available in a 144-pin LQFP package.

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Document Control: PB-VMax V1.0 December 97