VLSI Technology

VWS23201/2 VEGA+™

Combining Power and DECT Flexibility

OVERVIEW

VLSI Technology's Vega+™ devices are the latest members of the Vega family of DECT controllers. Two versions of the Vega+ are offered, the VWS23201 optimized for handsets and the VWS23202 for single-PSTN-line base stations. The two devices share a common architecture and together deliver an unmatched price/performance ratio for cost-sensitive DECT applications.

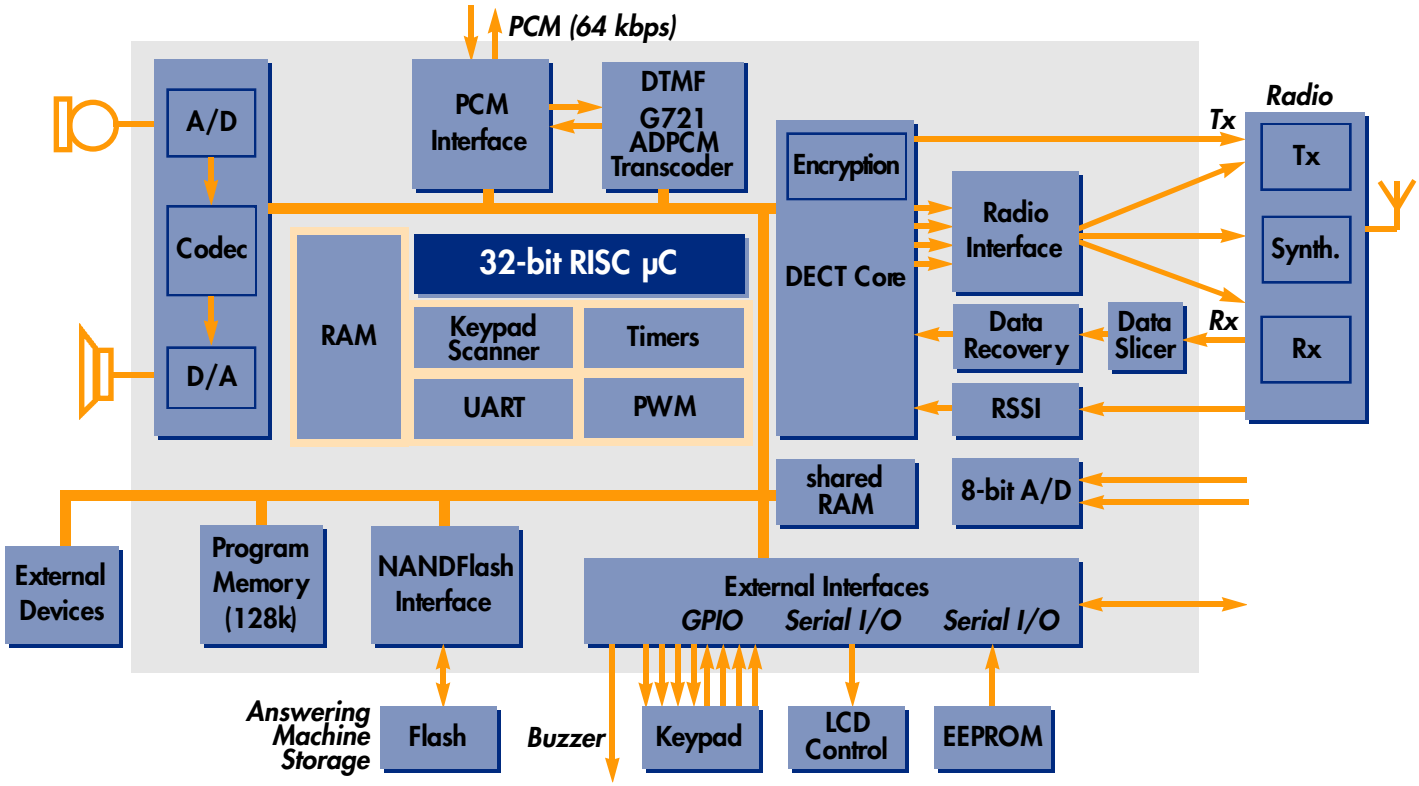
The Vega+ integrates a DECT burst-mode controller with a powerful 32-bit ARM RISC microprocessor, transcoder, codec and memory.

The base station version of Vega+ provides enough processing power to run DSP algorithms such as two-channel transcoding (for conference call functions), Caller Line ID, and voice compression, enabling digital answering machine functionality without the need for a costly external DSP. The Vega+ device also integrates 128 Kbytes of program ROM for a true low-cost single-chip system solution. Development tools and boards allow software integration to be completed before committing to mask-programmed devices.

KEY FEATURES

- Single-chip System-Level Silicon DECT baseband processor optimized for terminals and residential base stations
- On-chip DSP functions for added-value features:
  - · Voice compression
  - · Caller ID
  - · DTMF detection and generation
  - · Three-way calling
- Optional on-chip ROM (128 Kbytes)
- Low power consumption
- Direct peripheral interface to speaker, microphone, radio, keyboard and Flash memory
- Software packages, reference designs and development tools available
- Hardware/software commonality with Vega family DECT devices for WLL, PBX and other applications
- ARM7TDMI™ 32-bit RISC microprocessor
- Optional 128 Kbytes zero-wait-state on-chip mask-programmable ROM
- Multiple I/O ports (programmable pull-ups/pull-downs)
- Core supports E/U-MUX T-MUX and asynchronous handover
- Flexible radio interface
- On-chip data slicer and data recovery circuit for improved performance
- Serial interfaces for EEPROM/LCD and RS-232 connection
- Advanced power management features: 2.5V with 3.3V-compatible I/O
- 4-channel ADC (two general purpose channels available) with powerful auto scanning and battery measurement with interrupt mechanism
- PWT compatibility for US PCS
- Lower MAC GAP stack and DSP software available
- Samples available January 1999

Block Diagram



HANDSET FEATURES

The VWS23201 handset device also includes the following features:

- Single-channel 32 kbps ADPCM/PCM transcoder compliant with CCITT G.726
- 1 Kbytes of shared RAM plus 4 Kbytes of system RAM on-chip
- I/O ports configurable for up to 128 Kbytes address space (8-bit data bus)
- Keypad scanner (5 x 5 keys)
- Integrated audio codec
- 100-pin TQFP package: with or without on-chip ROM (128 Kbytes)
- 80-pin TQFP package, with on-chip ROM (128 Kbytes) and limited I/O

BASE FEATURES

The VWS23202 base station device also includes the following features:

- On-chip DSP functions supported: echo cancellation, Caller Line ID, DTMF detection generation, dial-tone and fax-tone detection, 3-way conferencing and TAD voice compression
- Two-channel ADPCM/PCM transcoder, compliant with CCITT G.726 for 32 Kbps
- 4 Kbytes of shared RAM plus 8 Kbytes of system RAM on-chip
- Interface for direct Flash connection
- I/O ports configurable up to 2 Mbytes address space 16-bit data bus
- Integrated audio codec with 12 and 16 kHz meter pulse detection
- 128-pin TQFP package: with or without on-chip ROM (128 Kbytes)
- 100-pin TQFP package, with on-chip ROM (128 Kbytes) and limited I/O

MICROPROCESSOR

The heart of the Vega+ is a small, powerful ARM7TDMI 32-bit RISC core with a 16-bit instruction mode allowing efficient performance with 8- or 16-bit-wide memory. The normal processor clock frequency is 13.8 MHz, but it can run at speeds up to a class-leading 55 MHz, providing ample MIPS for complex software algorithms running alongside the DECT protocol stack. The clock frequency is software-selectable, allowing a trade-off between processor bandwidth and current consumption.

PHYSICAL LAYER PROCESSOR

The Vega+ architecture is based around VLSI's advanced Vega DECT core. The core supports fully programmable B-field sizes, permitting half-, full- and double-slot operation, as well as allowing mixed-slot sizes within a single TDMA frame. The powerful Slot Control Block structure provides slot-by-slot control of key functions such as encryption, muting, interrupts and radio interface signals. The hardware implements the DECT T-MUX algorithm to reduce the load on the microprocessor, allowing the device to be placed in a suspend state while in idle-locked mode, maintaining synchronization with minimal software involvement.

VOICE INTERFACE

Vega+ incorporates ADPCM/PCM transcoding compliant with CCITT G.726 for 32 Kbps data compression. The base station can support three-way calling (two handsets and an outside line).

In handset applications, Vega+ connects directly to a microphone and earpiece. Multiplexed auxiliary output connections allow a loudspeaker to be driven as well.

RADIO INTERFACE

The software-programmable radio interface allows use of a wide range of radio architectures. A Gaussian pulse-shaping circuit on the TX data output may be used to reduce radio complexity (the digital TX data is also available if required). On the receive side, Vega+ provides an integrated, bypassable, data slicer and data recovery circuit. The RSSI A/D converter provides multiple inputs, allowing measurements of battery voltage or temperature in addition to received signal strength.

VERSATILE INTERFACE

In addition to a UART and a two-wire serial interface (e.g. for connection of an EEPROM and/or LCD controller), Vega+ integrates multiple parallel general-purpose I/O ports. I/O lines have programmable pull-ups and pull-downs to ease system design. Vega+ also includes two programmable PWM interfaces, as well as a ringer interface. The handset version of Vega+ includes a dedicated 5 x 5-key keypad scanner.

SUPPORT PACKAGES

VLSI offers the following packages for Vega+ to accelerate product development:

- Evaluation/Development board interfacing directly to leading DECT radio chipsets
- Lower MAC layer software
- Type-approved GAP software stack
- DSP algorithm portfolio

Software packages and reference designs are also available from third-party suppliers.

For update information, please visit our website at http://www.vlsi.com
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