333Mb/s 17 Channel LVDS to ECL Level Translator

VSC6431

Product Brief

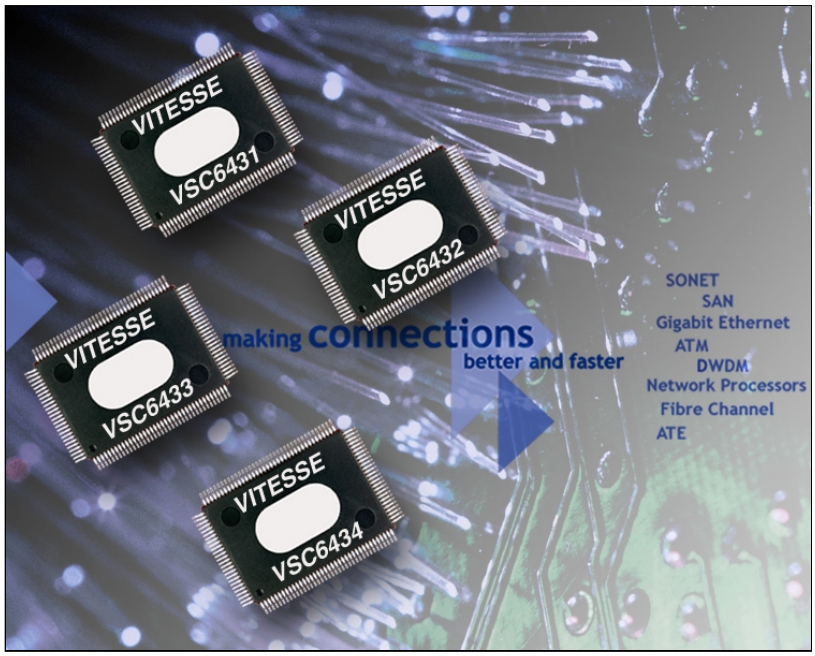
Timing and Logic

Features:

- 333MHz / 333Mb/s Operation
- ECL to LVDS Level Translation
- -2V and +3.3V Power Supplies
- 128-pin Thermally Enhanced PQFP Packaging
- 16 Data Channels, 1 Frame Pulse Channel, and a Clock Channel
- Data and Frame Pulse Retiming with the Clock Channel
- Frame Pulse Output Fanned Out to Four Outputs
- Clock Output Fanned Out to Two Outputs
- Fully Differential Clock Path
- Common Mode Output for Each Clock Output to Aid Single Ended Operation
- On Chip Termination for all LVDS Inputs

Applications:

- ECL to LVDS Technology Bridge



General Description

The VSC6431 is an LVDS to ECL Level Translator. It has 16 Data inputs, 1 Frame Pulse input and 1 Clock input all differential LVDS. The translated 16 Data outputs, 4 Frame Pulse outputs and 2 Clock outputs are all ECL. The 16 Data and 4 Frame Pulse outputs are all single ended ECL. The 2 Clock outputs are differential ECL. The maximum Clock frequency is 333MHz and maximum data rate is 333Mb/S. The Data and Frame outputs are retimed with respect to the rising edge of the True input of the Clock CKINP. All the LVDS inputs have on-chip 100 Ohms termination between the True and the Complimentary inputs. All ECL Outputs require external 50 Ohms termination to VTT. VCOMA and VCOMB are the Common Mode Voltages of the ECL Clock Outputs. LVDS inputs when floating shall have an external terimation of 100 KOhms to VDD or VCC.

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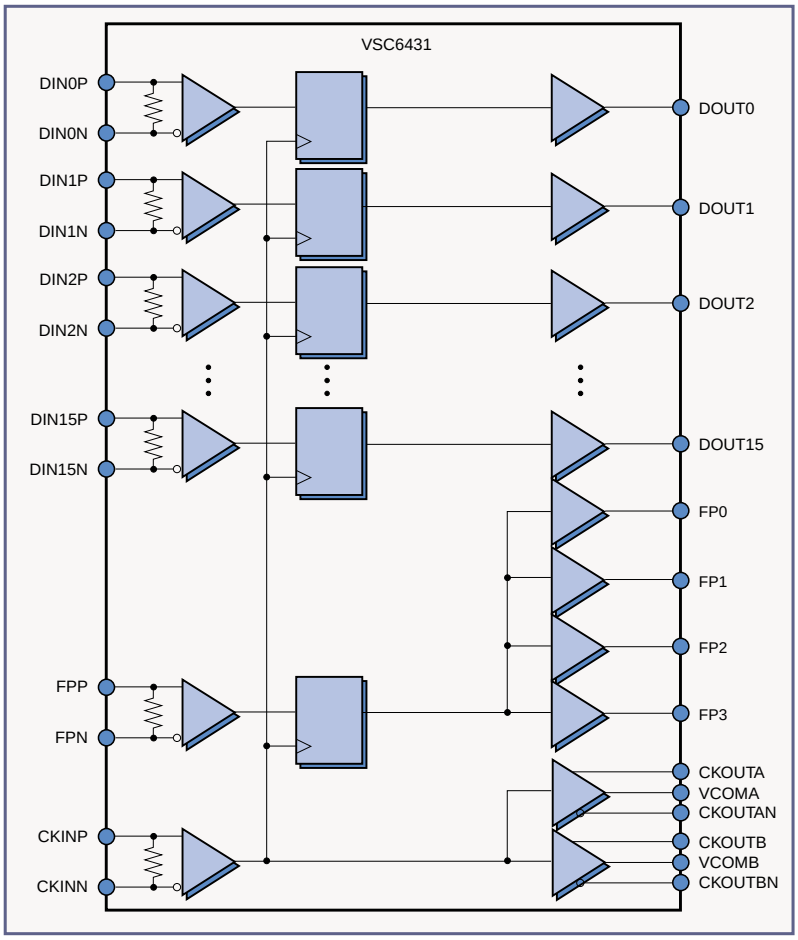
Benefits:

- Bridge Device from Older ECL Devices to the LVDS IO Available in CMOS Today
- Two Chip Solution for Bi-directional Data Flow. (VSC6432 is the Partner IC)
- Translation from a Negative Supply Technology to a Positive Supply Technology
- Retiming of the Data and Frame Pulse Channels to Bound Channel to Channel Skew and Ease System Integration
- Fully Differential Clock Path to Minimize Duty Cycle Distortion

Specifications:

- Data Rate: DC – 333Mb/s/333MHz
- Total Power Dissipation: 1.7W Maximum
- Supplies: -2V, & +3.3V
- 128-Pin PQFP Package
- On Chip 100 Ohm Input Termination
- 200mV LVDS Input Voltage Swing
- 300mV Differential ECL Output Swing
- 600mV Single Ended ECL Output Swing

VSC6431 Block Diagram



AC Characteristics

Description	Minimum	Maximum	Units
Input Data/Frame to Clock Setup Time	720		pS
Input Data/Frame to Clock Hold Time	220		pS
Clock Output to Data/Frame Output Skew	100	1100	pS

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