BURR - BROWN®

VSP3100

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14-Bit, 10MHz CCD/CIS SIGNAL PROCESSOR

FEATURES

- INTEGRATED TRIPLE-CORRELATED DOUBLE SAMPLER
- OPERATION MODE SELECTABLE: 1-Channel, 3-Channel, 10MSPS (typ), CCD/CIS Mode
- PROGRAMMABLE GAIN AMPLIFIER: 0dB to +13dB
- SELECTABLE OUTPUT MODES: Normal/Demultiplexed
- OFFSET CONTROL RANGE: ±400mV
- +3V, +5V Digital Output
- LOW POWER: 450mW (typ)
- LQFP-48 SURFACE-MOUNT PACKAGE

DESCRIPTION

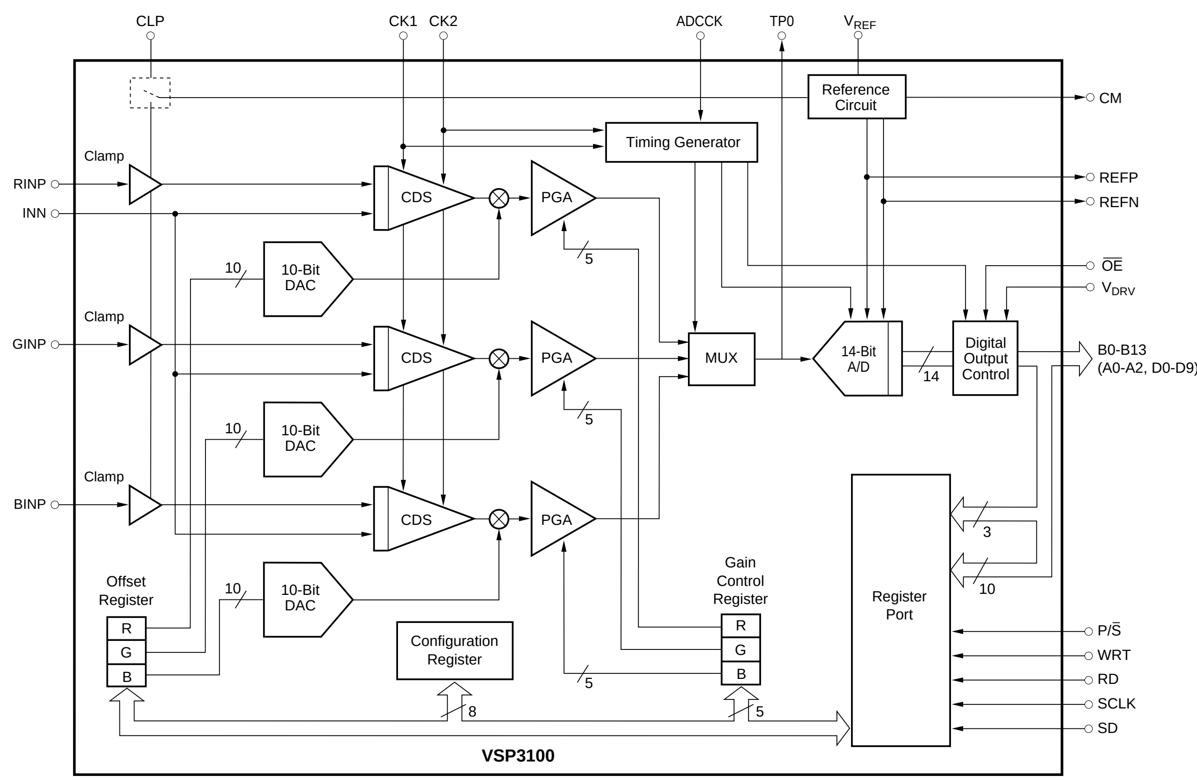
The VSP3100 is a complete CCD/CIS image processor which operates from a single +5V supply.

This complete image processor includes three Correlated Double Samplers (CDS) and Programmable Gain Amplifiers (PGA) to process CCD signals.

These three channel inputs also allow Contact Image Sensor (CIS) inputs.

The VSP3100 is an interface compatible with the VSP3000 which is 12-bit one-chip product.

The VSP3100 can be operated from 0°C to +85°C and is available in an LQFP-48 package.



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PDS-1583A

Printed in U.S.A. April, 2000

SBMS007

SPECIFICATIONS

At T_A = full specified temperature range, V_{CC} = +5V, f_{ADCCK} = 6MHz, f_{CK1} = 2MHz, f_{CK2} = 2MHz, PGA gain = 1, normal output mode, no output load, unless otherwise specified.

PARAMETER	CONDITIONS	VSP3100Y MIN	VSP3100Y TYP	VSP3100Y MAX	UNITS
RESOLUTION			14		Bits
CONVERSION CHARACTERISTICS					
1-, 3-Channel CDS Mode		10			MSPS
1-, 3-Channel CIS Mode		10			MSPS
DIGITAL INPUTS					
Logic Family			CMOS		
Convert Command	Start Conversion		Rising Edge of ADCCK Clock		
High Level Input Current (V_{IN} = V_{CC})				20	µA
Low Level Input Current (V_{IN} = 0V)				20	µA
Positive-Going Threshold Voltage	Pins 18, 19, 20, 21, 22, 24			3.80	V
Negative-Going Threshold Voltage	Pins 18, 19, 20, 21, 22, 24	1.25			V
Positive-Going Threshold Voltage	Pins 12, 14, 15, 16			2.20	V
Negative-Going Threshold Voltage	Pins 12, 14, 15, 16	0.80			V
Input Capacitance			5		pF
ANALOG INPUTS					
Full-Scale Input Range		0.5		3.5	Vp-p
Input Capacitance			10		pF
Input Limits		AGND – 0.3		V_{CC} + 0.3	V
External Reference Voltage Range		0.25		0.3	V
Reference Input Resistance			800		Ω
DYNAMIC CHARACTERISTICS					
Integral Non-Linearity (INL)			±4.0		LSB
Differential Non-Linearity (DNL)			0.5		LSB
No Missing Codes			Guaranteed		Bits
Output Noise	Gain = 0dB, Input Grounded		0.5		LSBs rms
PSRR			0.04		% FSR
DC ACCURACY					
Zero Error	Gain = 0dB		0.8		% FS
Gain Error	Gain = 0dB		1.5		% FS
DIGITAL OUTPUTS					
Logic Family			TTL/HCT		
Logic Coding			Straight Offset Binary		
Digital Data Output Rate, Max	Normal Mode		10		MHz
	Demultiplexed Mode		10		MHz
V_{DRV} Supply Range		+2.7		+5.3	V
Output Voltage, V_{DRV} = +5V					
Low Level	I_{OL} = 50µA			+0.1	V
High Level	I_{OH} = 50µA	+4.6			V
Low Level	I_{OL} = 1.6mA			+0.4	V
High Level	I_{OH} = 0.5mA	+2.4			V
Output Voltage, V_{DRV} = +3					
Low Level	I_{OL} = 50µA			+0.1	V
High Level	I_{OH} = 50µA	+2.5			V
Ouput Enable Time	Output Enable = LOW		20	40	ns
3-State Enable Time	Output Enable = HIGH		2	10	ns
Output Capacitance			5		pF
Data Latency			7		Clock Cycles
Data Output Delay	C_L = 15pF			12	ns
POWER SUPPLY REQUIREMENTS					
Supply Voltage: V_{CC}		4.7	5	5.3	V
Supply Current: I_{CC} (No Load)	3-Ch Mode		90		mA
	1-Ch Mode		75		mA
Power Dissipation (No Load)	3-Ch Mode		450		mW
	1-Ch Mode		375		mW
Thermal Resistance, θ_{JA}			100		°C/W
SPECIFIED TEMPERATURE RANGE			0 to +85		°C

NOTE: (1) SNR = 20log (full-scale voltage/rms noise).

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage[2]	+6.5V
Supply Voltage Differences[3]	±0.1V
GND Voltage Differences[4]	±0.1V
Digital Input Voltage	–0.3V to (V_{CC} + 0.3V)
Analog Input Voltage	–0.3V to (V_{CC} + 0.3V)
Input Current (any pins except suppplies)	±10mA
Operating Temperature	0°C to +85°C
Storage Temperature	–55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering)	+150°C
Package Temperature (IR Reflow, peak, 10s)	+260°C
Package Temperature (IR Reflow, peak, 5s)	+235°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) V_{CC}, V_{DRV}. (3) Among V_{CC}. (4) Among AGND.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

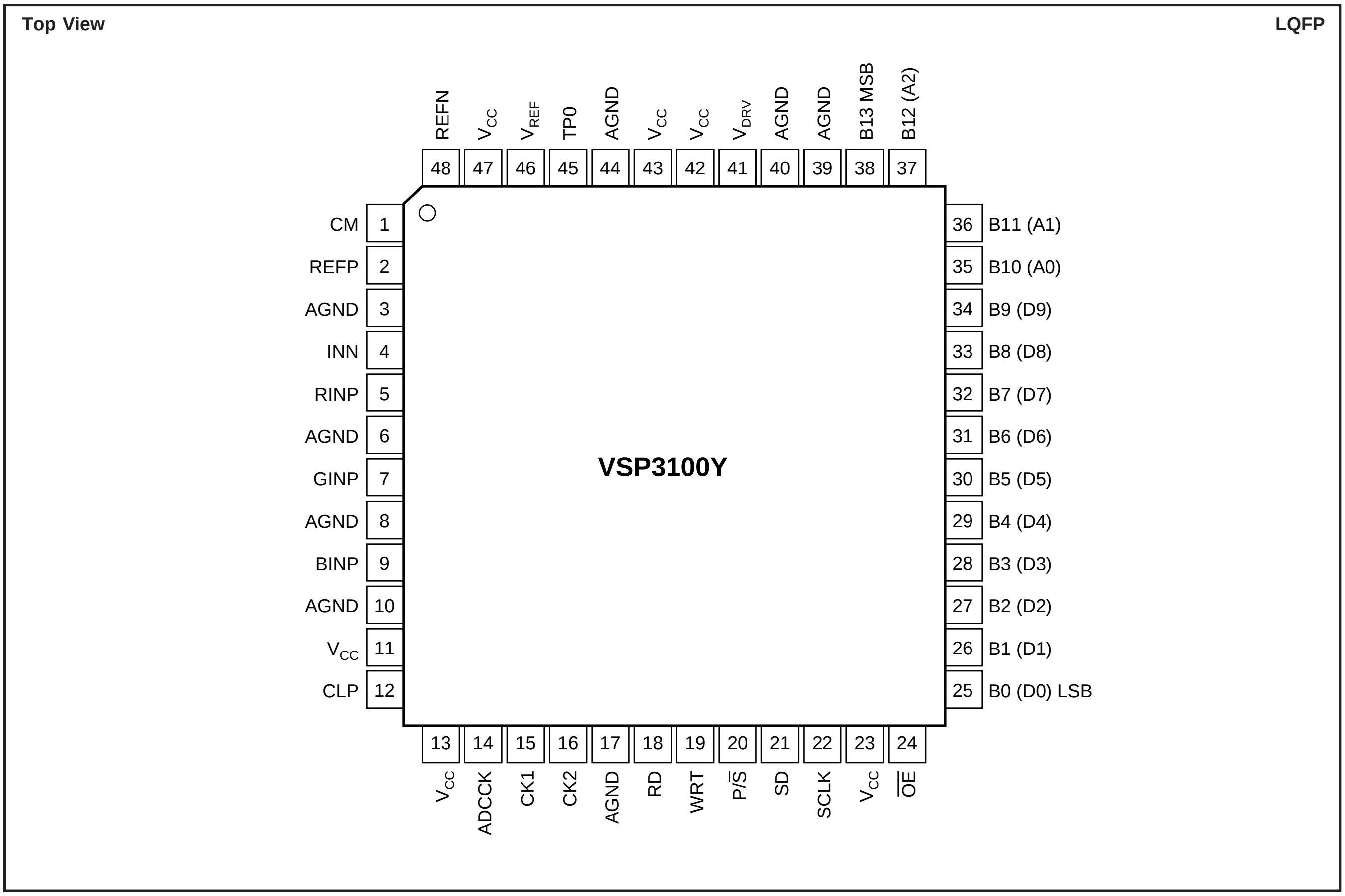
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
VSP3100Y	LQFP-48	340	0°C to +85°C	VSP3100Y	VSP3100Y	250-Piece Tray
"	"	"	"	VSP3100Y	VSP3100Y/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "VSP3100Y/2K" will get a single 2000-piece Tape and Reel.

DEMO BOARD ORDERING INFORMATION

PRODUCT	PACKAGE
VSP3100Y	DEM-VSP3100Y

PIN CONFIGURATION



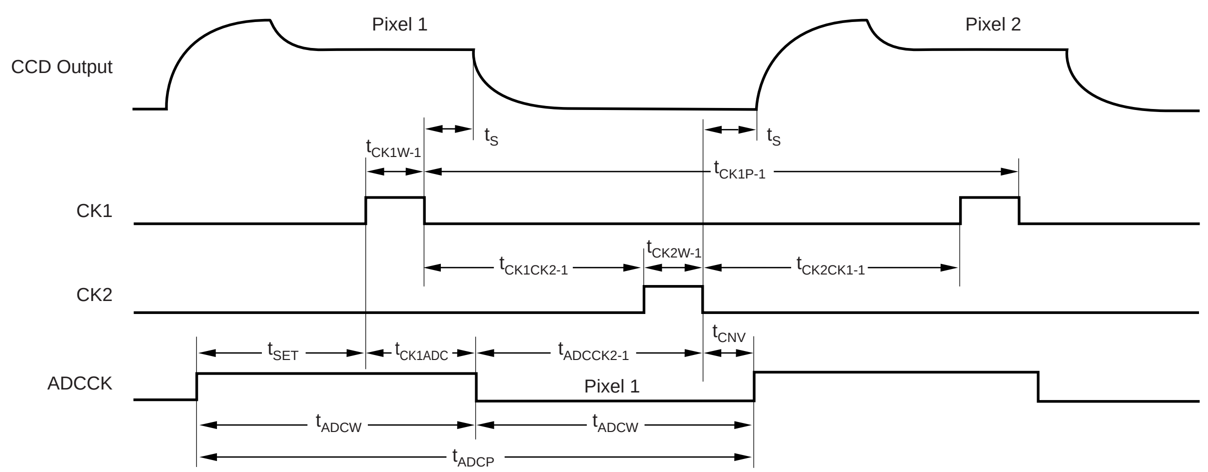
PIN DESCRIPTIONS

PIN	DESIGNATOR	TYPE	DESCRIPTION
1	CM	AO	Common-Mode Voltage
2	REFP	AO	Top Reference
3	AGND	P	Analog Ground
4	INN	AI	Red/Green/Blue Channel Reference Input
5	RINP	AI	Red Channel Analog Input
6	AGND	P	Analog Ground
7	GINP	AI	Green Channel Analog Input
8	AGND	P	Analog Ground
9	BINP	AI	Blue Channel Analog Input
10	AGND	P	Analog Ground
11	V_{CC}	P	Analog Power Supply, +5V
12	CLP	DI	Clamp Enable: "High" = Enable, "Low" = Disable
13	V_{CC}	P	Analog Power Supply, +5V
14	ADCCK	DI	Clock for A/D Converter Digital Data Output
15	CK1	DI	Sample Reference Clock
16	CK2	DI	Sample Data Clock
17	AGND	P	Analog Ground
18	RD	DI	Read Signal for Registers
19	WRT	DI	Write Signal for Registers
20	P/$\overline{S}$	DI	Parallel/Serial Port Select "High" = Parallel Port, "Low" = Serial Port
21	SD	DI	Serial Data Input
22	SCLK	DI	Serial Data Shift Clock
23	V_{CC}	P	Analog Power Supply, +5V
24	$\overline{OE}$	DI	Output Enable
25	B0 (D0) LSB	DIO	A/D Output (Bit 0) and Register Data (Bit 0)
26	B1 (D1)	DIO	A/D Output (Bit 1) and Register Data (Bit 1)
27	B2 (D2)	DIO	A/D Output (Bit 2) and Register Data (Bit 2)
28	B3 (D3)	DIO	A/D Output (Bit 3) and Register Data (Bit 3)
29	B4 (D4)	DIO	A/D Output (Bit 4) and Register Data (Bit 4)
30	B5 (D5)	DIO	A/D Output (Bit 5) and Register Data (Bit 5)
31	B6 (D6)	DIO	A/D Output (Bit 6) and Register Data (Bit 6)
32	B7 (D7)	DIO	A/D Output (Bit 7) and Register Data (Bit 7)
33	B8 (D8) B0: Demiltiplexed Mode	DIO	A/D Output (Bit 8) and Register Data (Bit 8) A/D Output (Bit 0) when Demultiplexed Output Mode
34	B9 (D9) B1: Demiltiplexed Mode	DIO	A/D Output (Bit 9) and Register Data (Bit 9) A/D Output (Bit 1) when Demultiplexed Output Mode
35	B10 (A0) B2: Demiltiplexed Mode	DIO	A/D Output (Bit 10) and Register Address (Bit 0) A/D Output (Bit 2) when Demultiplexed Output Mode
36	B11 (A1) B3: Demiltiplexed Mode	DIO	A/D Output (Bit 11) and Register Address (Bit 1) A/D Output (Bit 3) when Demultiplexed Output Mode
37	B12 (A2) B4: Demiltiplexed Mode	DIO	A/D Output (Bit 12) and Register Address (Bit 2) A/D Output (Bit 4) when Demultiplexed Output Mode
38	B13 MSB B5: Demiltiplexed Mode	DO	A/D Output (Bit 13) A/D Output (Bit 5) when Demultiplexed Output Mode
39	AGND	P	Analog Ground
40	AGND	P	Analog Ground
41	V_{DRV}	P	Digital Output Driver Power Supply
42	V_{CC}	P	Analog Power Supply, +5V
43	V_{CC}	P	Analog Power Supply, +5V
44	AGND	P	Analog Ground
45	TP0	AO	A/D Converter Input Monitor Pin (single-ended output)
46	V_{REF}	AIO	Reference Voltage Input/Output
47	V_{CC}	P	Analog Power Supply, +5V
48	REFN	AO	Bottom Reference

TIMING DIAGRAMS

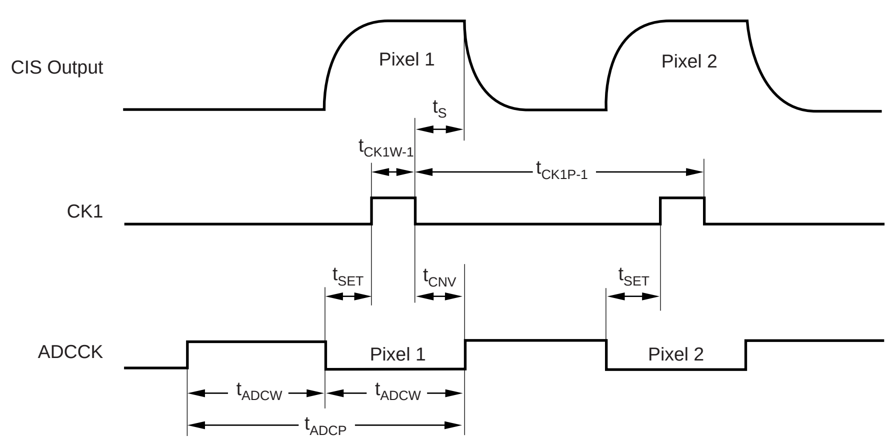
Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

1-Channel CCD Mode Timing



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CK1W-1}	CK1 Pulse Width	20	40		ns
t_{CK1P-1}	1-Channel Mode Conversion Rate	100	166		ns
t_{CK2W-1}	CK2 Pulse Width	20	40		ns
$t_{CK1CK2-1}$	CK1 Falling to CK2 Rising	15			ns
$t_{CK2CK1-1}$	CK2 Falling to CK1 Rising	40			ns
t_{CK1ADC}	CK1 Rising to ADCCK Falling	20			ns
$t_{ADCCK2-1}$	ADCCK Falling to CK2 Falling	15			ns
t_{ADCW}	ADCCK Pulse Width	41	83		ns
t_{ADCP}	ADCCK Period	83	166		ns
t_S	Sampling Delay	10			ns
t_{SET}	ADCCK Rising to CK1 Rising	10			ns
t_{CNV}	Conversion Delay	40			ns

1-Channel CIS Mode Timing

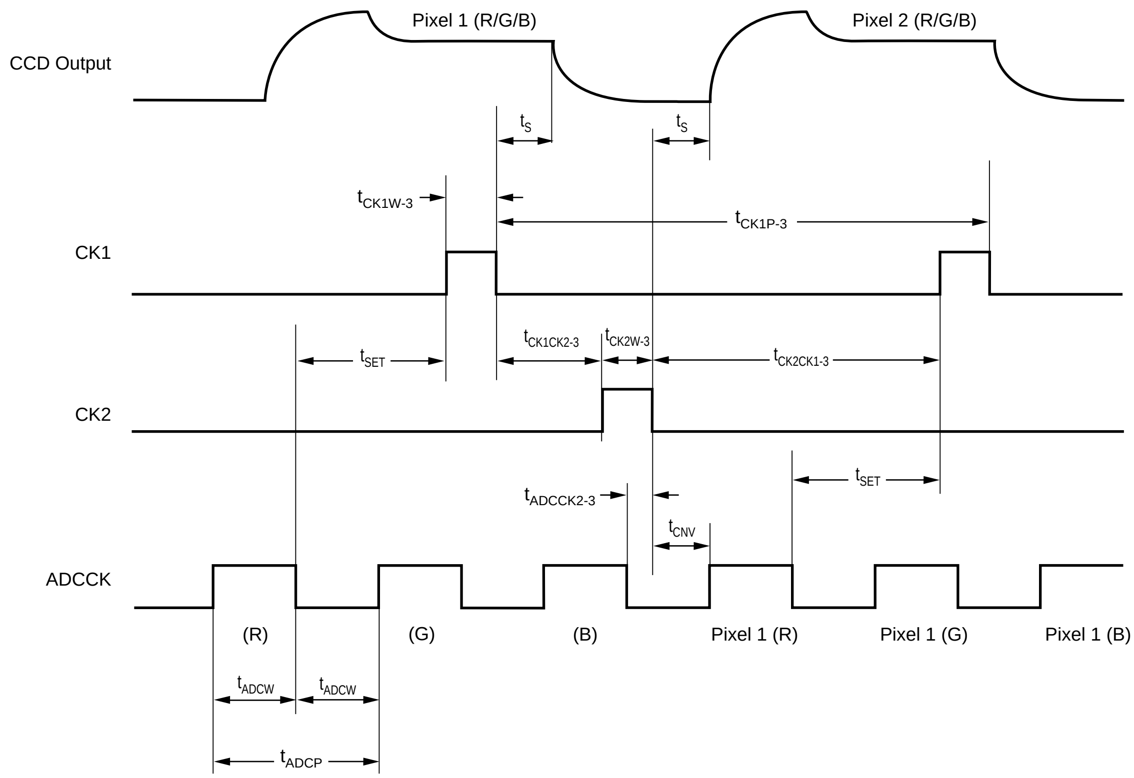


SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CK1W-1}	CK1 Pulse Width	20	40		ns
t_{CK1P-1}	1-Channel Mode Conversion Rate	100	166		ns
t_{ADCW}	ADCCK Pulse Width	41	83		ns
t_{ADCP}	ADCCK Period	83	166		ns
t_S	Sampling Delay	10			ns
t_{SET}	ADCCK Falling to CK1 Rising	10			ns
t_{CNV}	Conversion Delay	40			ns

TIMING DIAGRAMS (Cont.)

Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

3-Channel CCD Mode Timing

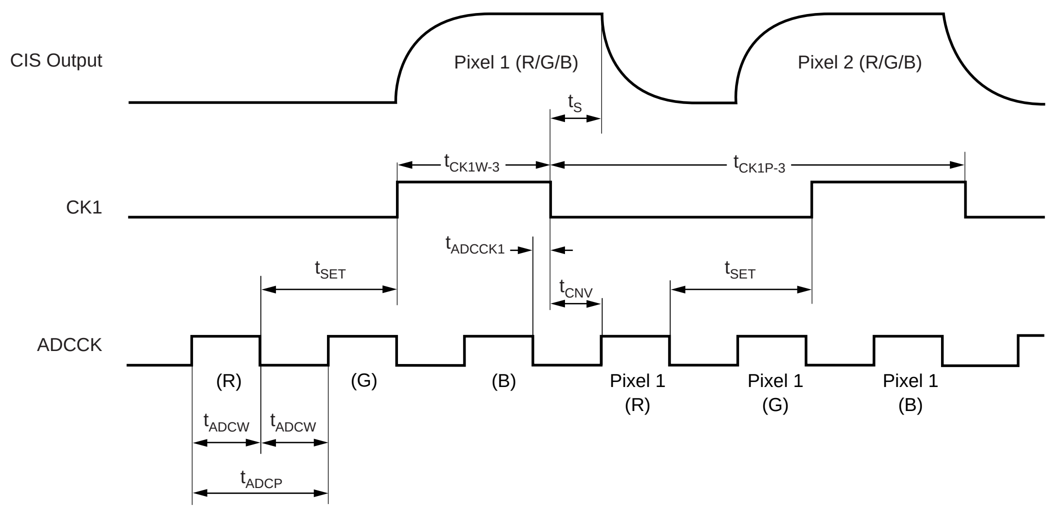


SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CK1W-3}	CK1 Pulse Width	20	125		ns
t_{CK1P-3}	3-Channel Mode Conversion Rate	300	500		ns
t_{CK2W-3}	CK2 Pulse Width	20	125		ns
$t_{CK1CK2-3}$	CK1 Falling to CK2 Rising	15			ns
$t_{CK2CK1-3}$	CK2 Falling to CK1 Rising	70			ns
$t_{ADCCK2-3}$	ADCCK Falling to CK2 Falling	5			ns
t_{ADCW}	ADCCK Pulse Width	41	83		ns
t_{ADCP}	ADCCK Period	83	166		ns
t_S	Sampling Delay	10			ns
t_{SET}	ADCCK Rising to CK1 Rising	10			ns
t_{CNV}	Conversion Delay	40			ns

TIMING DIAGRAMS (Cont.)

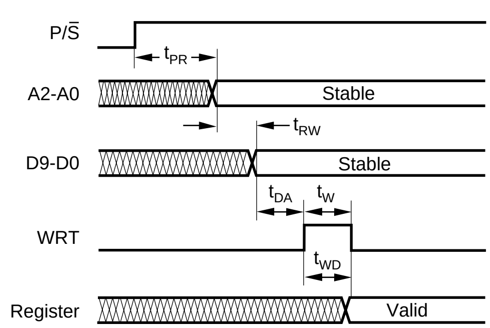
Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

3-Channel CIS Mode Timing



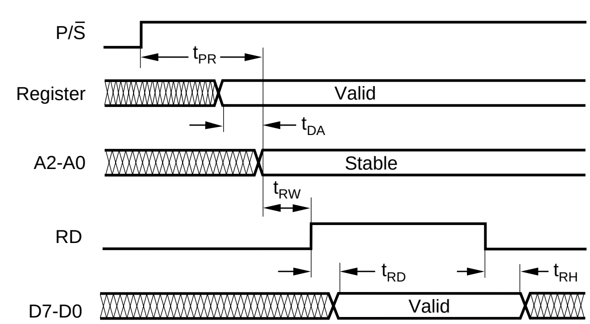
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CK1W-3}	CK1 Pulse Width	20	125		ns
t_{CK1P-3}	3-Channel Mode Conversion Rate	300	500		ns
t_{ADCCK1}	ADCCK Falling to CK1 Falling	5			ns
t_{ADCW}	ADCCK Pulse Width	41	83		ns
t_{ADCP}	ADCCK Period	83	166		ns
t_S	Sampling Delay	10			ns
t_{SET}	ADCCK Falling to CK1 Rising	10			ns
t_{CNV}	Conversion Delay	40			ns

Timing for Parallel Port Writing



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{PR}	Parallel Ready Time	20			ns
t_W	WRT Pulse Width	30	50		ns
t_{WD}	Data Valid Time			30	ns
t_{RW}	Address Setup Time	20	50		ns
t_{DA}	Data Setup Time	30	50		ns

Timing for Reading

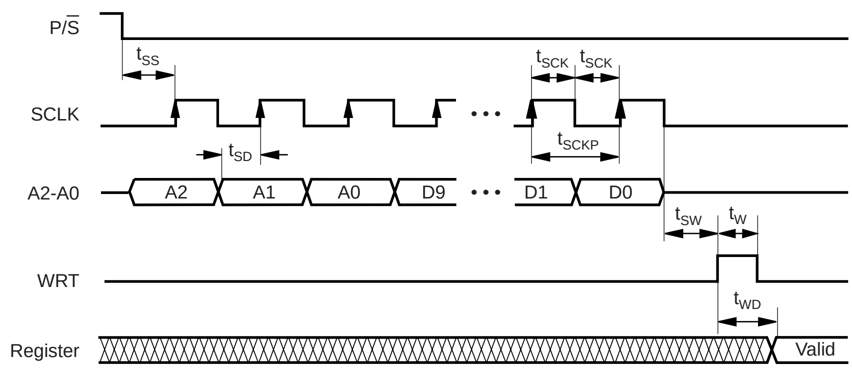


SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{PR}	Parallel Ready Time	20			ns
t_{DA}	Data Setup Time	30	50		ns
t_{RW}	Address Setup Time	20	50		ns
t_{RD}	Readout Delay			20	ns
t_{RH}	Data Hold Time			1	ns

TIMING DIAGRAMS (Cont.)

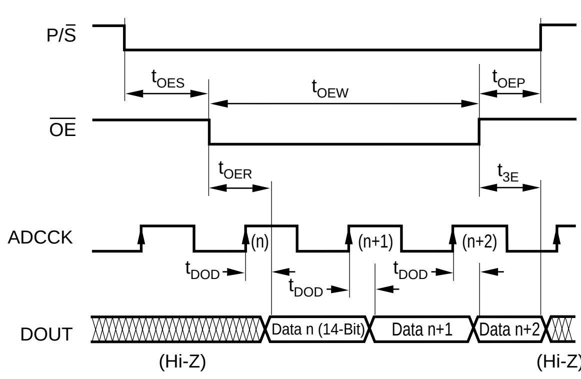
Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

Timing for Serial Port Writing



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	WRT Pulse Width	30	50		ns
t_{WD}	Data Valid Time			30	ns
t_{SD}	Data Ready Time	15	50		ns
t_{SCK}	Serial Clock Pulse Width	30	50		ns
t_{SCKP}	Serial Clock Period	60	100		ns
t_{SS}	Serial Ready Time	100	200		ns
t_{SW}	WRT Pulse Setup Time	50			ns

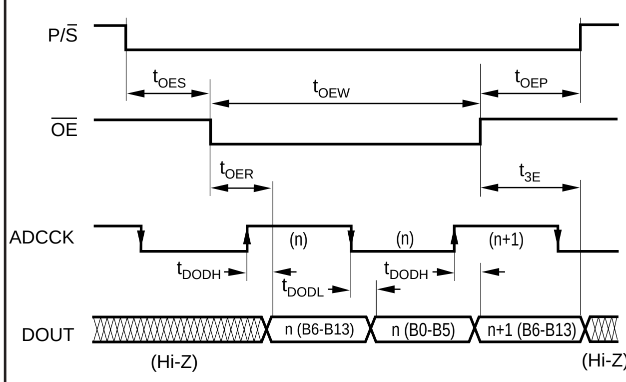
Timing for A/D Output (Normal Operation Mode)



NOTE: It is Inhibit Operation Mode that $\overline{OE}$ sets "Low" during P/$\overline{S}$ = "High" period.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{OES}	A/D Output Enable Setup Time	20			ns
t_{OER}	Output Enable Time		20	40	ns
t_{3E}	3-State Enable Time		2	10	ns
t_{OEW}	$\overline{OE}$ Pulse Width	100			ns
t_{DOD}	Data Output Delay			12	ns
t_{OEP}	Parallel Port Setup Time	10			ns

Timing for A/D Output (Demultiplexed Operation Mode)



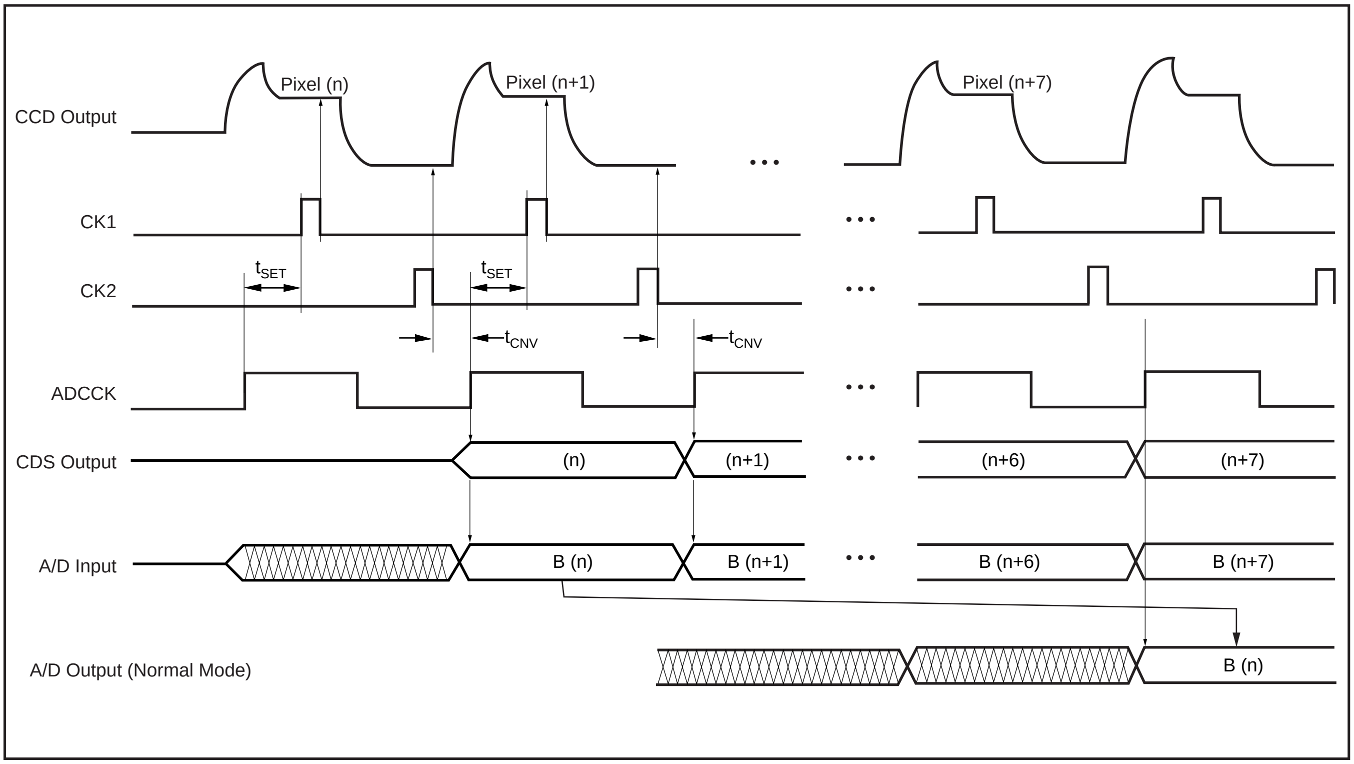
NOTE: It is Inhibit Operation Mode that $\overline{OE}$ sets "Low" during P/$\overline{S}$ = "High" period.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{OES}	A/D Output Enable Setup Time	20			ns
t_{OER}	Output Enable Time		20	40	ns
t_{3E}	3-State Enable Time		2	10	ns
t_{OEW}	$\overline{OE}$ Pulse Width	100			ns
t_{DODH}	Data Output Delay, High Byte			12	ns
t_{DODL}	Data Output Delay, Low Byte			12	ns
t_{OEP}	Parallel Port Setup Time	10			ns

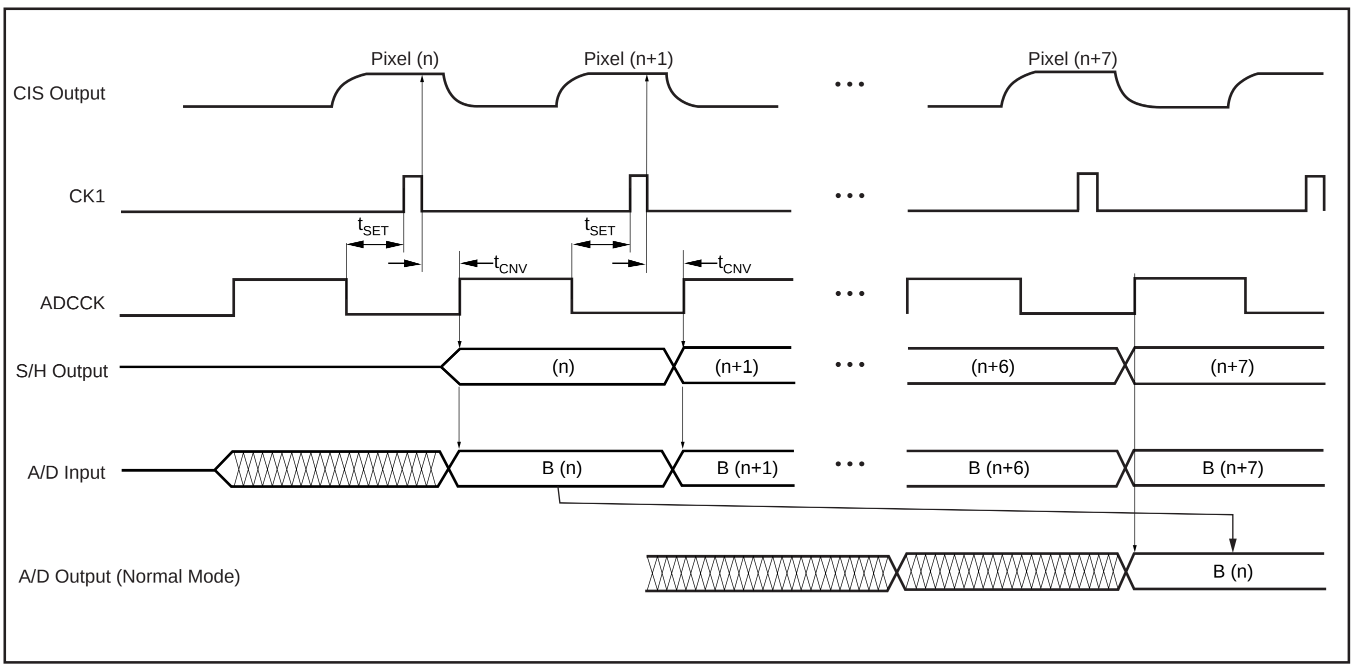
TIMING DIAGRAMS (Cont.)

Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

Digital Data Output Sequence; 1-ch CCD Mode (B-ch: D4 = 1 and D5 = 0)



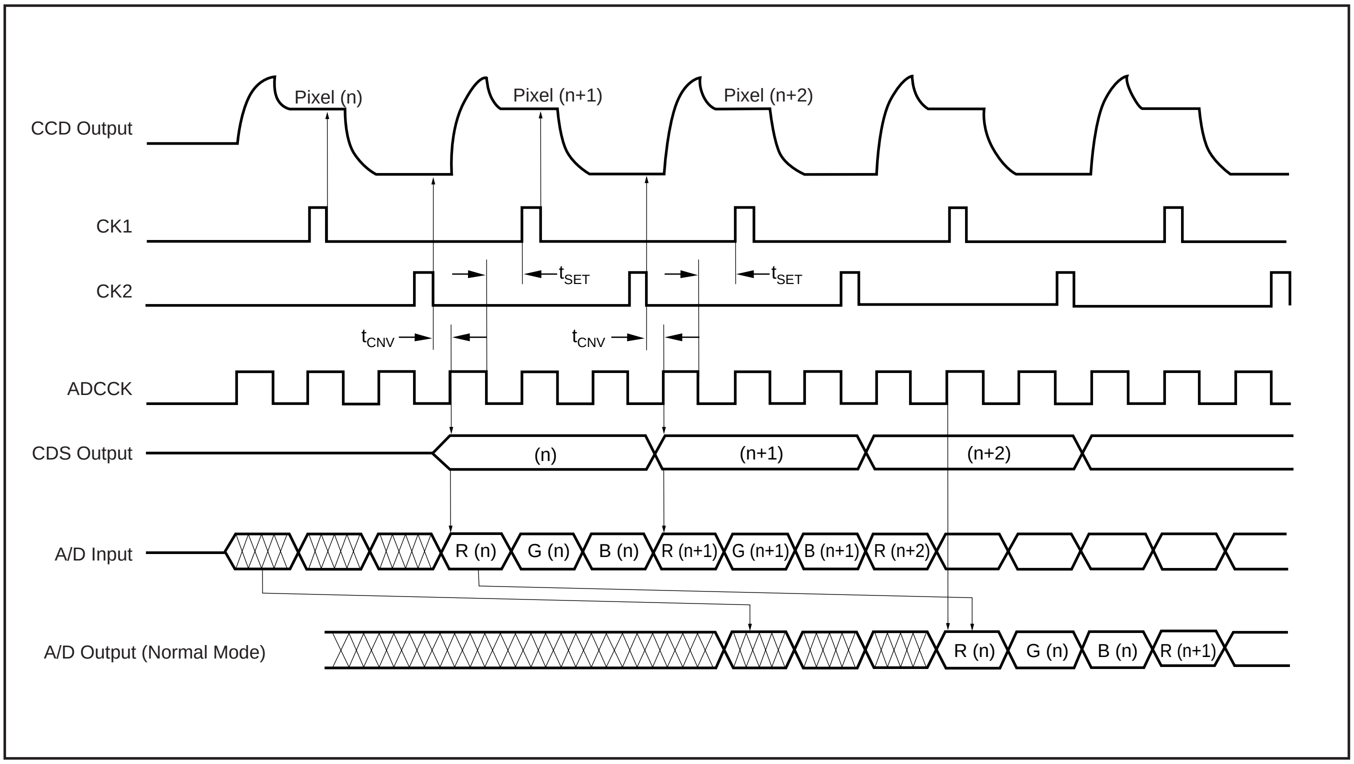
Digital Data Output Sequence; 1-ch CIS Mode (B-ch: D4 = 1 and D5 = 0)



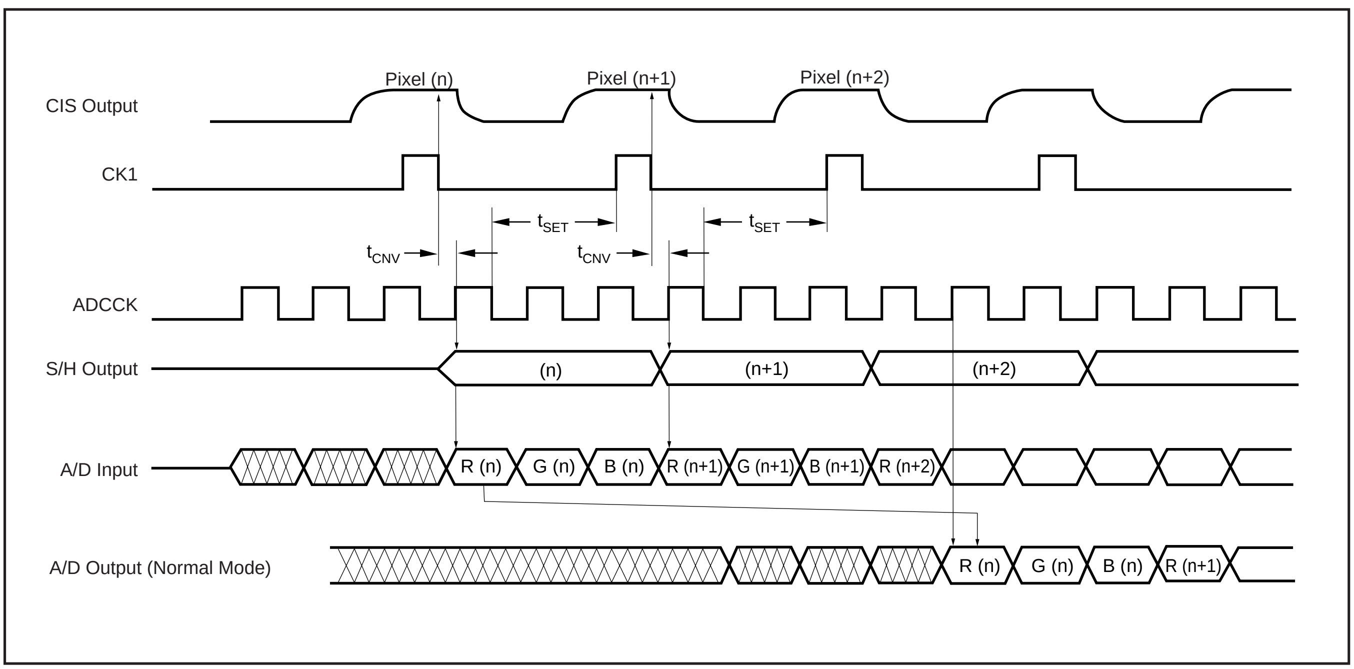
TIMING DIAGRAMS (Cont.)

Timing Specifications: V_{CC} = +5V supply and normal output mode with the specified temperature range, unless otherwise noted.

Digital Data Output Sequence; 3-ch CCD Mode, R > G > B Sequence

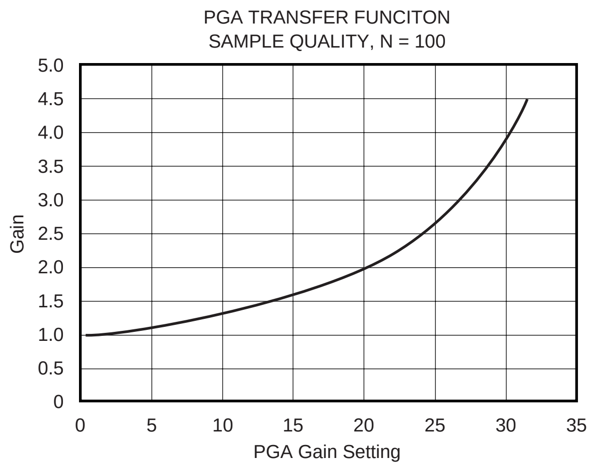


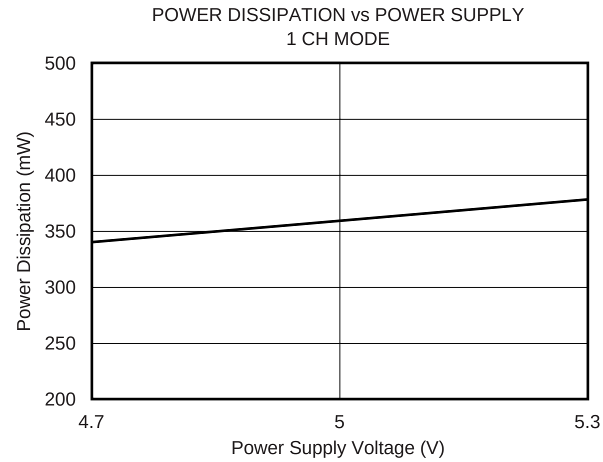
Digital Data Output Sequence; 3-ch CIS Mode, R > G > B Sequence

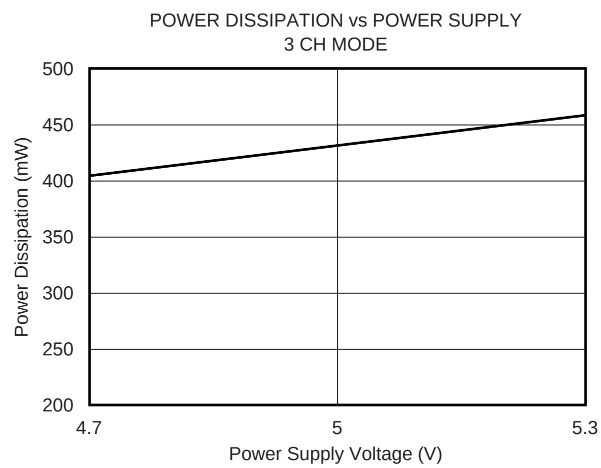


TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +5V supply, t_{ADCCK} = 6MHz, f_{CK1} = 2MHz, f_{CK2} = 2MHz, PGA Gain = 1, normal output mode, no load, unless otherwise specified.







THEORY OF OPERATION

VSP3100 can be operated in one of the following four modes:

(1) 1-Channel CCD

(2) 1-Channel CIS

(3) 3-Channel CCD

(4) 3-Channel CIS

1-CHANNEL CCD MODE

In this mode, the VSP3100 processes only one CCD signal (D3 of the Configuration Register sets to "1"). The CCD signal is AC-coupled to RINP, GINP, or BINP (depending on D4, D5 of the Configuration Register). The CLP signal enables internal biasing circuitry to clamp this input to a proper voltage, so that internal CDS circuitry can work properly. The VSP3100 input may be applied as a DC-coupled input, which needs to be level-shifted to a proper DC level.

The CDS takes two samples of the incoming CCD signals. The CCD reset signal is taken on the falling edge of CK1 and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDS and the result is stored as a CDS output.

In this mode, only one of the three channels is enabled. Each channel consists of a 10-bit Offset DAC (range from –400mV to +400mV). A 3-to-1 analog MUX is inserted between the CDSs and a high-performance 14-bit analog-to-digital converter. The outputs of the CDSs are then multiplexed to the A/D converter for digitization. The analog MUX is not cycling between channels in this mode. Instead, it is connected to a specific channel, depending on the contents of D4 and D5 in the Configuration Register.

The VSP3100 allows two types of output modes:

1) Normal (D7 of Configuration Register sets to "0").

2) Demultiplexed (D7 of Configuration Register sets to "1").

As specified in the "1-Channel CCD Mode" timing diagram, the rising edge of CK1 must be in the HIGH period of ADCCK, and at the same time, the falling edge of the CK2 must be in the LOW period of ADCCK. Otherwise, the VSP3100 will not function properly.

1-CHANNEL CIS MODE

In this mode, the VSP3100 operates as a 1-channel sampler and digitizer. Unlike CDS modes, the VSP3100 takes only one sample on the falling edge of the CK1. Since only one sample is taken, CK2 is grounded in this operation. The input signal is DC coupled in most cases. Here, VSP3100 inputs are differential input. Using the Red channel as an example, RINP is the CIS input signal, and INN is the CIS common reference signal input. The same applies to the Green channel (GINP and INN) and Blue channel (BINP and INN).

In this mode, CDS becomes CIS (act like sample-and-hold). Each channel consists of a 10-bit Offset DAC (range from –400mV to +400mV).

A 3-to-1 analog MUX is inserted between the CISs and a high-performance, 14-bit A/D converter. The outputs of the CIS are then multiplexed to the A/D converter for digitization. The analog MUX is not cycling between channels in this mode. Instead, the analog MUX is connected to a specific channel, depending on the contents of D4 and D5 in the Configuration Register.

The VSP3100 allows two types of output modes:

1) Normal (D7 of Configuration Register sets to "0").

2) Demultiplexed (D7 of Configuration Register sets to "1").

As specified in the "1-Channel CIS Mode" timing diagram, the active period of both CK1 (t_{CK1B}) and CK2 (t_{CK2B}) must be in the LOW period of ADCCK. If it is in the HIGH period of ADCCK, the VSP3100 will not function properly.

3-CHANNEL CCD MODE

In this mode, the VSP3100 can simultaneously process triple output CCD signals. CCD signals are AC coupled to the RINP, GINP, and BINP inputs. The CLP signal enables internal biasing circuitry to clamp these inputs to a proper voltage so that internal CDS circuitry can work properly. VSP3100 inputs may be applied as a DC-coupled inputs, which need to be level-shifted to a proper DC level.

The CDSs take two samples of the incoming CCD signals. The CCD reset signals are taken on the falling edge of CK1 and the CCD information is taken on the falling edge of CK2. These two samples are then subtracted by the CDSs and the results are stored as a CDS output.

In this mode, three CDSs are used to process three inputs simultaneously. Each channel consists of a 10-bit Offset DAC (range from –400mV to +400mV). A 3-to-1 analog MUX is inserted between the CDSs and a high-performance, 14-bit A/D converter. The outputs of the CDSs are then multiplexed to the A/D converter for digitization. The analog MUX is switched at the falling edge of CK2, and can be programmed to cycle between the Red, Green, and Blue channels. When D6 of the Configuration Register sets to "0", the MUX sequence is Red > Green > Blue. When D6 of the Configuration Register sets to "1", the MUX sequence is Blue > Green > Red.

MUX resets at the falling edge of CK1. In the case of a Red > Green > Blue sequence, it resets to "R", and in the case of a Blue > Green > Red sequence, it resets to "B".

The VSP3100 allows two types of output modes:

1) Normal (D7 of Configuration Register sets to "0").

2) Demultiplexed (D7 of Configuration Register sets to "1").

As specified in the "3-Channel CCD Mode" timing diagram, the falling edge of CK2 must be in the LOW period of ADCCK. If the falling edge of CK2 is in the HIGH period of ADCCK (in the timing diagram, ADCCK for sampling B-channel), the VSP3100 will not function properly.

3-CHANNEL CIS MODE

In this mode, the VSP3100 is operated as 3-channel samplers and a digitizer. Unlike CCD modes, VSP3100 takes only one sample on the falling edge of CK1 for each input. Since only one sample is taken, CK2 is grounded in this operation. The input signals are DC coupled in most cases. Here, the VSP3100 inputs allow differential inputs. Using the Red channel as an example, RINP is the CIS input signal, and INN is the CIS common reference signal input. The same applies to the Green channel (GINP and INN) and Blue channel (BINP and INN).

In this mode, three CDSs become CISs (act like sample-and-hold) to process three inputs simultaneously. Each channel consists of a 10-bit Offset DAC (range from –400mV to +400mV). A 3-to-1 analog MUX is inserted between the CISs and a high-performance, 14-bit A/D converter. The outputs of the CIS are then multiplexed to the A/D converter for digitization. The analog MUX is switched at the falling edge of CK2, and can be programmed cycling between the Red, Green, and Blue channels. When D6 of the Configuration Register sets to "0", the MUX sequence is Red > Green > Blue. When D6 of the Configuration Register sets to "1", the MUX sequence is Blue > Green > Red.

MUX resets at the falling edge of CK1. In the case of a Red > Green > Blue sequence, it resets to "R", and in the case of a Blue > Green> Red sequence, it resets to "B".

The VSP3100 allows two types of output modes:

1) Normal (D7 of Configuration Register sets to "0").

2) Demultiplexed (D7 of Configuration Register sets to "1").

As specified in the "3-Channel CIS Mode" timing diagram, the falling edge of CK1 must be in the LOW period of ADCCK. If the falling edge of CK1 is in the HIGH period of ADCCK (in the timing diagram, ADCCK for sampling B-channel), the VSP3100 will not function properly.

DIGITAL OUTPUT FORMAT

The Digital Output Format is shown in Table I. The VSP3100 can be operated in one of the following two digital output modes:

(1) Normal output.

(2) Demultiplexed (B13-based Big Endian Format).

In Normal mode, the VSP3100 outputs the 14-bit data by B0 (pin 25) through B13 (pin 38) simultaneously.

In Demultiplexed mode, VSP3100 outputs the high byte (upper 8 bits) by B6 (pin 31) through B13 (pin 38) at the rising edge of ADCCK "HIGH", then outputs the low byte (lower 6 bits) by B8 (pin 33) through B13 (pin 38) at the falling edge of ADCCK.

An 8-bit interface can be used between the VSP3100 and the Digital Signal Processor, allowing for a low-cost system solution.

BIT	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
High Byte	B13	B12	B11	B10	B9	B8	B7	B6	Low	Low	Low	Low	Low	Low
Low Byte	B5	B4	B3	B2	B1	B0	Low	Low	Low	Low	Low	Low	Low	Low

TABLE I. Digital Output Format.

DIGITAL OUTPUTS

The digital outputs of the VSP3100 are designed to be compatible with both high-speed TTL and CMOS logic families. The driver stage of the digital outputs is supplied through a separate supply pin, V_{DRV} (pin 41), which is not connected to the analog supply pins (V_{CC}). By adjusting the voltage on V_{DRV}, the digital output levels will vary respectively. Thus, it is possible to operate the VSP3100 on a +5V analog supply while interfacing the digital outputs to 3V logic. It is recommended to keep the capacitive loading on the data lines as low as possible (typically less than 15pF). Larger capacitive loads demanding higher charging current surges can feed back to the analog portion of the VSP3100 and influence the performance. If necessary, external buffers or latches may be used, providing the added benefit of isolating the VSP3100 from any digital noise activities on the bus, coupling back high-frequency noise. In addition, resistors in series with each data line may help minimize the surge current. Their use depends on the capacitive loading seen by the converter. As the output levels change from low to high and high to low, values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances.

PROGRAMMABLE GAIN AMPLIFIER

VSP3100 has one Programmable Gain Amplifier (PGA), and it is inserted between the CDSs and the 3:1 MUX. The PGA is controlled by a 5-bit of Gain Register and each channel (Red, Green, and Blue) has its own Gain Register.

The gain varies from 1 to 4.44 (0dB to 13dB), and the curve has log characteristics. Gain Register Code all "0" corresponds to minimum gain, and Code all "1" corresponds to maximum gain.

The transfer function of the PGA is:

$$\text{Gain} = 4/(4 - 0.1 \cdot x)$$

where, x is the integer representation of the 5-bit PGA gain register.

Figure 1 shows the PGA transfer function plot.

INPUT CLAMP

The input clamp should be used for 1-channel and 3-channel CCD mode, and it will be enabled when both CLP and CK1 are set to HIGH.

Bit Clamp: the input clamp is always enabled.

Line Clamp: enables during the dummy pixel interval at every horizontal line, and disables during the effective pixel interval.

Generally, "Bit Clamp" is used for many scanner applications, however, "Line Clamp" is used instead of "Bit Clamp" when the clamp noise is impressive.

CHOOSING THE AC INPUT COUPLING CAPACITORS

The purpose of the Input Coupling Capacitor is to isolate the DC offset of the CCD array from affecting the VSP3100 input circuitry. The internal clamping circuitry is used to restore the necessary DC bias to make the VSP3100 input circuitry functional. Internal clamp voltage, V_{CLAMP}, is set when both the CLP pin and CK1 are set high. V_{CLAMP} changes depending on the value of V_{REF}. V_{CLAMP} is 2.5V if V_{REF} is set to 1V (D1 of the Configuration Register set to "0"), and V_{CLAMP} is 3V if V_{REF} is set to 1.5V (D1 of the Configuration Register set to "1").

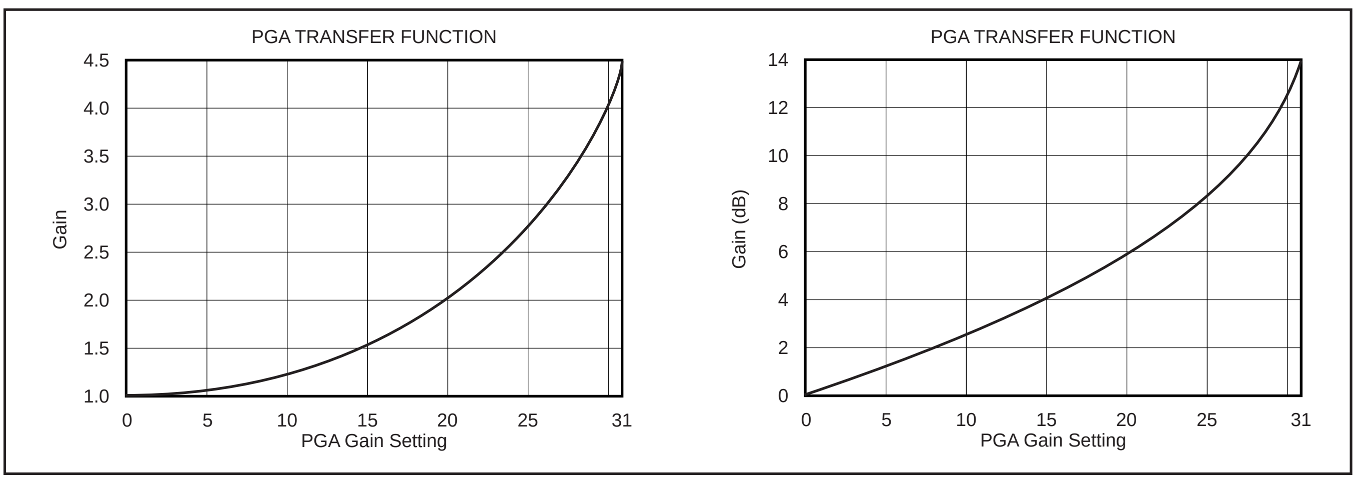


FIGURE 1. PGA Transfer Plot.

There are many factors that decide what size of Input Coupling Capacitor is needed. Those factors are CCD signal swing, voltage difference between the Input Coupling Capacitor, leakage current of the VSP3100 input circuitry, and the time period of CK1.

Figure 2 shows the equivalent circuit of the VSP3100 inputs.

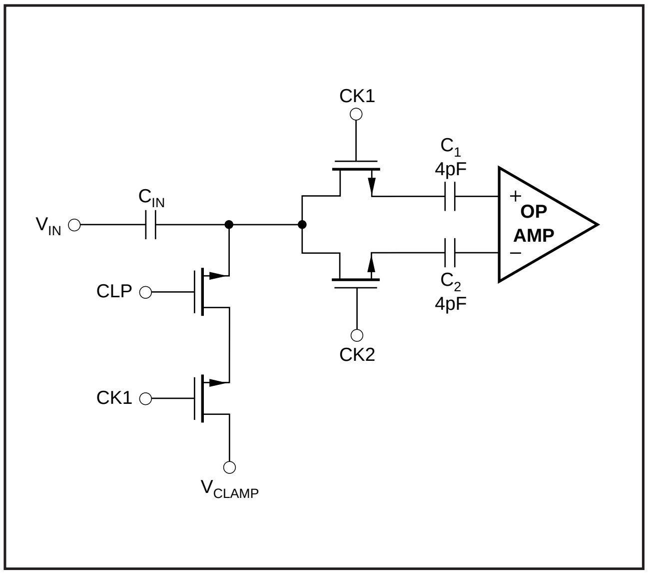


FIGURE 2. Equivalent Circuit of VSP3100 Inputs.

In this equivalent circuit, Input Coupling Capacitor C_{IN}, and Sampling Capacitor C_1, are constructed as a capacitor divider (during CK1). For AC analysis, OP inputs are grounded. Therefore, the sampling voltage, V_S, (during CK1) is:

$$V_S = (C_{IN}/(C_{IN} + C_1)) \cdot V_{IN}$$

From the above equation, we know that a larger C_{IN} makes V_S close to V_{IN}. In other words, input signal, V_{IN}, will not be attenuated if C_{IN} is large.

However, there is a disadvantage of using a large C_{IN}. It will take longer for the CLP signal to charge up C_{IN} so that the input circuitry of the VSP3100 can work properly.

CHOOSE C_{MAX} AND C_{MIN}

As mentioned, a large C_{IN} is better if there is enough time for the CLP signal to charge up C_{IN} so that the input circuitry of the VSP3100 can work properly. Typically, 0.01µF to 0.1µF of C_{IN} can be used for most cases.

In order to optimize C_{IN}, the following two equations can be used to calculate the maximum (C_{MAX}) and minimum (C_{MIN}) values of C_{IN}:

$$C_{MAX} = (t_{CK1} \cdot N)/[R_{SW} \cdot \ln(V_D/V_{ERROR})]$$

where t_{CK1} is the time when both CK1 and CLP go HIGH, and N is the number of black pixels; R_{SW} is the switch resistance of the VSP3100 (typically, driver impedance + 4kΩ); V_D is the droop voltage of C_{IN}; V_{ERROR} is the voltage difference between V_S and V_{CLAMP}.

$$C_{MIN} = (I/V_{ERROR}) \cdot t$$

where I is the leakage current of the VSP3100 input circuitry (10nA is a typical number for this leakage current); t is the clamp pulse period.

PROGRAMMING VSP3100

The VSP3100 consists of 3 CCD/CIS channels and a 14-bit A/D. Each channel (Red, Green, and Blue) has its own 10-bit Offset and 5-bit Gain Adjustable Registers to be programmed by the user. There is also an 8-bit Configuration Register, on-chip, to program the different operation modes. Those registers are shown in Table II.

ADDRESS A2 A1 A0	REGISTER	POWER-ON DEFAULT VALUE
0 0 0	Configuration Register (8-bit)	All "0s"
0 0 1	Red Channel Offset Register (10-bit)	All "0s"
0 1 0	Green Channel Offset Register (10-bit)	All "0s"
0 1 1	Blue Channel Offset Register (10-bit)	All "0s"
1 0 0	Red Channel Gain Register (5-bit)	All "0s"
1 0 1	Green Channel Gain Register (5-bit)	All "0s"
1 1 0	Blue Channel Gain Register (5-bit)	All "0s"
1 1 1	Reserved	

TABLE II. On-Chip Registers.

These registers can be accessed by the following two programming modes:

(1) Parallel Programming Mode using digital data output pins, with the data bus assigned as D0 to D9 (pins 25 to 34), and the address bus as A0 to A2 (pins 35 to 37). It can be used for both reading and writing operations. However, it cannot be used by the Demultiplexed mode (when D7 of the Configuration Register is set to "1").

(2) Serial Programming Mode using a serial port, Serial Data (SD), the Serial Shift Clock (SCLK), and Write Signal (WRT) assigned.

It can be used only for writing operations; reading operations via the serial port are prohibited.

Table III shows how to access these modes.

$\overline{OE}$	P/$\overline{S}$	MODE
0	0	Digital data output enabled, Serial mode enabled
0	1	Prohibit mode
1	0	Digital data output disabled, Serial mode enabled
1	1	Digital data output disabled, Parallel mode enabled

TABLE III. Access Mode for Serial and Parallel Port.

CONFIGURATION REGISTER

The Configuration Register design is shown in Table IV.

BIT	LOGIC '0'	LOGIC '1'
D0	CCD mode	CIS mode
D1	V_{REF} = 1V	V_{REF} =1.5V
D2	Internal Reference	External Reference
D3	3-channel Mode, D4 and D5 disabled	1-channel Mode, D4 and D5 enabled
D4,D5	(disabled when 3-channel)	**D4 D5** 0 0 1-channel mode, Red channel 0 1 1-channel mode, Green channel 1 0 1-channel mode, Blue channel
D6	MUX Sequence Red > Green > Blue	MUX Sequence Blue > Green >Red
D7	Normal output mode	Demultiplexed output mode

TABLE IV. Configuration Register Design.

Power-on default value is all "0s", set to 3-channel CCD mode with 1V internal reference, R > G > B MUX sequence, and normal output mode.

For reading/writing to the Configuration Register, the address will be A2 = "0", A1 ="0", and A0 = "0".

For Example:

A 3-channel CCD with internal reference V_{REF} = 1V (2V full-scale input), R > G > B sequence and normal output mode will be D0 = "0", D1 = "0", D2 ="0", D3 = "0", D4 = "x (don't care)", D5 = "x (don't care)", D6 = "0", and D7 = "0".

For this example, bypass V_{REF} with an appropriate capacitor (for example, 10µF to 0.1µF) when internal reference mode is used.

Another Example:

A 1-channel CIS mode (Green channel) with an external 1.2V reference (2.4V full-scale input), Demultiplexed Output mode will be D0 = "1", D1 = "x (don't care)", D2 = "1", D3 = "1", D4 = "0", D5 = "1", D6 = "x (don't care)", and D7 = "1".

For this example, V_{REF} will be an input pin applied with 1.2V.

OFFSET REGISTER

Offset Registers control the analog offset input to channels prior to the PGA. There is a 10-bit Offset Register on each channel. The offset range varies from –400mV to +400mV. The Offset Register uses a straight binary code. All "0s" corresponds to –400mV, and all "1s" corresponds to +400mV of the offset adjustment. The register code 200_H corresponds to 0mV of the offset adjustment. The Power-on default value of the Offset Register is all "0s", so the offset adjustment should be set to –400mV.

PGA GAIN REGISTER

PGA Gain Registers control the gain to channels prior to the digitization by the A/D converter. There is a 5-bit PGA Gain Register on each channel. The gain range varies from 1 to 4.44 (from 0dB to 13dB). The PGA Gain Register is a straight binary code. All "0s" corresponds to an analog gain of 0dB, and all "1s" corresponds to an analog gain of 13dB. PGA Transfer function is log gain curve. Power-on default value is all "0s", so that it sets the gain of 0dB.

OFFSET AND GAIN CALIBRATION SEQUENCE

When the VSP3100 is powered on, it will be initialized as a 3-Channel CCD, 1V internal reference mode (2V full-scale) with an analog gain of 1, and normal output mode. This mode is commonly used for CCD scanner applications. The calibration procedure is done at the very beginning of the scan.

To calibrate the VSP3100, use the following procedure:

1. Set the VSP3100 to the proper mode.
2. Set Offset to 0mV (control code: 00_H), and PGA gain to 1 (control code: 200_H).
3. Scan dark line.
4. Calculate the pixel offsets according to the A/D Converter output.
5. Readjust input Offset Registers.
6. Scan white line.
7. Calculate gain. It will be the A/D Converter full-scale divided by the A/D Converter output when the white line is scanned.
8. Set the Gain Register. If the A/D Converter output is not close to full-scale, go back to item 3. Otherwise, the calibration is done.

The calibration procedure is started at the very beginning of the scan. Once calibration is done, registers on the VSP3100 will keep this information (offset and gain for each channel) during the operation.

RECOMMENDATION FOR POWER SUPPLY AND GROUNDING

Proper grounding, bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multi-layer PC boards are recommended for the best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

It is recommended that analog and digital ground pins of the VSP3100 be joined together at the IC and connected only to the analog ground of the system. The VSP3100 has several analog supply pins (V_{CC}), so the VSP3100 should be treated as an analog component, and all supply pins should be powered by the analog supply on your system. This will ensure the most consistent results since digital supply lines often carry high levels of noise that would otherwise be coupled into the converter and degrade the achievable performance.

As the result of the high operation speed, the converter also generates high-frequency current transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently decoupled with ceramic capacitors.

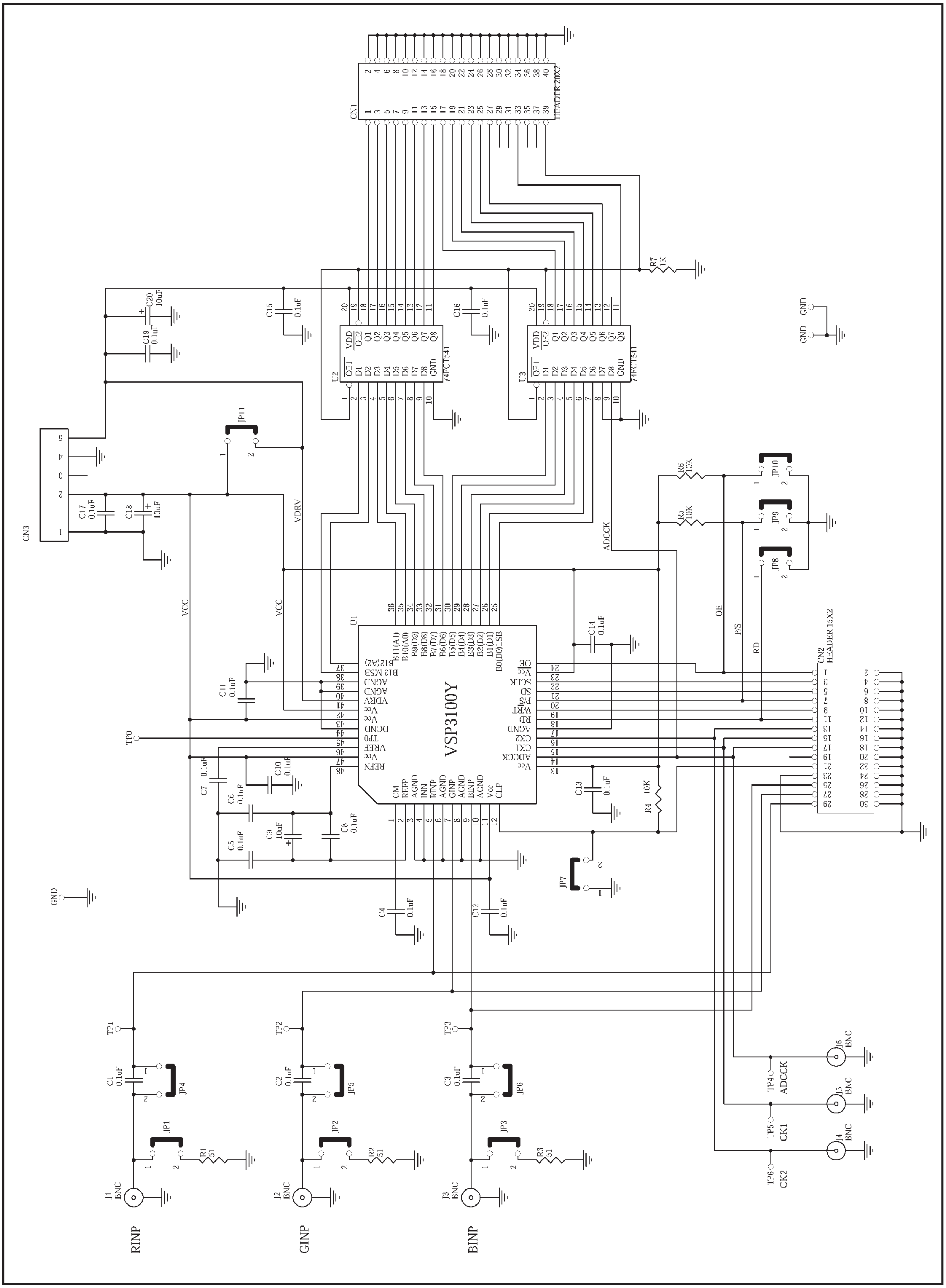


FIGURE 3. Demo Board Schematic (DEM-VSP3100).

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