Advance Product Information

VSC8120

2.488 Gbit/sec SONET/SDH Clock and Data Recovery IC

Features

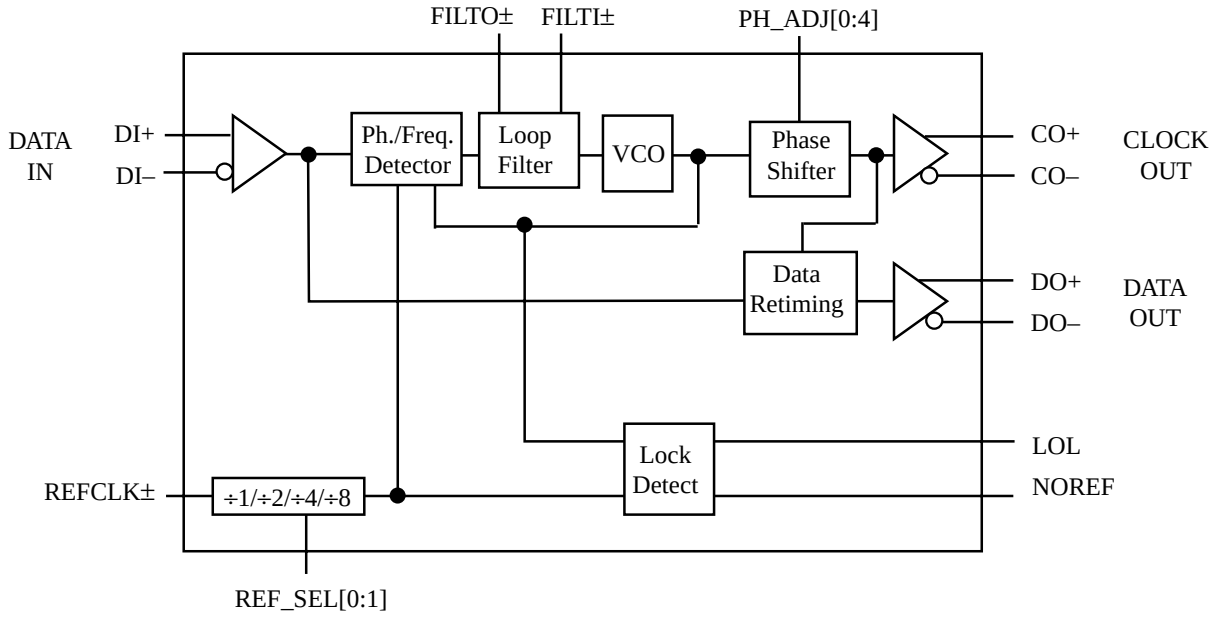
- 2.488 Gb/s Clock and Data Recovery
- SONET OC-48 / SDH STM-16
- Differential ECL I/O
- Maintains Clock Output in the Absence of Data
- Sampling Point can be Adjusted Within the Data Eye
- 10x10 mm PQFP Packaging

General Description

The VSC8120 is a single chip clock recovery IC for use in SONET OC48 and SDH STM16 systems operating at the 2.488Gb/s data rate. It complies with SONET jitter tolerance, jitter transfer and jitter peaking specifications.

Alarm functions support typical telecom system applications. The LOL output indicates when the device goes out of lock, which would most often occur in the event of a loss of valid data. The NOREF output flags when the reference input to the VSC8120 either is removed, or goes severely out of tolerance.

VSC8120 Block Diagram



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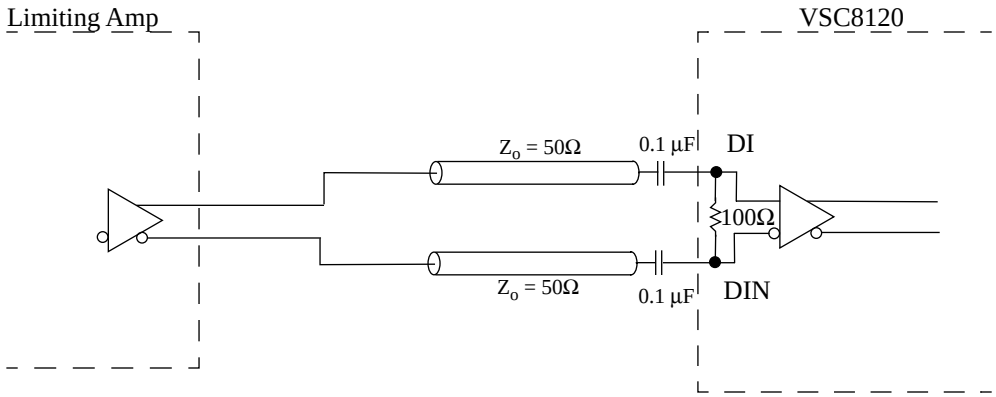
Functional Description

Data Input:

The data input receiver is internally terminated with a 100 ohm resistor between the true and complement inputs. The input requires a differential signal with a peak to peak voltage on both the true and complement of a minimum of 350mV. These inputs are recommended to be AC coupled to permit use with a variety of limiting amplifiers

Figure 1: Input Termination



Clock Recovery:

The incoming data is presented both to the clock recovery circuit and the data retiming circuit. When there is a phase error between the incoming data and the on-chip VCO, the loop filter raises or lowers the control voltage of the VCO to null the phase difference.

The lock detector monitors the frequency difference between the REF_CLK and the recovered clock. In the event of the loss of an input signal, or if the input is switching randomly, the VCO will move in one direction. At the time VCO and the REF_CLK differ by more than 1MHz from the 2.48832GHz rate, the lock detector will assert the LOL output. LOL is designed to be asserted from between 2.3us and 100us after the interruption of data. The VCO will continue to be locked at approximately 1MHz off of the REF_CLK based 2.48832GHz rate.

When NRZ data is again presented at the data input, the phase detector will permit the VCO to lock to the incoming data. Hysteresis is provided which delays the deassertion of LOL until approximately 160us following the restoration of valid data.

The NOREF output will go high to indicate that there is no signal on the REF_CLK input, or that the REFCLK is more than approximately 25% above or below the expected value.

Internally, the VSC8120 requires a 19.44MHz reference. The customer can select to provide either the 19.44MHz reference, or the 2x, 4x or 8x of that reference at 38.88MHz, 77.76MHz or 155MHz. The REF_SEL[0:1] inputs will program the internal divider as required to use the selected REF_CLK frequency.

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Table 1: Reference Frequency

Reference Frequency	*REF_SEL0*	*REF_SEL1*
19.44MHz	0	0
38.88MHz	1	0
77.76MHz	0	1
155.52MHz	1	1

Retiming:

The retiming decision circuit functions as a D Flip Flop. The recovered clock nominally clocks the decision circuit in the center of the data eye. Internally, the recovered clock can be adjusted by +/-UI/2 in steps of UI/32. The PH_ADJ[0:4] inputs select the phase of the clock that is used to retime the data. Certain lightwave systems employing optical amplifiers suffer from noise in the leading edge of the data eye. Therefore these systems may achieve their lowest Bit Error Rate (BER) by delaying the retiming point until later in the eye. These inputs can be strapped to generate a fixed delay or the customer can develop a dynamic circuit which can select the optimum retiming point during a training sequence. Refer to Table 2.

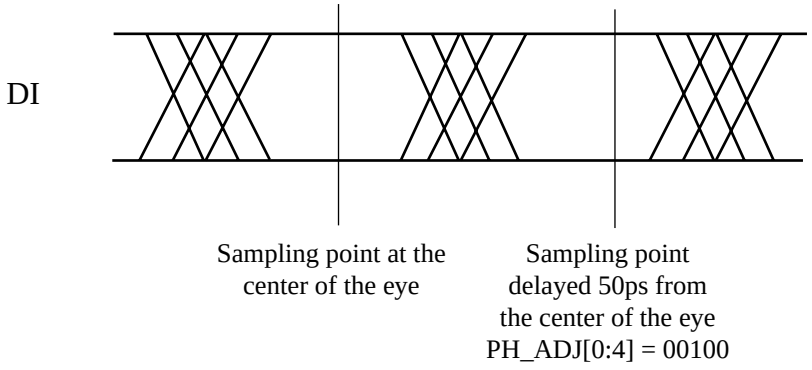
Table 2: Retiming Phase Adjust Settings

PH_ADJ4	*PH_ADJ3*	*PH_ADJ2*	*PH_ADJ1*	*PH_ADJ0*	*Degrees From Center*	*PS From Center*
0	0	0	0	0	0.00	0.0
0	0	0	0	1	11.25	12.6
0	0	0	1	0	22.50	25.1
0	0	0	1	1	33.75	37.7
0	0	1	0	0	45.00	50.2
0	0	1	0	1	56.25	62.8
0	0	1	1	0	67.50	75.4
0	0	1	1	1	78.75	87.9
0	1	0	0	0	90.00	100.5
0	1	0	0	1	101.25	113.0
0	1	0	1	0	112.50	125.6
0	1	0	1	1	123.75	138.2
0	1	1	0	0	135.00	150.7
0	1	1	0	1	146.25	163.3
0	1	1	1	0	157.50	175.8
0	1	1	1	1	168.75	188.4
1	0	0	0	0	180.00	201.0
1	0	0	0	1	-168.75	-188.4
1	0	0	1	0	-157.50	-175.8
1	0	0	1	1	-146.25	-163.3

Table 2: Retiming Phase Adjust Settings

PH_ADJ4	*PH_ADJ3*	*PH_ADJ2*	*PH_ADJ1*	*PH_ADJ0*	*Degrees From Center*	*PS From Center*
1	0	1	0	0	-135.00	-150.7
1	0	1	0	1	-123.75	-138.2
1	0	1	1	0	-112.50	-125.6
1	0	1	1	1	-101.25	-113.0
1	1	0	0	0	-90.00	-100.5
1	1	0	0	1	-78.75	-87.9
1	1	0	1	0	-67.50	-75.4
1	1	0	1	1	-56.25	-62.8
1	1	1	0	0	-45.00	-50.2
1	1	1	0	1	-33.75	-37.7
1	1	1	1	0	-22.50	-25.1
1	1	1	1	1	-11.25	-12.6

Figure 2: Retiming Offset



Loop Filter

The Phase Locked Loop on the VSC8120 employs an external loop filter. The PLL design is fully differential; therefore the loop filter must also be fully differential. One capacitor should be connected betweeen FILTO+ and FILTI+, with the other connected between FILTO- and FILTI-.

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AC Characteristics *(Over recommended operating conditions)*

Table 3: AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
t_{pd}	Center of output data eye from falling edge of CO+	-75	+75	ps	
t_r,t_f	DO± rise and fall times	—	150	ps.	20% to 80% into 50 Ohm load.
t_r,t_f	CO± rise and fall times	—	135	ps	20% to 80% into 50 Ohm load.

Figure 3: High Speed Clock and Data Outputs

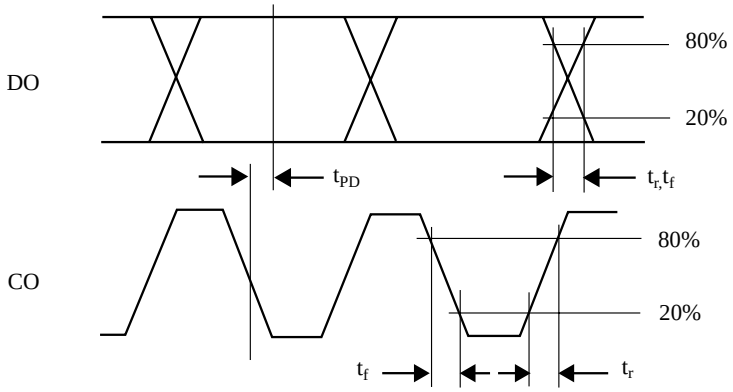

Table 4: High Speed ECL Inputs and Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔV_{OD}	Data Output voltage swing	450	—	1000	mV	
ΔV_{OC}	Clock Output voltage swing	450	—	1000	mV	
V_{DIFF}	Serial input absolute voltage differential peak-to-peak swing (DI±)	350		1200	mV	
V_{CM}	Input common mode range	-3.6		-3	V	
R_{IN}	Input Resistance between DI+ and DI-	80	100	120	Ohms	

Table 5: PLL Parameters

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
	REF_CLK Duty Cycle	45		55	%	
	REF_CLK Frequency Range	-100		+100	ppm	

DC Characteristics *(Over recommended operating conditions).*

Table 6: Low Speed ECL Inputs and Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1100	—	-700	mV	50 ohms to V_{TT}
V_{OL}	Output LOW voltage	V_{TT}	—	-1620	mV	50 ohms to V_{TT}
V_{IH}	Input HIGH voltage	-1040		-600	mV	
V_{IL}	Input LOW voltage	V_{TT}		-1600	mV	
I_{IH}	Input HIGH current			200	uA	
I_{IL}	Input LOW current	-50			uA	

Table 7: Power Supply

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{EE}	Supply voltage	-5.46	—	-4.94	V	
V_{TT}	Supply voltage	-2.1		-1.9	V	
P_D	Power dissipation	—		1.5	W	Outputs open
I_{EE}	Supply Current	—		tbd	mA	Outputs open
I_{TT}	Supply Current	—		tbd	mA	Outputs open

Absolute Maximum Ratings

Power Supply Voltage, (V_{EE}) ..... -7V to V_{CC}+0.5V
Power Supply Voltage, (V_{TT}) ..... -3V to 0.5V
DC Input Voltage (Differential inputs) ..... -2.5V to +0.5V
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C

Recommended Operating Conditions

Power Supply Voltage, (V_{EE}) ..... -5.2V±5%
Power Supply Voltage, (V_{TT}) ..... -2.0V±5%
Operating Temperature Range ..... 0^{o}C Ambient to $+85^{o}$C Case Temperature

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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Package Pin Descriptions

Figure 4: Pin Diagram

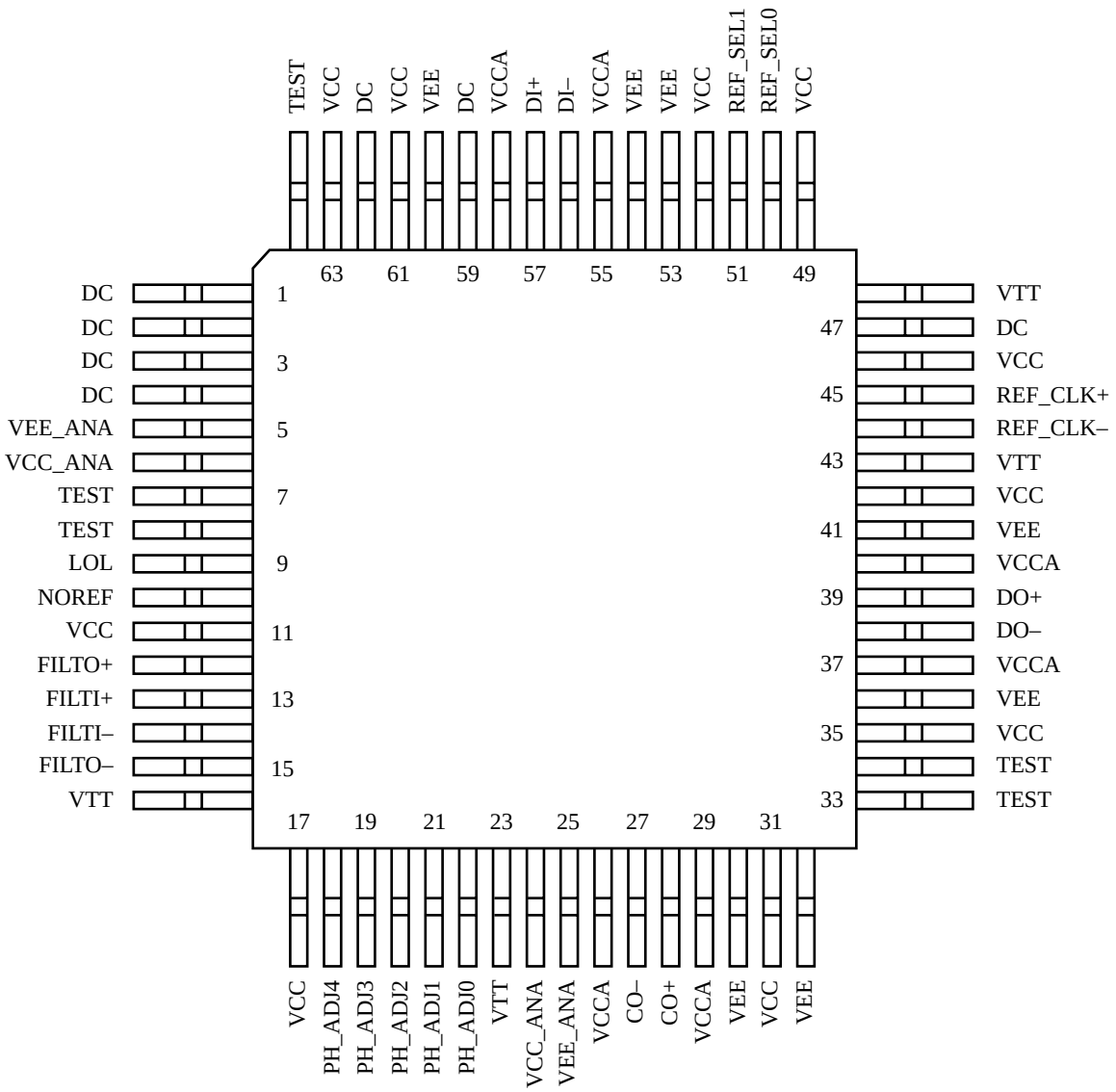

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Table 8: Pin Identification

Pin #	*Name*	*Description*
44,45	REF_CLK±	Differential reference clock input. ECL levels.
56,57	DI±	Data Input. Differential ECL levels
27,28	CO±	Differential high speed clock output. ECL levels
38,39	DO±	Differential retimed data output. ECL levels
18,19,20, 21,22	PH_ADJ[0:4]	Phase Adjust input, ECL levels. Internally biased to a logic “0” if left open.
50,51	REF_SEL[0: 1]	Selects between 19.44MHz, 38.88MHz, 77.76MHz or 155MHz for REFCLK
9	LOL	Loss of Lock output. Provides indication that the CRU has lost lock based on too few transitions in the incoming NRZ data. ECL levels.
10	NOREF	No Reference output. Goes HIGH to indicate REFCLK is far off of the expected frequency, or is not toggling. ECL levels.
12,13,14, 15	FILTO+/ FILTI+/ FILTO-/ FILTI-	Loop Filter pins
1,2,3,4,47, 59,62	DC	Don’t Connect, leave open
7,8,33,34, 64	TEST	Test Inputs, leave open
30,32,36, 41,53,54, 60	V_{EE}	Power Supply at -5.2V
5, 25	V_{EE_ANA}	Power Supply at -5.2V, for internal analog circuitry
16,23,43, 48	V_{TT}	Power Supply at -2.0V
11,17,31, 35,42,46, 49,52,61, 63	V_{CC}	Ground (0V)
26,29,37, 40,55,58	V_{CCA}	Ground (0V), for high speed inputs and outputs
6,24	V_{CC_ANA}	Ground (0V), for internal analog circuitry

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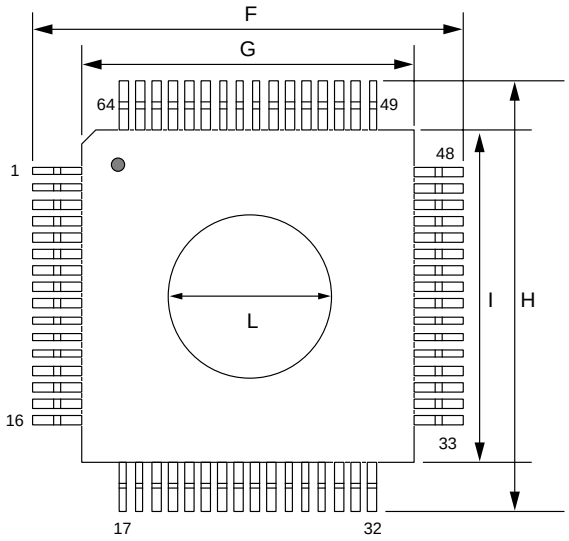
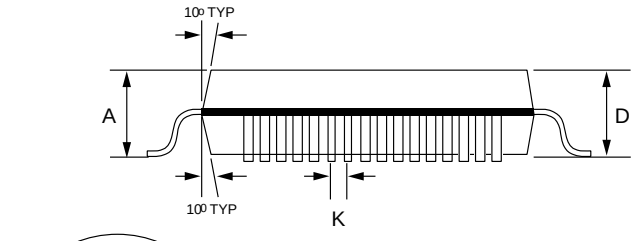
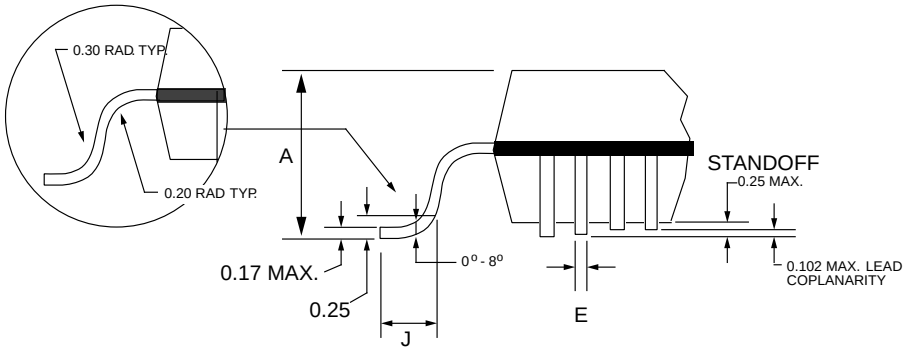
Package Information

64-pin PQFP Package Drawing



Item	*10 mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	±.15
K	0.50	BASIC





NOTES:
Drawing not to scale.
Heat spreader up on 10mm package only.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

Package #: 101-XXX-X
Issue #: 1

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Issue #: 1

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Notice

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