Preliminary Datsheet

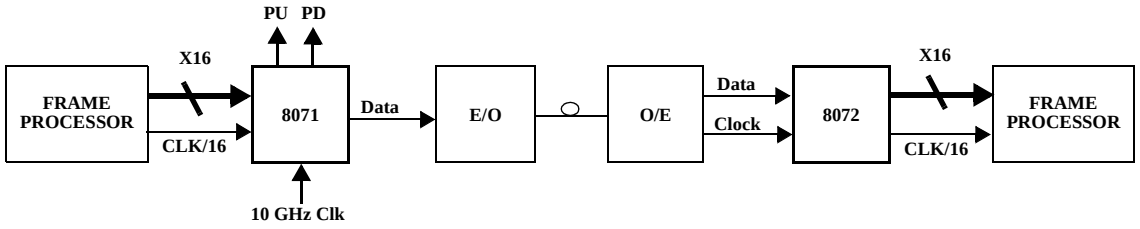
VSC8071/VSC8072

10 Gbits/sec 16-Bit Mux/Demux Chipset for STS-192 and STM-64 Applications

Features

- Performs 16:1, 1:16 Mux/Demux Between 10Gb/s High Speed Signal and 16 622Mb/s Low Speed Signals.
- Industry Standard -2.0V and -5.2V Power Supplies
- 50Ω Output Drive Capability and Impedance Matched Outputs
- Internal Input Terminations
- High Performance Module
- VSC8071 is a 16:1 10Gb/s Multiplexer with an Integrated Phase-frequency Detector
- VSC8072 is a 1:16 10Gb/s Demultiplexer

Typical System Block Diagram



General Description

The Vitesse 10Gb/s multiplexer/demultiplexer chipset is intended to perform serialization and de-serialization between 622Mb/s and 10Gb/s rate bit streams. The devices are packaged in a custom multilayer connectorized module to provide an environment compatible with 10GHz clock rates. The VSC8071/72 are first generation 10Gb/s devices. Please contact Vitesse regarding development plans for 10Gb/s products.

VSC8071 Functional Description

The VSC8071 10Gb/s multiplexer integrates a 16:1 multiplexer with synchronous timing control together with a phase detector. The phase detector can be used with an external loop filter and VCO to generate the bit rate clock.

The ECL compatible parallel data inputs (**D0...D15**) and parallel data rate clocks (**CLK16I/CLK16IN**) are provided with on chip 50 ohm terminations to V_{TT}. The bit rate clock (**CLKI**) input is internally terminated with a 50 ohm termination to V_{CC}. The serial data outputs (**DO, DON**) are back terminated with on-chip 100 ohm resistors. ECL compatible divided clock (**CLK16O/CLK16ON**) is provided and should be externally terminated with 50 ohm resistors to V_{TT}.

VSC8072 Functional Description

The VSC8072 10Gb/s demultiplexer integrates a 1:16 demultiplexer with synchronous timing control.

Serial data inputs (**DI/DIN**) and bit rate clock input (**CLKI**) are internally terminated with 50 ohm termination to V_{CC}. The deserialized data outputs (**Q0...Q15)** and divided clock (**CLK16O/CLK16ON**) are ECL compatible outputs and should be terminated in 50 ohms to V_{TT}.

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Figure 1: VSC8071 Functional Block Diagram

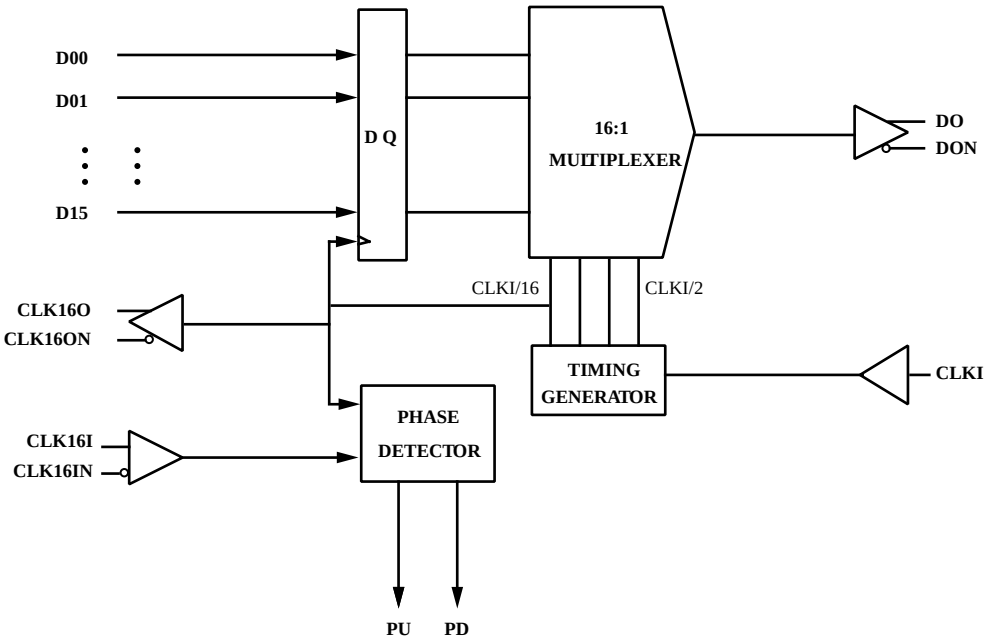

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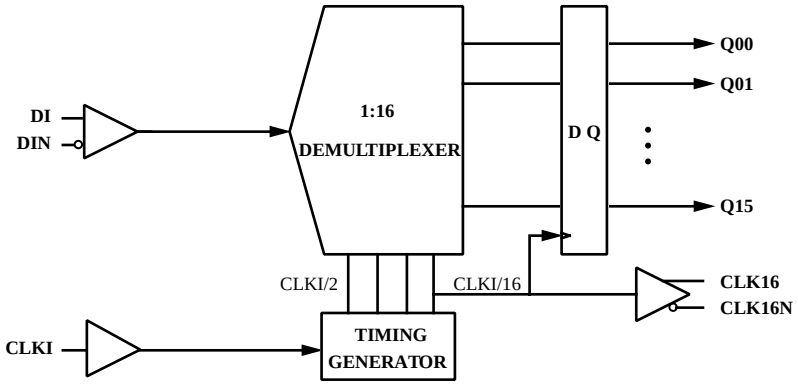
Figure 2: VSC8072 Functional Block Diagram



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VSC8071 AC Characteristics *(Over recommended operating conditions)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{DOR}, t_{DOF}	Serial data rise and fall time		50		pS	See figure 7.
t_{CLK16R}, t_{CLK16F}	CLK16O rise and fall times	-	200	350	pS	See figure 7.
t_{DS}	Data setup to CLK16O	TBD			pS	—
t_{DH}	Data hold from CLK16O	TBD			pS	—
t_{PE}	CLK16I to CLK16O delay		50		pS	Single ended CLK16I, PU/PD = zero on-chip phase error
t_{CLKI}	CLKI period		100		pS	See figure 4.
t_{CLK16I}	CLK16I period		1.6		nS	See figure 4.
V_{TM}	Threshold Margin	180			mV	
t_{PM}	Phase Margin	180			Deg.	
K_{PD}	Phase Detector Gain		140		mv/rad	1 radian ~ 16 ps

Figure 3: VSC8071 AC Timing Waveforms

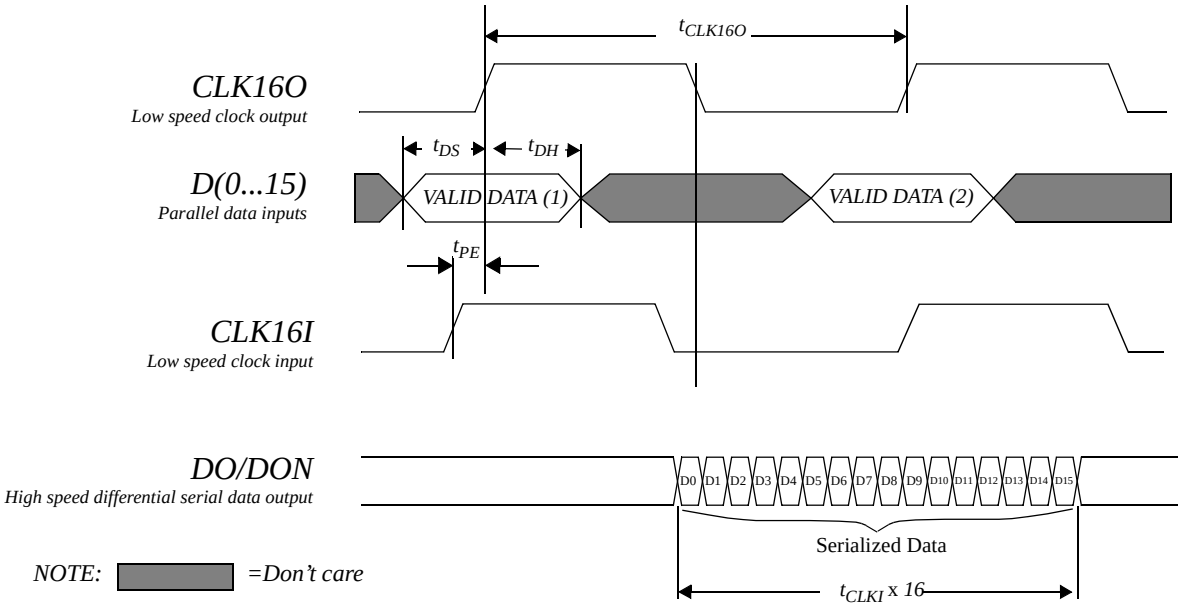

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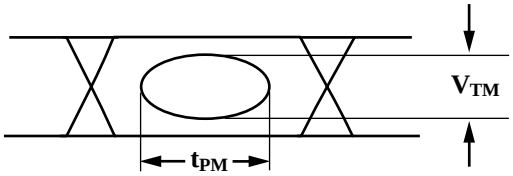
Figure 4: VSC8071 Output Data Eye



VSC8072 AC Characteristics *(Over recommended operating conditions)*

Parameters	*Description*	*Min.*	*Typ.*	*Max.*	*Units*	*Conditions*
t_{CLK16R}, t_{CLK16F}	CLK16 rise and fall times.		200	350	pS	See figure 7.
t_{QR}, t_{QF}	Parallel data out rise and fall time.		300		pS	See figure 7.
t_{PM}	Phase Margin	90	180		deg	at (2^{23} -1) PRBS
t_{QS}	Output data valid time before CLK16.	TBD			pS	—
t_{QH}	Output data valid time after CLK16.	TBD			pS	—
t_{CLK}	CLK period.		100		pS	—
V_{TM}	Threshold Margin	80	180		mV	

Figure 5: VSC8072 AC Timing Waveforms

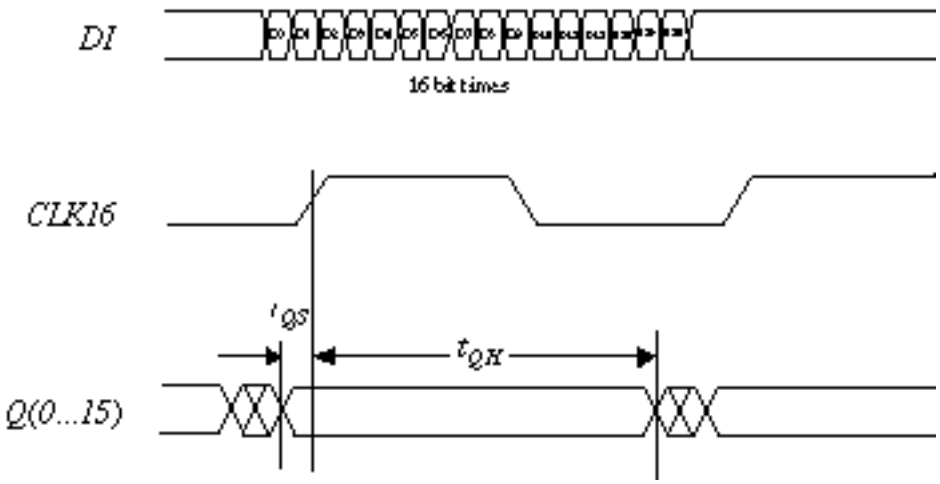


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Figure 6: VSC8072 Input Data Eye

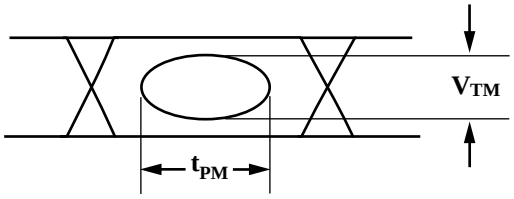

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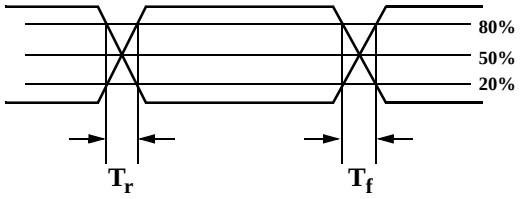
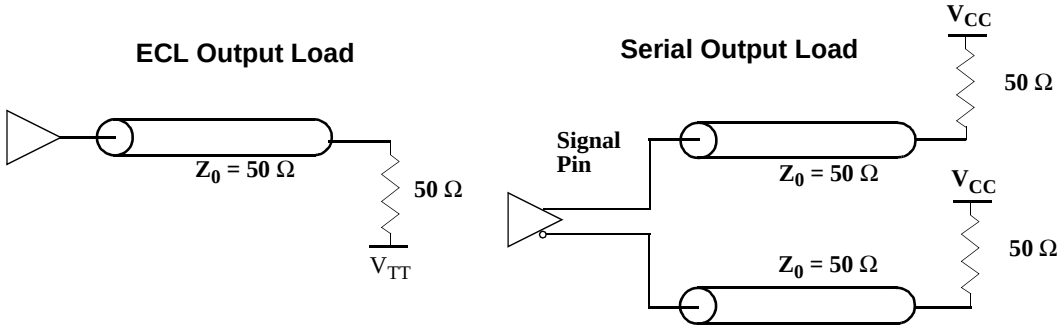
Figure 7: Parametric Measurement Information

Output Rise and Fall Time



Parametric Test Load Circuit



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DC Characteristics *(Over recommended operating conditions)*

Table 1: ECL Inputs/Outputs.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1100	—	-700	mV	50Ω to V_{TT} Load
V_{OL}	Output LOW voltage	V_{TT}	—	-1620	mV	50Ω to V_{TT} Load
V_{IH}	Input HIGH voltage	-1165	—	-700	mV	
V_{IL}	Input LOW voltage	V_{TT}	—	-1475	mV	
I_{IH}	Input HIGH current	—	—	32	mA	V_{IN} = -700mV, V_{TT} = -2.1 V
I_{IL}	Input LOW current			9	mA	V_{IN} = -1750mV, V_{TT} = -2.1 V

Table 2: High-Speed Outputs (VSC8071)

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-200	-100	0	mV	External 50Ω to $\mathbf{V_{CC}}$
V_{OL}	Output LOW voltage	-1100	-900	-750	mV	External 50Ω to $\mathbf{V_{CC}}$
I_{OL}	Output Low Current			23	mA	—
I_{OH}	Output High Current			3	mA	—

Note: 1) DC Characteristics of high speed outputs apply at effective output rates of 100 MHz or less.

Table 3: High-Speed Data Inputs (VSC8072)

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ýV_{IN}	Amplitude	1.0		2.0	V	
V_{IN}	Input Voltage	-2.0	-0.5	0.5	V	
R_{TERM}	Termination Resistor	40	50	60	Ohms	

Table 4: High-Speed Clock Inputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔV_{IN}	Input Swing - single ended	0.6	0.75	2.0	V	—
V_{INDC}	DC Value of CLKI	-1.8		+1.8	V	
R_{TERM}	Termination Resistor	40	50	60	Ohms	

Table 5: Power Dissipation

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{EE}	Supply Current - VSC8071	—	850		mA	V_{EE} = V_{EE} min, apply only to IEE max
I_{EE}	Supply Current - VSC8072	—	650		mA	

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Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{TT}	Termination Current - VSC8071	—		570	mA	$V_{TT} = V_{TT}$ min, ECL Inputs High apply only to ITT max
I_{TT}	Termination Current - VSC8072	—		50	mA	
P_D	Power Dissipation - VSC8071	—	5		W	$V_{EE} = V_{EE}$ min, $V_{TT} = V_{TT}$ min, ECL Inputs High apply only to PD max
P_D	Power Dissipation - VSC8072	—	4		W	

Absolute Maximum Ratings (1)

ECL Power Supply Voltage, (V_{EE}) ..... -7.0 V to +0.7 V
V_{TT} - Termination Voltage (ECL Inputs) ..... -2.5 V to +0.5 V
V_{TT} - Termination Voltage (CLKI) ..... -2.5 V to +0.5 V
DC Input Voltage (Low-speed inputs) ..... V_{TT} - 2.5 V to +0.5 V
DC Input Voltage, (CLKI) ..... V_C - 2.0 V to V_C +2.0 V
DC Input Voltage, (DI) ..... -2.5 V to +0.5 V
Case Temperature Under Bias ..... -55^o to $+125\ ^oC$
Storage Temperature ..... $-65\ ^oC$ to $+150\ ^oC$

Recommended Operating Conditions

Power Supply Voltage, (V_{EE}) ..... -5.2V to -5.5V
Termination Supply Voltage, (V_{TT}) ..... -2.0V ± 5%
Operating Temperature Range, (T) (2) ..... $0\ ^oC$ to $+\ 70\ ^oC$

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.
(3) CAUTION: Do not apply V_{TT} prior to V_{EE}

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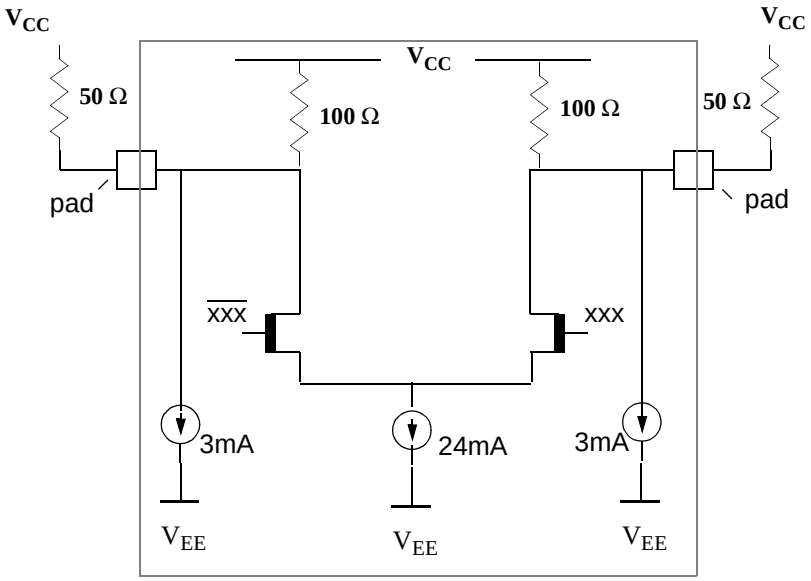
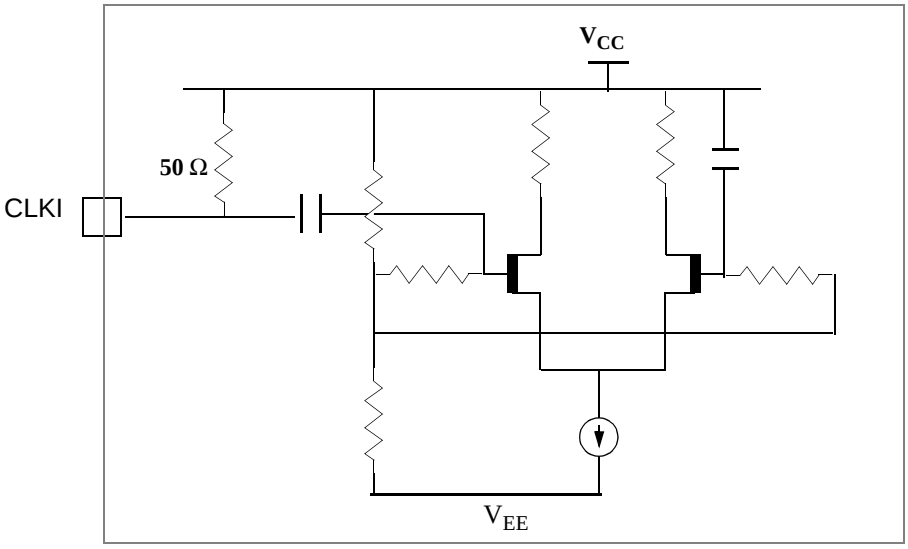
Figure 8: IO Structures



MUX High-Speed Output Buffer



High-Speed Clock Input Buffer

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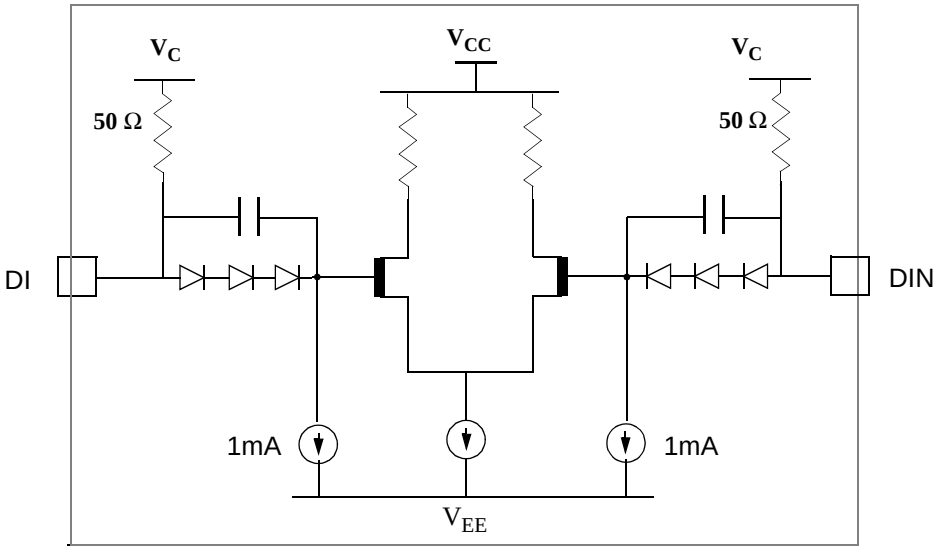
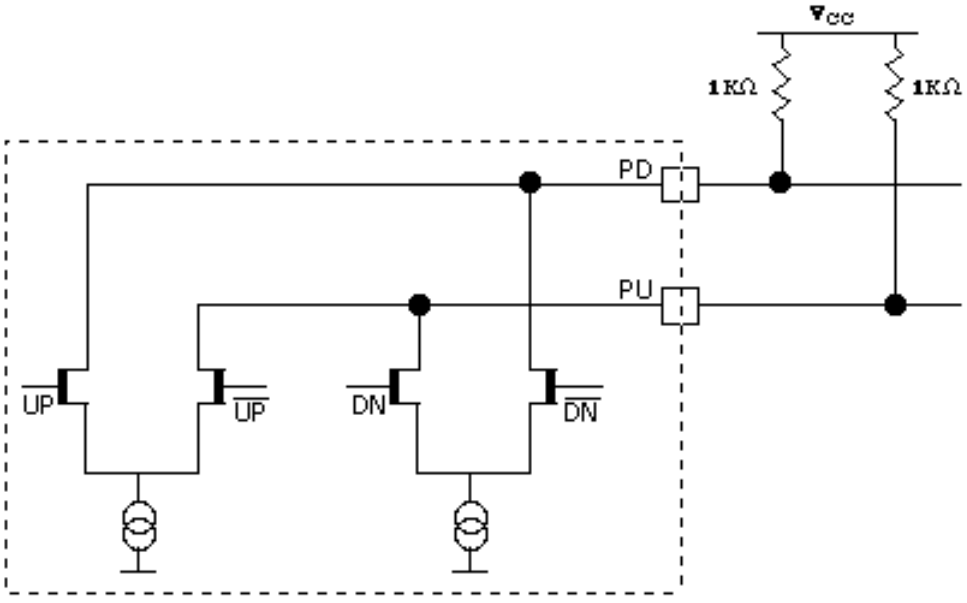
Figure 9: IO Structures Cont.



DMUX High-Speed Data Input Buffer



MUX Phase-Detector Outputs

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Package Pin Descriptions

Table 6: VSC8071 Pin Description

Name	*Description*
D00:15	INPUT -ECL Parallel data presented to this port is clocked into the device. The timing of this data is relative to the CLK16O output.
CLKI	INPUT - HIGH SPEED CLOCK Bit rate input clock. This clock is terminated in 50 Ohms to V_C, and is AC coupled on-chip.
V_C	POWER SUPPLY Common mode termination voltage for CLKI inputs. (Typically grounded)
CLK16I, CLK16IN	INPUT- DIFFERENTIAL ECL Parallel data rate clock.
DO, DON,	OUTPUT - DIFFERENTIAL HIGH SPEED Serial data output stream. DO and DON should be terminated with 50 Ohms to ground at the load.
CLK16O, CLK16ON	OUTPUT - DIFFERENTIAL ECL This is the bit rate clock divided by 16.
PU, PD	OUTPUT - ANALOG Phase detector outputs.
V_{CC}	GROUND
V_{EE}	POWER SUPPLY (-5.2 V NOM.)
V_{TT}	POWER SUPPLY (-2.0 V NOM.) Termination supply for ECL inputs.
Vbb	ECL Reference Voltage (typ. -1.32V)

Table 7: VSC8072 Pin Description

Name	*Description*
DI, DIN	INPUT - HIGH SPEED DIFFERENTIAL (HS) Serial data input stream. These inputs are internally terminated. If a single ended signal is used the other input should be capacitively de-coupled to $\mathbf{V_{CC}}$.
CLKI	INPUT - HIGH SPEED CLOCK (HS) Bit rate clock input.
V_C	POWER SUPPLY Common mode termination voltage for CLKI input. (Typically grounded)
Q00:15	OUTPUT - ECL De-serialized data outputs. The outputs are updated at 1/16 of the bit rate.
CLK16, CLK16N	OUTPUT - DIFFERENTIAL ECL This is the bit rate clock divided by 16.
V_{CC}	GROUND
V_{EE}	POWER SUPPLY (-5.2 V NOM.)
V_D	POWER SUPPLY Common mode termination voltage for DI,DIN inputs. (Typically grounded)

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Table 8: Package Pin Table

PIN #	*VSC8071*	*VSC8072*	*PIN #*	*VSC8071*	*VSC8072*	*PIN #*	*VSC8071*	*VSC8072*
1	Gnd	Gnd	17	D10	Q05	33	D00	Q15
2	Vc	Vc	18	D09	Q06	34	Vee	Vee
3	Vd	Vd	19	D08	Q07	35	Clk16i	NC
4	Gnd	Gnd	20	Gnd	Gnd	36	Vtt	Vcca
5	Vbb	NC	21	Vtt	Vcca	37	Clk16in	NC
6	Clk16o	Clk16on	22	Vee	Vee	38	Pd	Pd
7	Vtt	Vcca	23	Gnd	Gnd	39	Pu	Pu
8	Clk16on	Clk16	24	D07	Q08	40	Vc01*	Vc01*
9	Vee	Vee	25	D06	Q09	41	Vc02*	Vc02*
10	D15	Q00	26	D05	Q10	42	Gnd	Gnd
11	D14	Q01	27	D04	Q11			
12	D13	Q02	28	Gnd	Gnd			
13	D12	Q03	29	Vee	Vee	RF1	NC	NC
14	Vee	Vee	30	D03	Q12	RF2	CLKI	CLKI
15	Gnd	Gnd	31	D02	Q13	RF3	DO	DIN
16	D11	Q04	32	D01	Q14	RF4	DON	DI

Notes:
*(1) *Not Currently Implemented*

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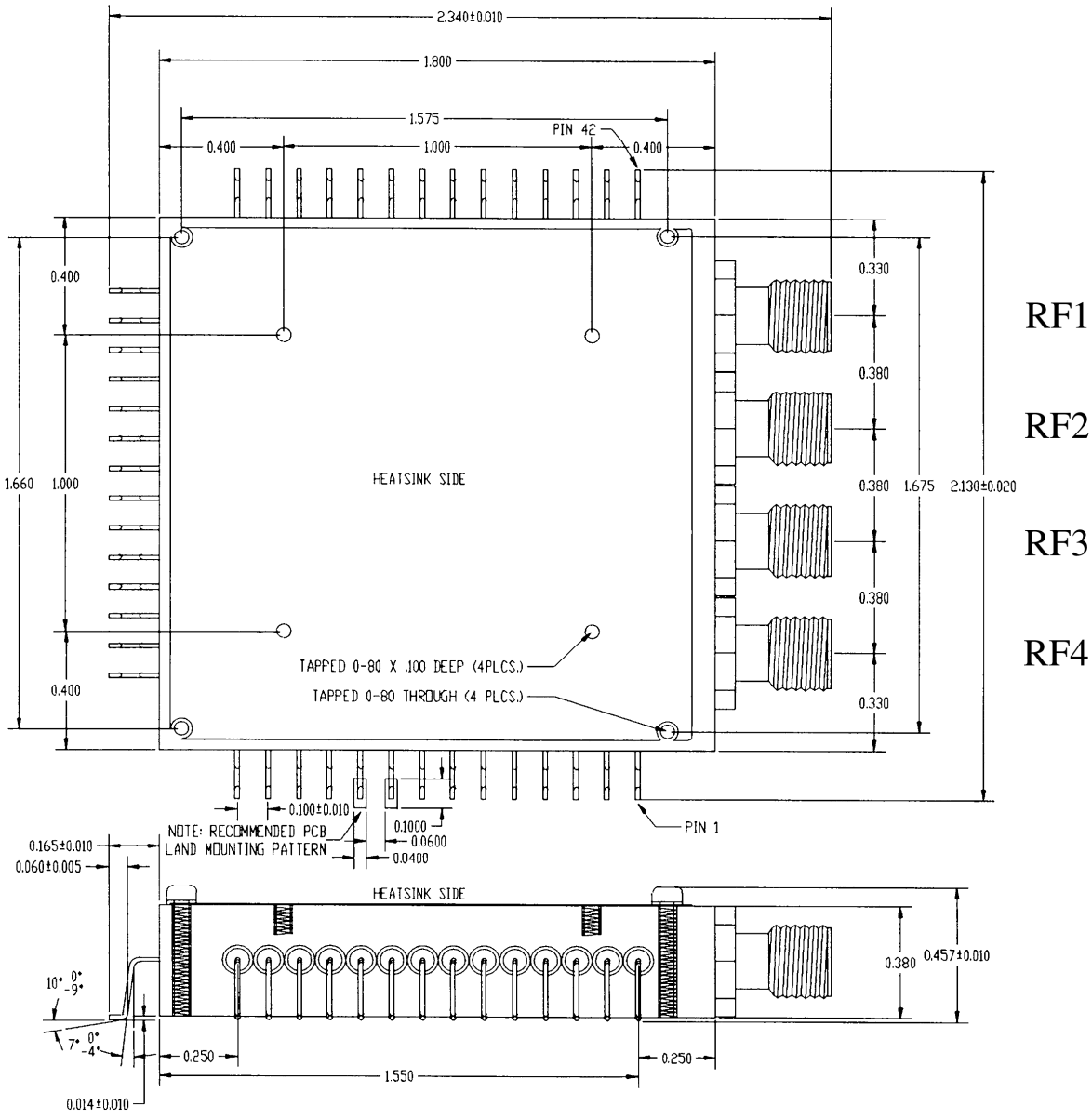
Package Information *(BAL Lead Formed Version)*



Notes: 1) BA straight lead version has leads 0.015 in diameter 0.32 long with a center line 0.191 from the heat sink side.
2) Dimensions are in inches.

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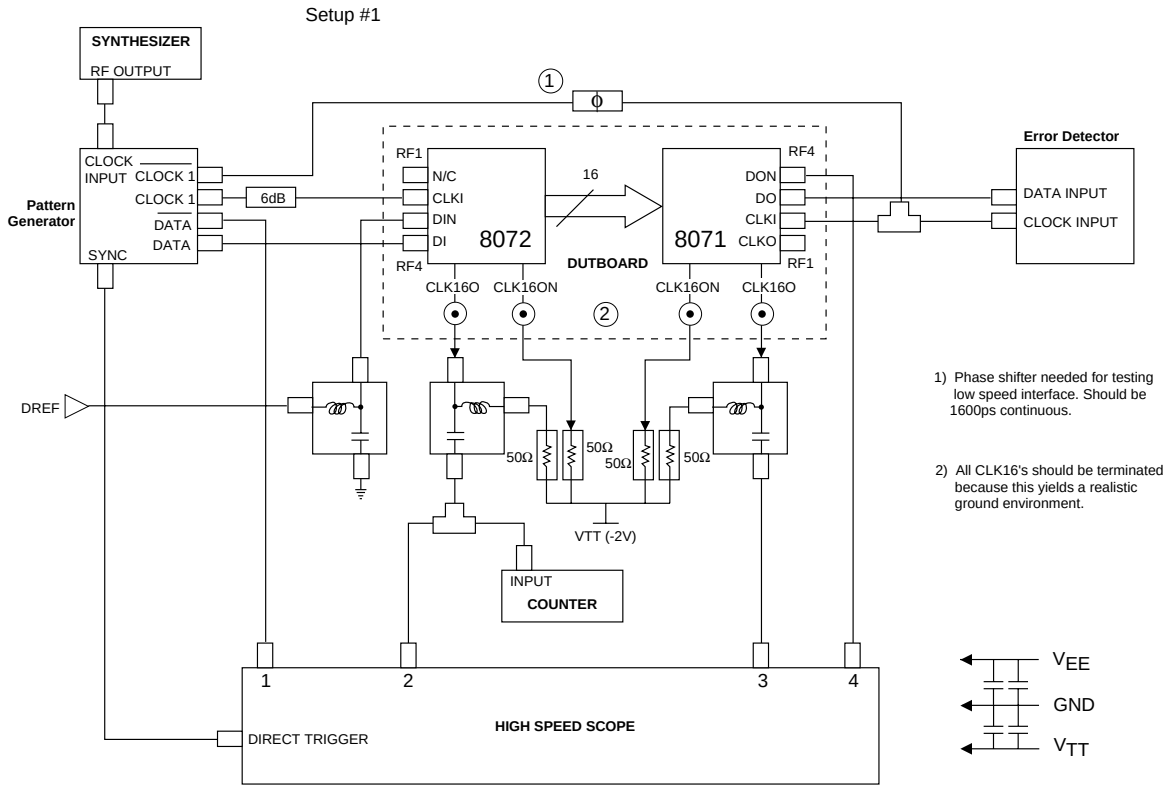
Figure 10: Setup #1 Typical Test Configuration



TYPICAL TEST CONFIGURATION

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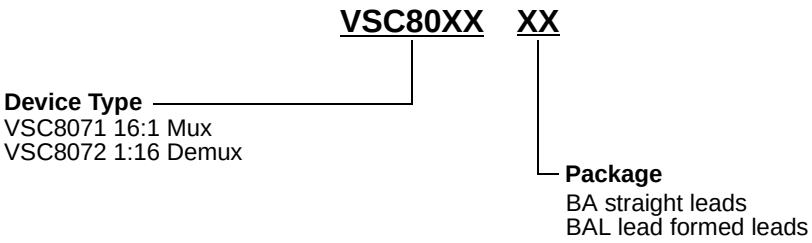
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Notice

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