

## ***Product Bulletin***



### **VM10LA Series 10 Gb/s Receiver Limiting Amplifier**

These rugged, low-cost, high performance receiver amplifiers utilize single-substrate COPLANAR MIC thin-film technology and state-of-art GaAs active devices. Designed for receiver applications, these products produce a “quantized” output, effectively providing the decision circuit for the receiver.

Optional threshold symmetry adjustments allows BER optimization at minimum input level. EYE diagrams exhibit very large phase and amplitude margin even when the input (usually from a PD/TZ amplifier) is “dirty”. The output level is electrically adjustable. Output rise and fall times at nominal 50 mVpp input approach 25 ps.

Pulse parameters such as rise and fall times and EYE opening at 10 Gb/s are guaranteed. Supplied with removable DC shells and SMA-F RF connectors.

#### **Key features**

- Advanced GaAs technology
- Inputs from 15 to 1500 mV produce constant output
- Optional threshold symmetry adjustment (suffix TO)
- Low noise figure for excellent BER at lowest inputs
- Adjustable output voltage, Vp-p
- Rise and fall times < 30 ps
- Guaranteed EYE and step responses
- Internal DC regulation, protection
- Small package

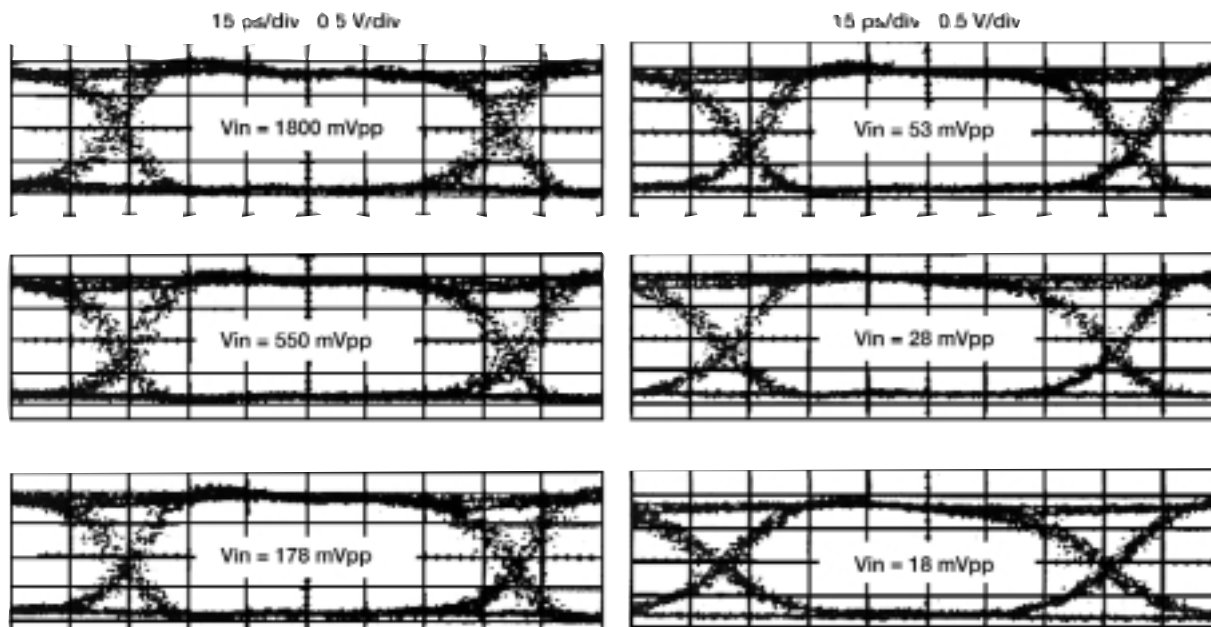
#### **Applications**

- 10 Gb/s receiver electronics for low-cost, high reliability fiberoptic communication system
- High speed data links

## Typical Performance of VM10CDS-180

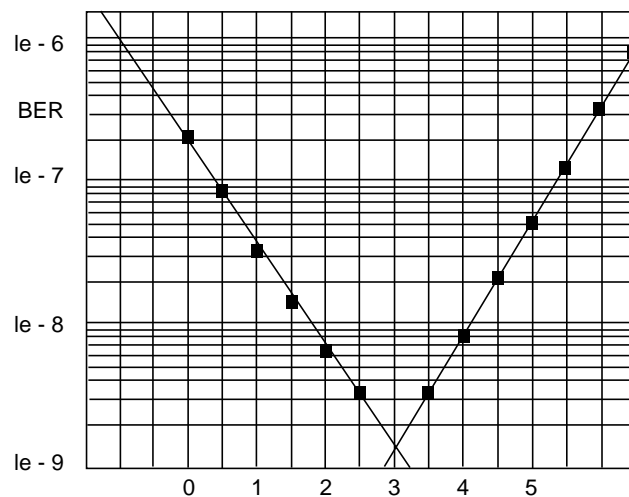
### Typical Output EYES

Input varied from 18 mVpp to 1800 mVp-p. Input is  $(2^{31} - 1)$  word, 10 Gb/s. Note large phase margins, typically 60% of bit width. EYE opening near 100% at center of bit; good crossover symmetry over 40 dB input range. Sampling scope 10 S persistence, 12.5 GHz BW.



### BER vs. Threshold Control

Duty cycle: 55%, PRBS word:  $2^{31} - 1$ , Input level: Minimum



## 10 Gb/s Receiver Limiting Amplifier Performance Specifications

Model # VM10LA - xxx*	V <sub>in</sub> , p-p mV	Gain dB <sup>1</sup>	V <sub>o</sub> , p-p Volts <sup>2</sup>	Tr, Tf pS MAX <sup>3</sup> V1 V2		I <sub>dc</sub> MAX/TYP mA @+15V
- 145	20-1500	44	1.6 (min.)	38	29	400/320
- 155	15-1500	50	1.6 (min.)	38	29	450/360
*Add "- TO" suffix to specify threshold adjustment option.						

### Notes

1. Small-signal gain at 25°C, MIN
2. -3 dB adjustability from V<sub>out</sub> MAX, for all input voltages
3. Rise/fall times from 10-90% at MIN. (V1) and MAX. (V2) input level.

### Other Specifications

- Minimum EYE opening 85% at 10 Gbps
- NF < 8 dB
- Crossover asymmetry ±20% MAX
- S<sub>11</sub> < -10 dB from 400 kHz to 8 GHz; S<sub>22</sub> < -10 dB from 100 kHz to 6 GHz
- Output port is DC blocked to ±10 V. MAX input level 2 V<sub>p-p</sub>
- DC requirement +15 V (internal regulation)
- Reverse voltage protection 50 V
- Output level control terminal: 0 to +12 V at 5 mA MAX; V<sub>o</sub> largest at +12V
- Frequency response from 100 kHz (MAX) to 10 GHz (MIN), saturated

### Mechanical Data

Aluminum 6061-T6, nickle plate. RF (SMA-F) and DC shells. Shell removal exposes .015" diameter pin. Heat removal through case (conduction). Wire harness/connector available.

### Reliability

High reliability screening, visual inspections and other screening per VMI Level III, including centrifuge, burn-in, temperature cycle, seal and final test are optional at extra cost.

### Factory Testing Technique

Pattern generator with 25 ps rise/fall time, 10 Gbs/s (NRZ), fixed 2.0 V<sub>p-p</sub> output. Variable attenuator. Sampling oscilloscope with 12 GHz bandwidth (29 ps). Input to DUT is (2<sup>31</sup> - 1) word length. Correct observed Tr, Tf for system speed, using sum of squares rule.

### Threshold Adjust Option

Apply +5 to -5 V DC at < 10 mA to "TA" pin to optimize system BER at the lowest input level specified. Polarity depends upon system configuration; improvement of 2-3 orders of magnitude in BER are typical, or about 1.5 dB in input level threshold for specified BER.

