VLSI Technology

ViSTA VES1820

Single-Chip DVB-C Continuously Variable Cable Channel Receiver

OVERVIEW

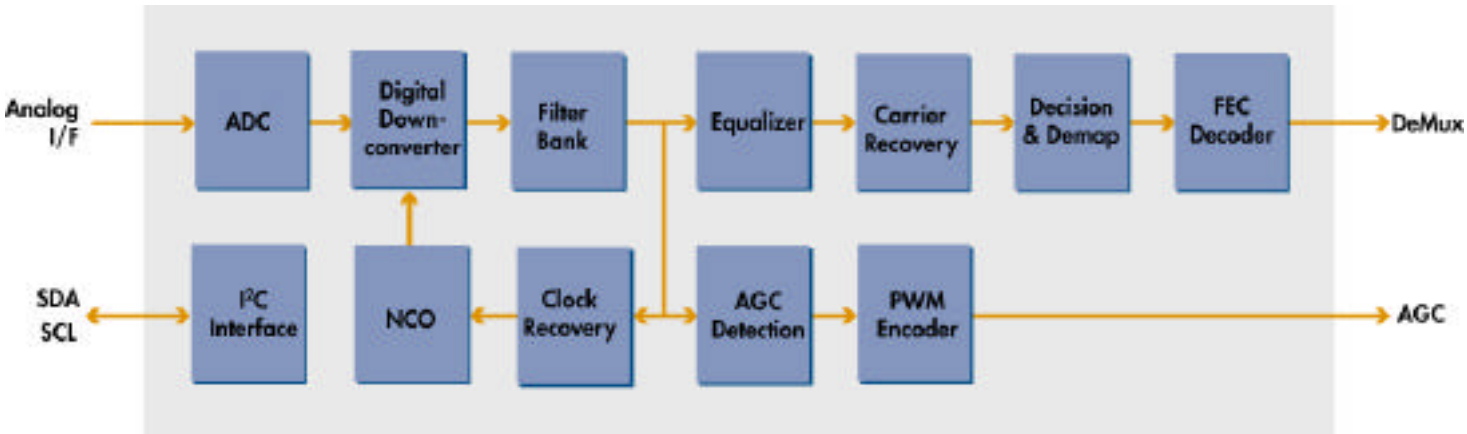
The ViSTA VES1820 integrates all features of its predecessor ViSTA VES1520 (DVB-C compliant Digital Cable Receiver) combined with a direct IF interface and 9-bit ADC (Analog to Digital Converter) on a single chip. The ViSTA VES1820 is a fully contained digital cable channel receiver for digitally transmitted DVB-C compatible signal format. The VES1820 is based on VLSI's industry leading Integrated Set-Top Architecture (ViSTA)

The VES1820 is a single chip channel receiver for 16, 32, 64, 128, and 256-QAM modulated signals. The device interfaces directly to the IF output of a tuner, and provides on-chip analog to digital conversion plus digital demodulation and error correction. Demodulation symbol rates are variable from 0.87-8.7 MBaud and are achieved using an external fixed crystal frequency. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the specific application.

Equalization filters can be configured as either T-spaced transversal equalizer or DFE type, so that the system performance can be optimized according to the network characteristics.
A proprietary equalization algorithm is provided to achieve carrier recovery independent of carrier offset. Next, a decision directed algorithm takes place to achieve final equalization convergence.

The VES1820 implements a FORNEY convoluted deinterleaver of depth 12 and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The deinterleaver and the RS decoder are automatically synchronized to the frame synchronization algorithm that uses the MPEG2 sync byte. Finally, descrambling according to the DVB-C standard is achieved at the Reed-Solomon output. This device is controlled via an I²C bus.

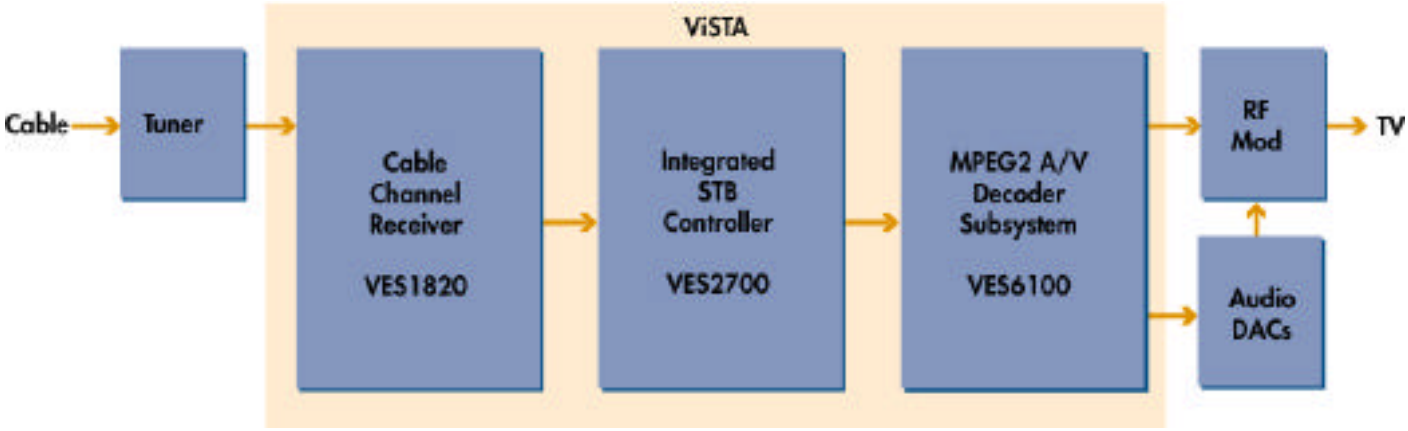
Block Diagram



FEATURES

- 16/32/64/128/256 QAM demodulator
- 9-bit ADC
- Digital 9-bit bandpass input signal
- Digital down conversion (direct IF sampling)
- Half-Nyquist filters (roll off = 15%)
- Automatic gain control (AGC) Post Width Modulation output
- DC offset compensation
- Symbol timing recovery, with programmable second order loop filter
- Variable rate capability: SACLK/64 to SACLK/4 (SACLK max = 36 MHz)
- Full digital carrier recovery loop
- Carrier acquisition range up to 7% of symbol rate
- Integrated adaptive equalizer (Transversal or DFE equalizer)
- On-chip FEC decoder (Deinterleaver & RS decoder), full DVB-C compliant
- DVB compatible differential coding and mapping
- I^2C bus interface, for easy control
- 100 MQFP package
- 0.35 µm CMOS technology

Typical Application



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