StaticGuard

AVX Multilayer Ceramic Transient Voltage Suppressors
ESD Protection for CMOS and Bi Polar Systems

GENERAL INFORMATION

- Typical ESD failure voltage for CMOS and/or Bi Polar is ≥ 200V.
- 15kV ESD pulse (air discharge) per IEC 1000-4-2, Level 4, generates < 20 millijoules of energy.
- Low capacitance (<200pF) is required for high-speed data transmission.
- Low leakage current (I_L) is necessary for battery operated equipment.

PART NUMBER IDENTIFICATION (See page 2 for details)

Chips

V C 08 LC 18 A 500 R P

- **TERMINATION FINISH:** X = Pt/Pd/Ag (Non-Plated), P = Ni/Sn Alloy (Plated)
- **PACKAGING (Pcs/Reel)**
- **CLAMPING VOLTAGE**
- **ENERGY RATING**
- **WORKING VOLTAGE (0-18V)**
- **LOW CAPACITANCE DESIGN**
- **CASE SIZE DESIGNATOR**
- **CASE STYLE**
- **PRODUCT DESIGNATOR**

Axials

V A 10 LC 18 A 500 R L

- **LEAD FINISH:** L = Copper Clad Steel, Solder Coated
- **PACKAGING (Pcs/Reel)**
- **CLAMPING VOLTAGE**
- **ENERGY RATING**
- **WORKING VOLTAGE (0-18V)**
- **LOW CAPACITANCE DESIGN**
- **CASE SIZE DESIGNATOR**
- **CASE STYLE**
- **PRODUCT DESIGNATOR**

AVX Part Number	Working Voltage	Clamping Voltage	Peak Current	Transient Energy	Capacitance	Inductance
Symbol	V_{WM}	V_C	I_{peak}	E_{trans}	C	L
Units	Volts (max.)	Volts (max.)	Amp (max.)	Joules (max.)	pF (typ.)	nH (typ.)
Test Condition	<10µA	8/20µS†	8/20µs	10/1000µS	0.5Vrms @: 1 MHz	di/dt = 100mA/ns
VC04LC18V500 _ _	See specifications on page 3 and performance data on page 4.					
VC06LC18X500 _ _	≤18.0	50	20	.05	75	<1.0
VC08LC18A500 _ _	≤18.0	50	30	0.1	100	<1.5
VC12LC18A500 _ *	≤18.0	50	30	0.1	200	<1.7
VA10LC18A500 _ L	≤18.0	50	30	0.1	200	<3.5

Termination Finish: X = Pt/Pd/Ag (Non-Plated)
P = Ni/Sn Alloy (Plated)
* = Contact Factory for Availability
Lead Finish: L = Copper Clad Steel, Solder Coated
Packaging (Pcs/Reel): see page 2

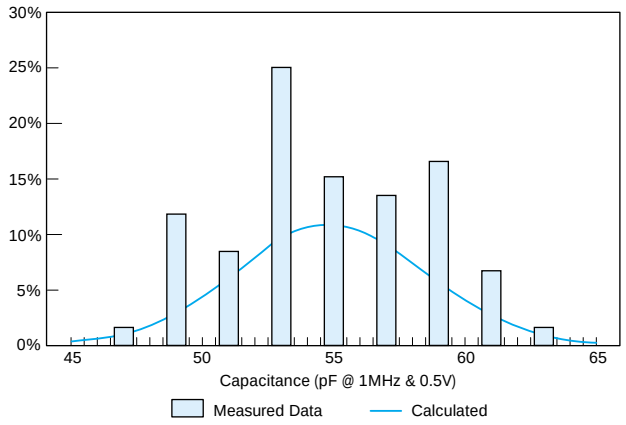
V_{WM}—Maximum steady-state DC operating voltage the varistor can maintain and not exceed 50µA leakage current
V_C—Maximum peak voltage across the varistor measured at a specified pulse current and waveform

†Transient Energy Rating	Pulse Current & Waveform
<0.05 Joule	1A 8/20µS
0.1 Joule	2A 8/20µS

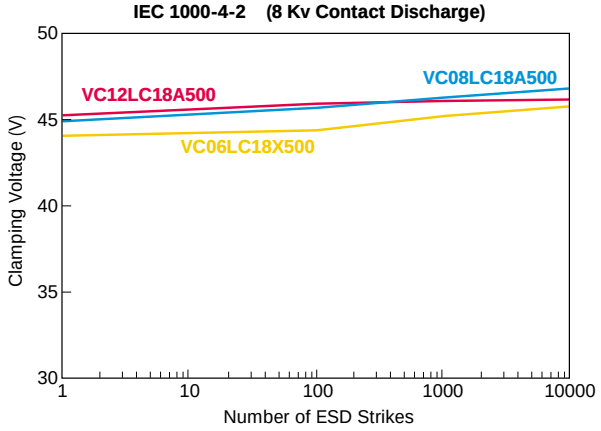
I_{peak}—Maximum peak current which may be applied with the specified waveform without device failure
E_{tran}—Maximum energy which may be dissipated with the specified waveform without device failure
C—Device capacitance measured with zero volt bias 0.5Vrms and 1MHz
L—Device inductance measured with a current edge rate of 100 mA/nS
Dimensions: Millimeters (Inches)

TYPICAL PERFORMANCE DATA

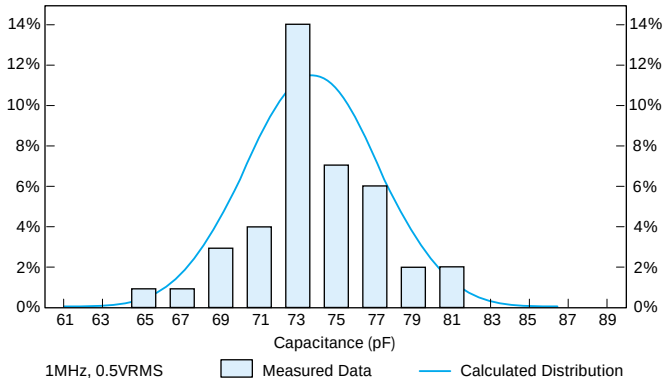
VC06LC18X500 Capacitance Histogram



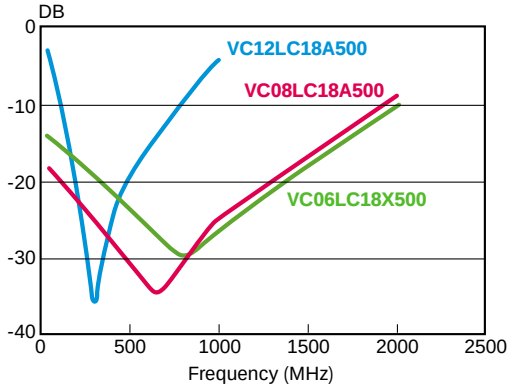
StaticGuard ESD RESPONSE
IEC 1000-4-2 (8 Kv Contact Discharge)



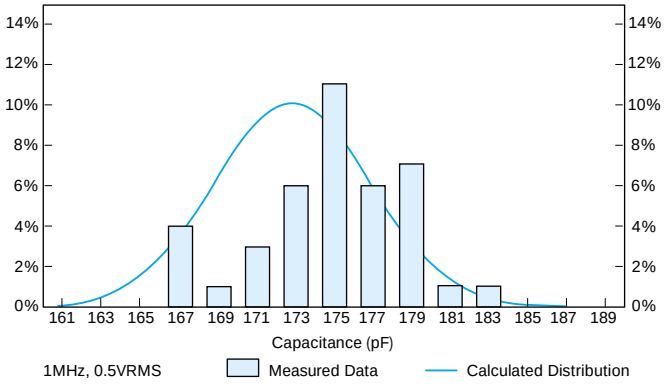
VC08LC18A500 Capacitance Histogram



StaticGuard S21



VC12LC18A500 Capacitance Histogram



VI Curves - StaticGuard Products