Advance Product Information

VSC7924

SDH/SONET 2.5Gb/s
Laser Diode Driver

Features

- Rise Times Less Than 100ps
- High Speed Operation (Up to 2.5Gb/s NRZ Data)
- Single-ended Operation
- Single Power Supply
- Direct Access to Modulation and Bias FET's
- Data Density Monitors

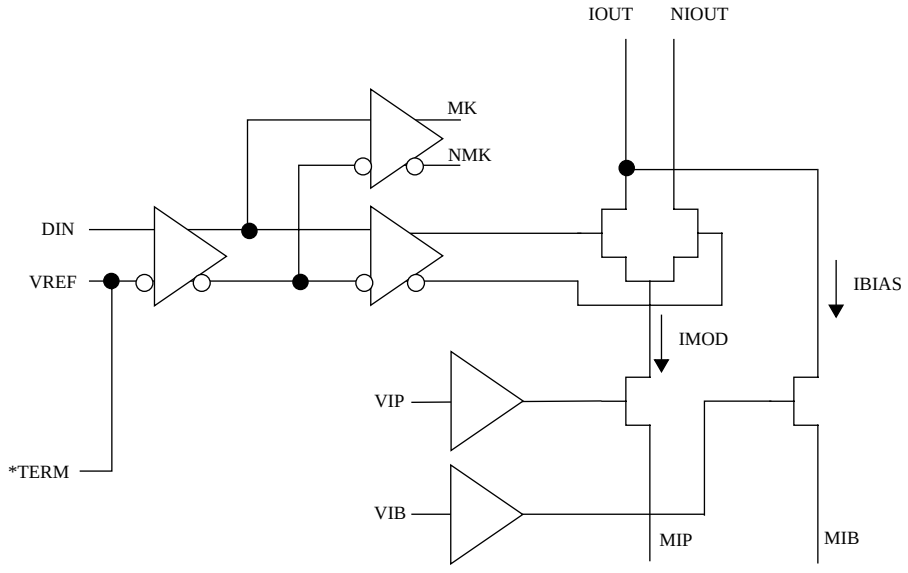
Introduction

The VSC7924 is a single 5V supply, 2.5Gb/s laser diode driver with direct access to the laser modulation and bias FET's. Laser bias and modulation currents are set by external components allowing precision monitoring and setting of the current levels. Data inputs accept ECL levels. Data density outputs are provided to allow the user to adjust the laser bias in high unbalanced data applications.

Applications

- SDH/SONET @ 622Mb/s, 1.244Gb/s, 2.488Gb/s
- Full Speed Fibre Channel (1.062 Gb/s)

VSC7924 Block Diagram



*Terminated to Off-chip Capacitor

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Table 1: Signal Pin Reference

Signal	Type	Level	# Pins	Description
DIN	In	ECL	1	Data Input
MK, NMK	Out	ECL	2	Data Density Differential Outputs
NIOUT	Out		1	Laser Modulation Current Output (Complementary)
IOUT	Out		1	Laser Modulation Current Output (To Laser Cathode))
VSS	Pwr	Pwr	5	Negative Voltage Rail
GND	Pwr	Pwr	8	Positive Voltage Rail
VIP	In	DC	1	Modulation Gate Node
MIP	In	DC	1	Modulation Source Node
VIB	In	DC	1	Bias Gate Node
MIB	In	DC	1	Bias Source Node
VREF	In	DC	1	Data Input Reference
TERM	In	DC	1	Data Input Reference
Total Pins			24	

Table 2: Absolute Maximum Ratings

Symbol	Rating	Limit
V_{SS}	Negative Power Supply Voltage	V_{CC} to -6.0V
T_j	Maximum Junction Temperature	-55°C to + 125°C
T_{stg}	Storage Temperature	-65°C to +150°C

Table 3: ECL Input and Outputs

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IN}	Input Voltage Swing	300		800	mV	Peak to Peak, VREF = -1.3V
V_{OH}	ECL Output High Voltage	-1200		-700	mV	50 Ohms to -2.0 Volts
V_{OL}	ECL Output Low Voltage	-2000		-1600	mV	50 Ohms to -2.0 Volts

Table 4: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
GND	Positive Voltage Rail		0		V	
VSS	Negative Voltage Rail	-5.5	-5.2	-4.9	V	
Tc_l	*Operational Temperature	-40		85**	C	Power dissipation = 1.25W
Tj	Junction Temperature			125	C	

**Lower limit of specification is ambient temperature and upper limit is case temperature.*
***See section "Calculation of the Maximum Case Temperature" for detailed maximum temperature calculations.*

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Table 5: Power Dissipation

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{VSS}	Power Supply Current (VSS)	-	-	220	mA	V_{SS} = -5.5, I_{MOD} = I_{BIAS} = 0 mA
Pd	Total Power Dissipation	-	-	1120	mW	V_{SS} = -5.5, I_{MOD} = I_{BIAS} = 0 mA, Rload = 25 Ohms to GND
Pdmax	Maximum Power Dissipation	-	-	1815	mW	V_{SS} = -5.5, I_{MOD} = 60mA, I_{BIAS} = 50 mA, I_{OUT} = 0 Volts

Table 6: Laser Driver DC Electrical Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{BIAS}	Programmable Laser Bias Current	2		50	mA	-
I_{MOD}	Programmable Modulation Current	2	-	60	mA	
V_{IB}	Laser Bias Control Voltage			V_{SS} + 2.1	V	I_{BIAS} = 50 mA
V_{IP}	Laser Modulation Control Voltage			V_{SS} + 2.1	V	I_{MOD}= 60 mA
V_{OCM}	Output Voltage Compliance	GND -2.2V			V	V_{SS} = -5.2V

Table 7: Laser Driver AC Electrical Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_r t_f	Output Rise and Fall Times			100	ps	25 Ohm load, 20%-80%, 15mA < I_{MOD} < 60 mA, I_{BIAS} = 20 mA

Table 8: Package Thermal Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
θ_{JCC}	Thermal Resistance from Junction to Case		25		°C/W	Ceramic Package
θ_{JCMG}	Thermal Resistance from Junction to Case		32		°C/W	Metal Glass Package

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Calculation of the Maximum Case Temperature

The VSC7924 is designed to operate with a maximum junction temperature of 125°C. The rise from the case to junction is determined by the power dissipation of the device. The power dissipation is determined by the V_{SS} current plus the operating I_{MOD} and I_{BIAS} currents.

The power of the chip is determined by the following formula:

$$P_D = (-V_{SS} * I_{SS}) + ((V_{IOUT} - V_{SS}) * I_{MOD}) + ((V_{IBIAS} - V_{SS}) * I_{BIAS})$$

For example with:

V_{SS} = -5.2V
I_{MOD} = 40mA
I_{BIAS} = 20mA
V_{IBIAS} = -2.0V
V_{IOUT} = -2.0V

$$P_D = (-5.2 * 220mA) + ((5.2 - 2.0) * 40mA) + ((5.2 - 2.0) * 20mA)$$

$$P_D = 1144mW + 128mW + 64mW = 1.336W$$

The thermal rise from junction to case is $\theta_{JC} * P_D$. For the metal glass package, θ_{JC} = 32 °C/W. Thus the thermal rise is:

32°C/W * 1.336W = 42.7°C

The maximum case temperature is:

125°C – 42.7°C = 82.3°C

The absolute maximum power dissipation of the device is at:

V_{SS} = -5.5V
I_{MOD} = 60mA
I_{BIAS} = 50mA
V_{IBIAS} = 0V
V_{IOUT} = 0V

$$P_D = (5.5 * 220mA) + (5.5 * 60mA) + (5.5mA * 50mA) \quad P_D = 1.815W$$

This will net a maximum junction to case thermal rise of: 1.815W * 32°C/W = 58°C

This situation will allow maximum case temperature of: 125°C – 58°C = 67°C

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Input Termination Schemes

Figure 1: Input Structure

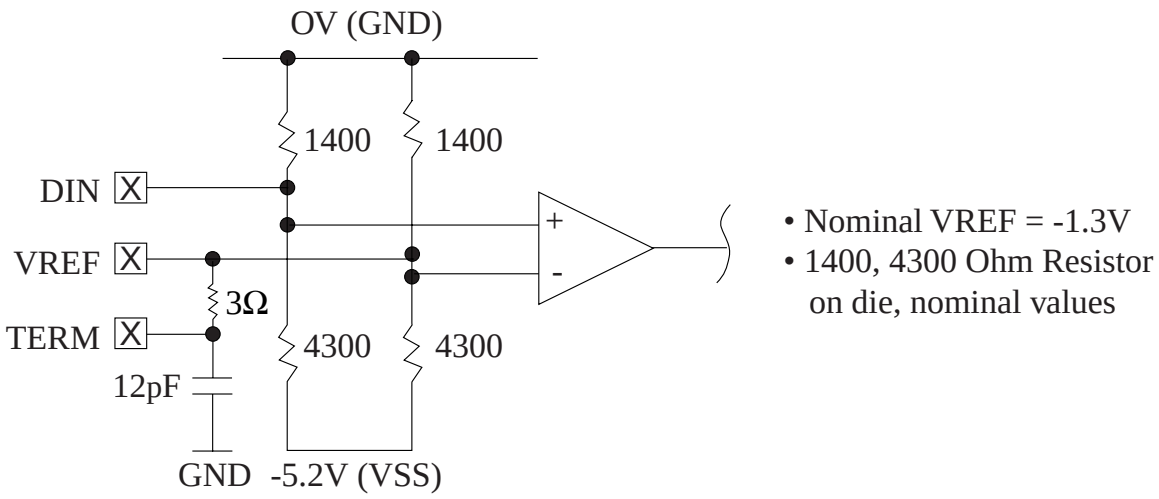

Figure 2: Single Ended AC Coupled

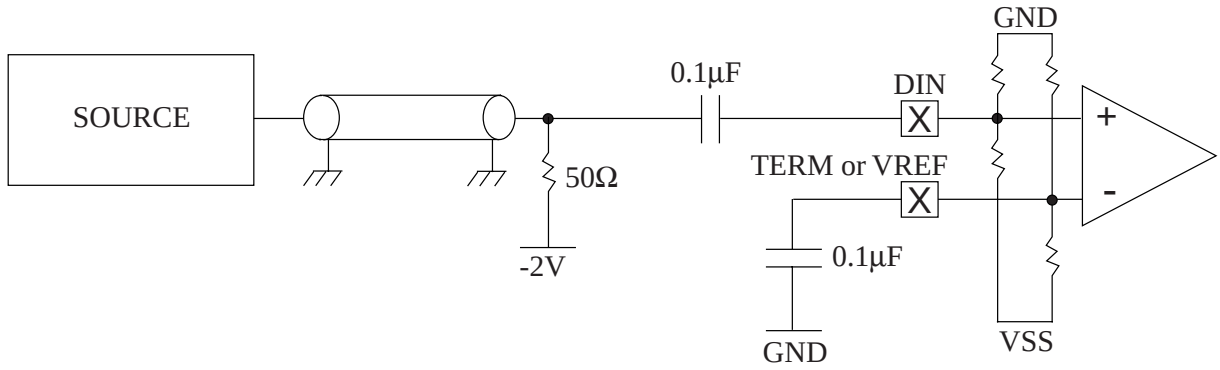

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Figure 3: Single Ended AC Coupled with Offset Adjust

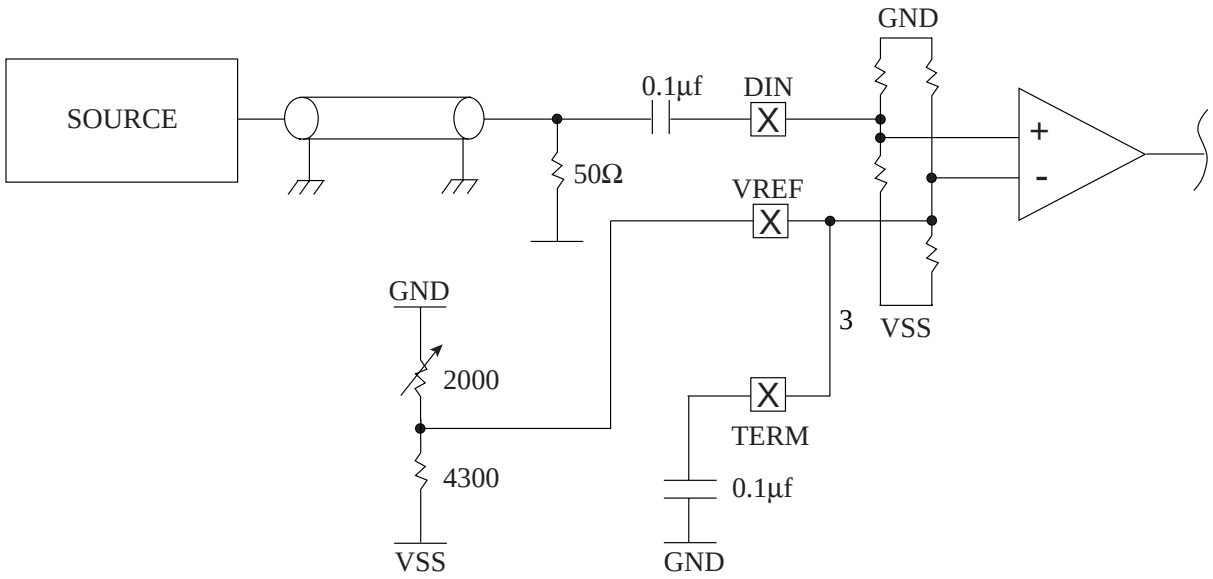
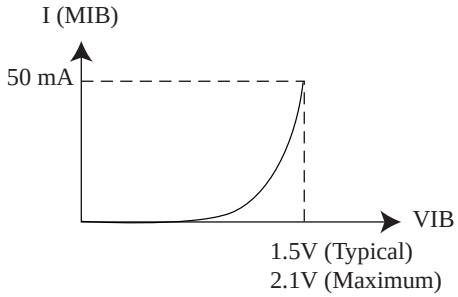
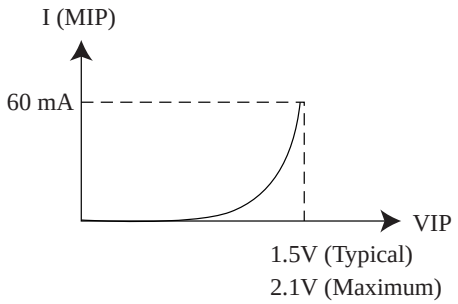


Figure 4: Control Signals VIP and VIB



Typical Bias Current v.s. Bias Voltage



Typical Modulation Current v.s. Modulation Voltage

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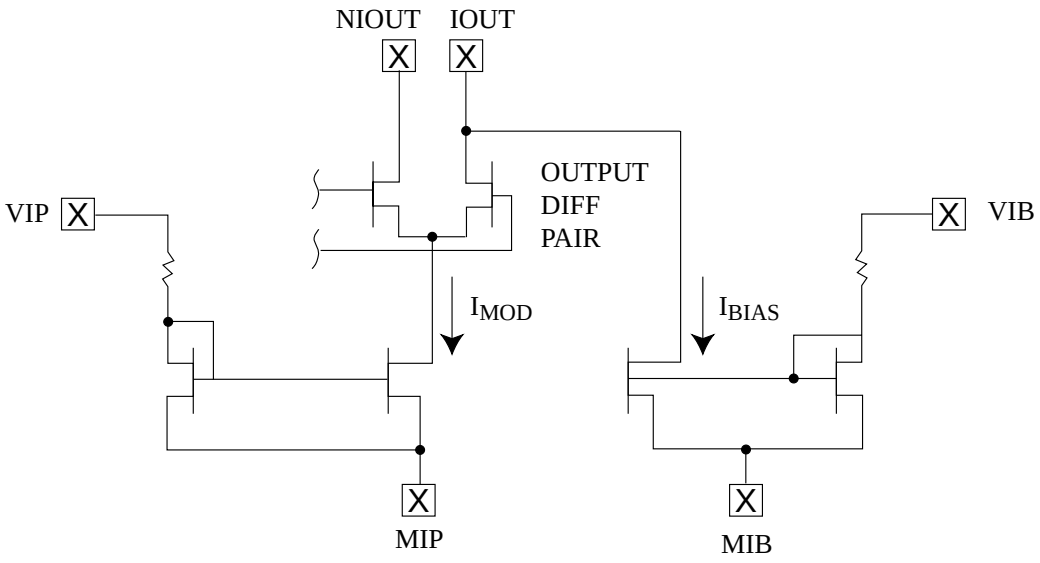
Figure 5: Simplified Output Structure



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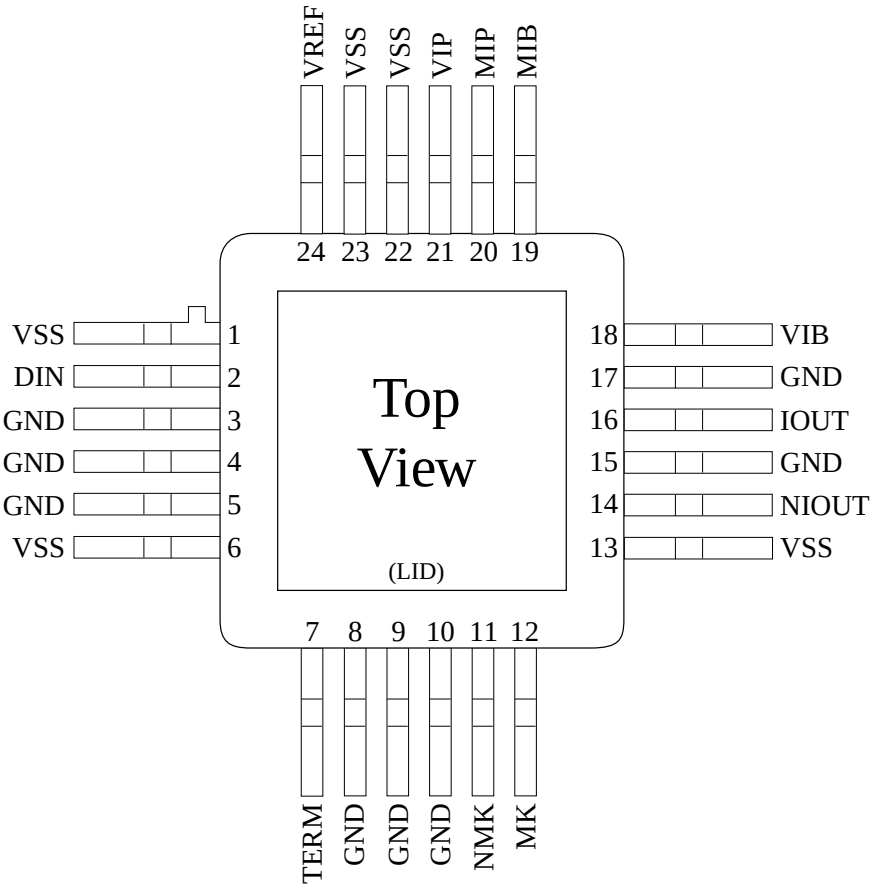
Pin Diagram for 24 Pin Metal-Glass Package



Note: ***Package bottom plate is connected to GND within the package. Package lid is electrically unconnected.***

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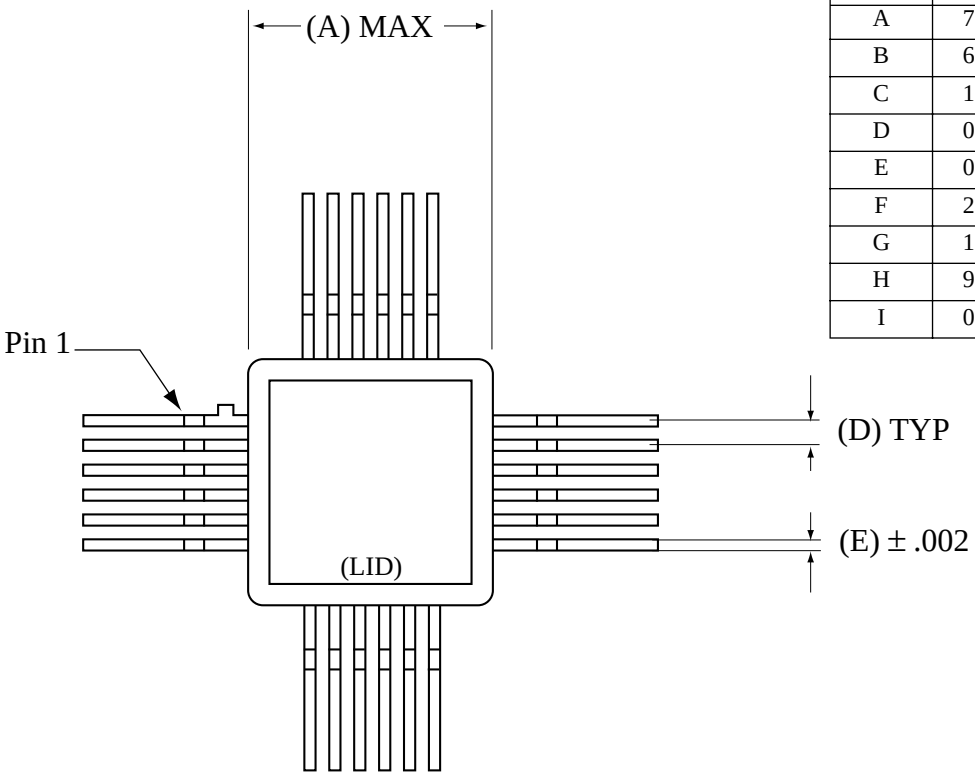
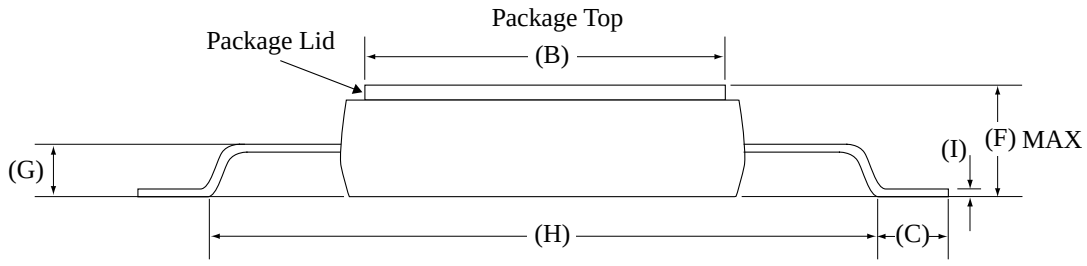
Package Information - 24 Pin Metal-Glass Package (Formed Leads)

Top View



Key	*mm*	*In*
A	7.11	0.280
B	6.10	0.240
C	1.02	0.040
D	0.76	0.030
E	0.30	0.012
F	2.08	0.082
G	1.02	0.040
H	9.52	0.375
I	0.13	0.005

Side View



NOTES: Drawing not to scale.
Package #: 101-291-8 Issue #:1
Lid #: 101-292-3 Issue #:1

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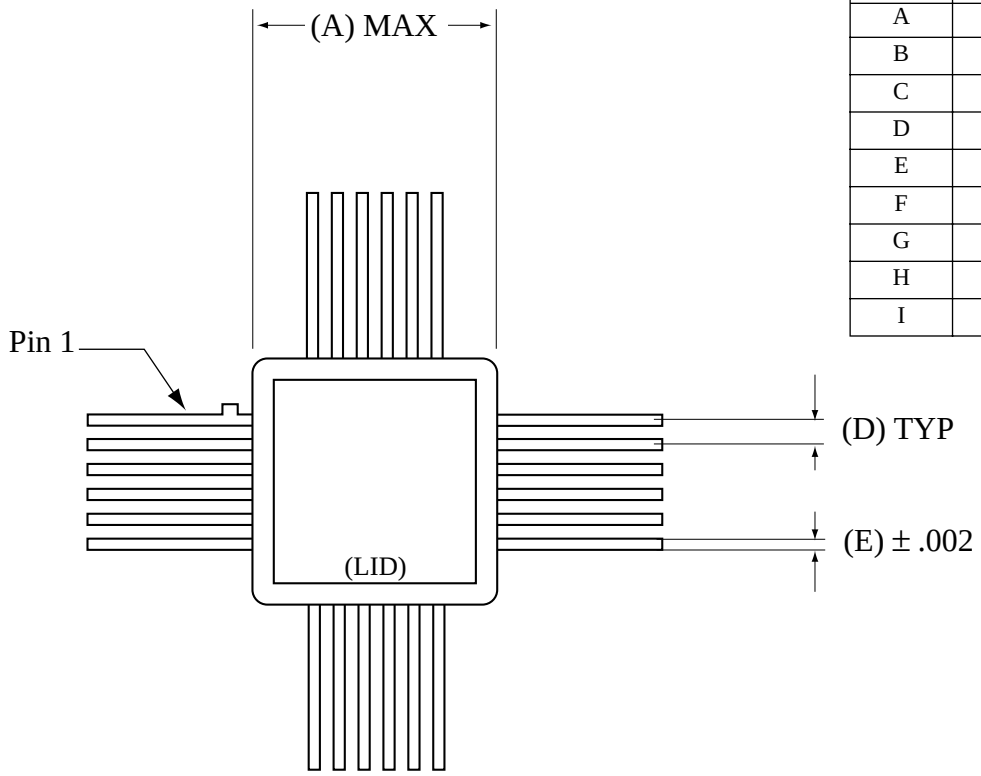
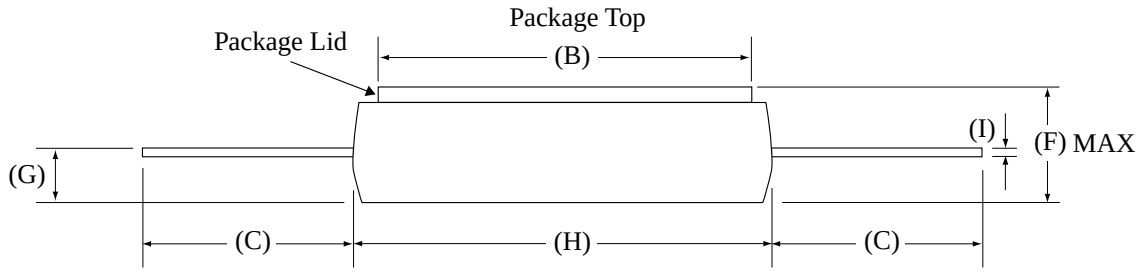
Package Information - 24 Pin Metal-Glass Package (Straight Leads)

Top View



Key	mm	In
A	7.11	0.280
B	6.10	0.240
C	5.21	0.205
D	0.76	0.030
E	0.30	0.012
F	2.08	0.082
G	1.02	0.040
H	7.11	0.280
I	0.13	0.005

Side View



NOTES: Drawing not to scale.
Package #: 101-000-0 Issue #:1

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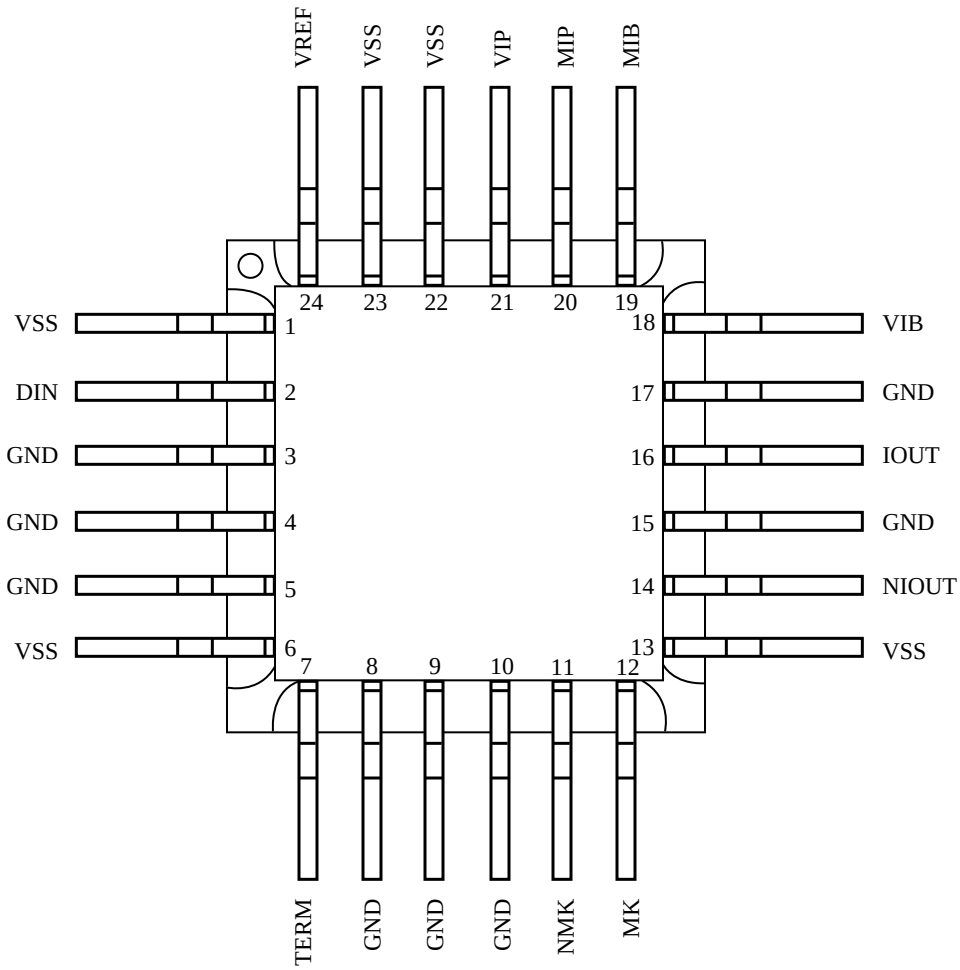
Pin Diagram for 24 Pin Ceramic Package



Note: ***Package bottom plate is connected to GND within the package. Package lid is electrically unconnected.***

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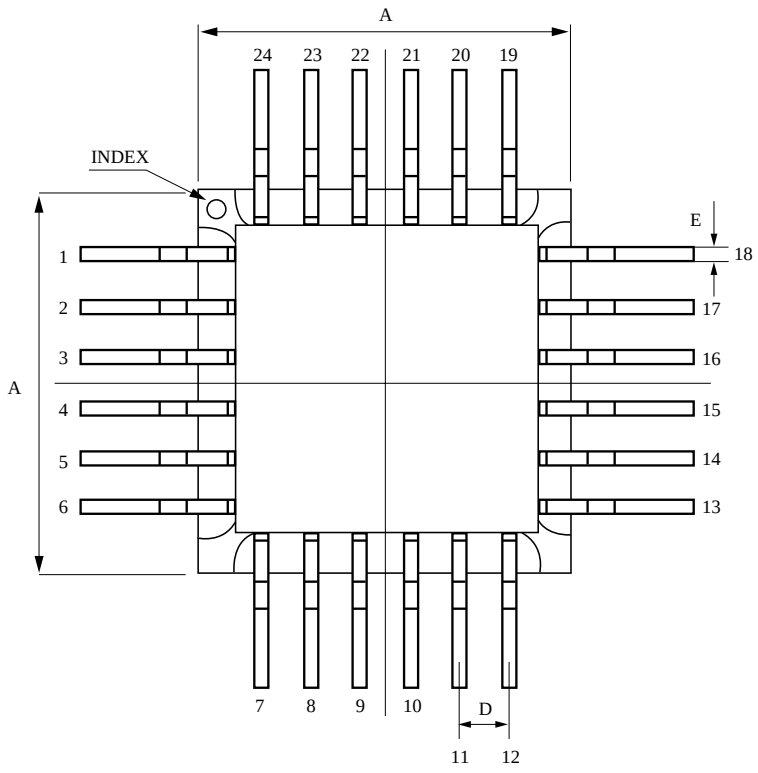
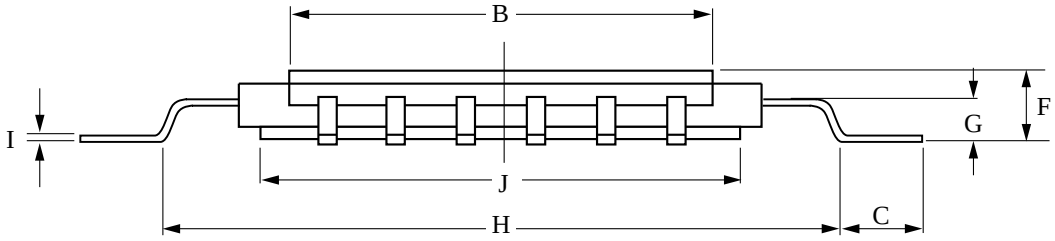
Package Information - 24 Pin Ceramic Package (Formed Leads)

Top View



Key	mm	In
A	9.5	0.374
B	7.7	0.303
C	2.0	0.079
D	1.27	0.050
E	0.30	0.012
F	1.7	0.067
G	0.6	0.024
H	11.5	0.453
I	0.125	0.005
J	8.51	0.335

Side View



NOTES: Drawing not to scale.
Package #: 101-312-0 Issue #:1
L id #: 101-303-1 Issue #:1

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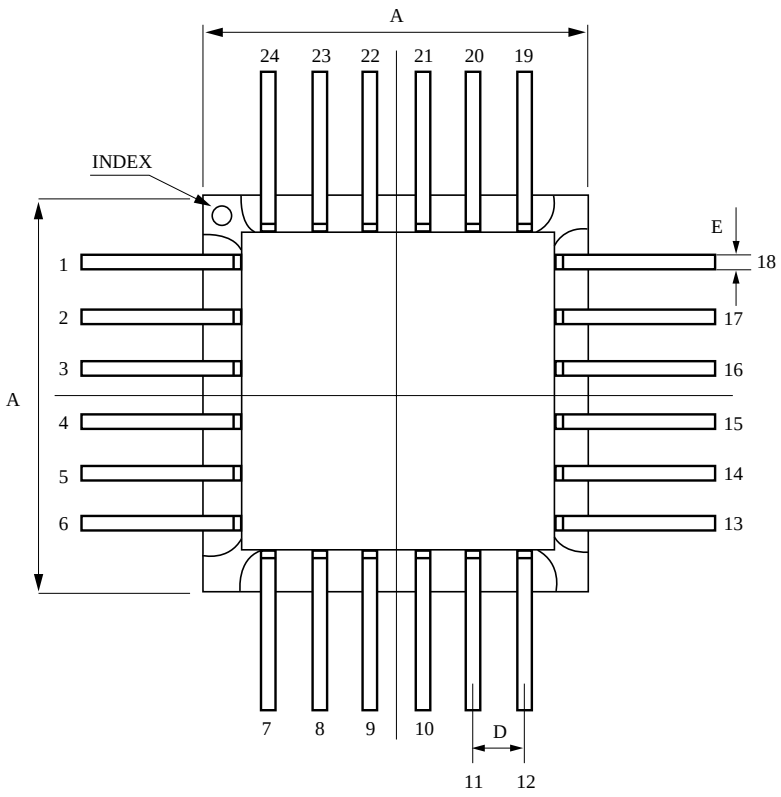
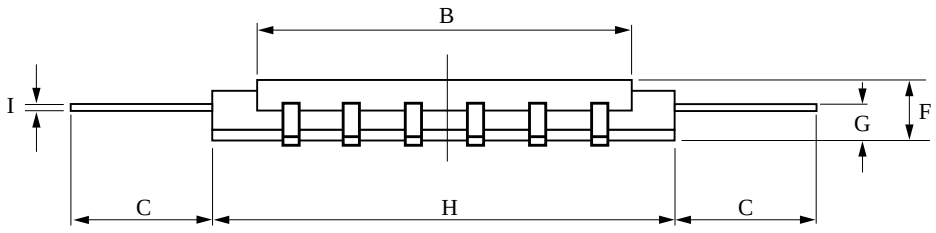
Package Information - 24 Pin Ceramic Package (Straight Leads)

Top View



Key	mm	In
A	9.5	0.374
B	7.7	0.303
C	5.8	.230
D	1.27	0.050
E	0.30	0.012
F	1.7	0.067
G	0.6	0.024
H	9.53	0.375
I	0.125	0.005
J	8.51	0.335

Side View



NOTES: Drawing not to scale.
Package #: 101-000-0 Issue #:1

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Ordering Information

The order number for this product is formed by a combination of the device number, and package style.

VSC7924 **XXX-T** Tape and Reel Devices

Device Type
VSC7924: 2.5Gb/s Laser Diode Driver

Package Style
CA: (Metal Glass - Straight Leads)
KF: (Ceramic - Straight Leads)
CAL: (Metal Glass - Formed Leads)
KFL: (Ceramic- Formed Leads)

Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

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