Advance Product Information

VSC7127/VSC7129

Family of Repeater/Retimer and Port Bypass Circuits for Fibre Channel

Features

- ANSI X3T11 Fibre Channel Compliant
- 1.0625 Gb/s Operation
- Features the FibreTimer™ Configurable Clock Recovery Unit (CRU): Repeater, Retimer or Bypassed
- Six Port Bypass Circuits (PBC)
- Analog/Digital Signal Detect (SDU)
- On-chip transmit termination
- 3.3V, 700mW Power Dissipation
- 44-Pin, 10mm PQFP
- Compatible with HDMP-0451 (VSC7127) or HDMP-0452 (VSC7129)

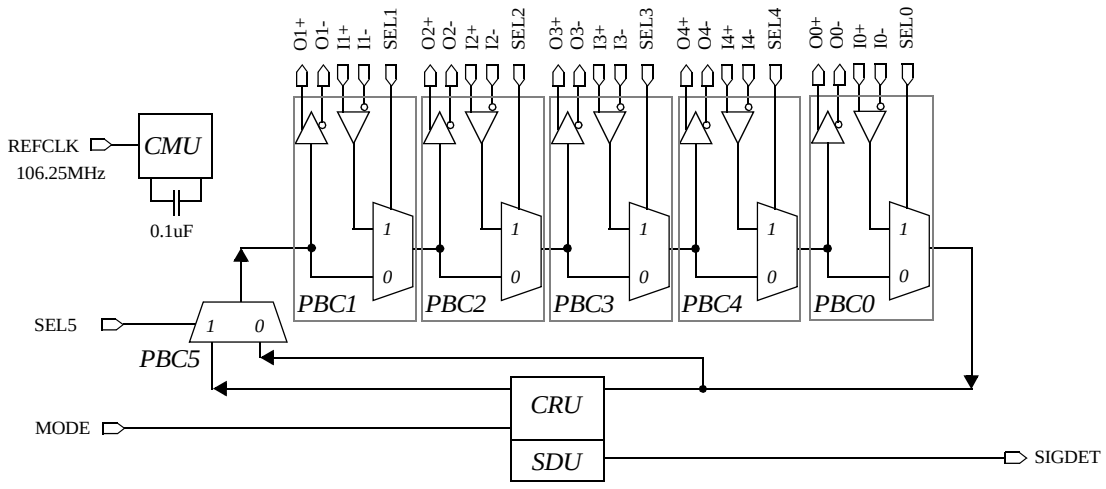
General Description

The VSC7127 and VSC7129 contain six cascaded Port Bypass Circuits (PBCs), the FibreTimer™ configurable Repeater/Retimer (CRU) and a Signal Detect Unit (SDU). These parts are typically used in distributing Fibre Channel signals to an array of disk drives in an FC-AL loop as illustrated in Figure 1: "12-Drive FC-AL JBOD Application". The first VSC7127's CRU is configured as a Repeater to attenuate jitter. The second VSC7127's CRU is bypassed to reduce power. The third VSC7127's CRU is configured as a retimer so that the output of the device is a jitter compliance point.

Each PBC is a multiplexer that is controlled by the corresponding SELx line which, if HIGH, selects the external input or, if LOW, selects the output of the previous PBC. For the VSC712xR, When MODE is LOW and SEL5 is HIGH, the CRU is a sophisticated repeater which has low latency, no peaking and attenuates jitter even at low frequencies. When MODE is HIGH and SEL5 is HIGH, the CRU is a retimer which eliminates jitter transfer but has increased latency due to an elasticity buffer which adds/drops Fibre Channel fill words in order to accomodate the difference between the baud rate of the incoming data and the local REFCLK. When SEL5 is LOW, the CRU is bypassed and powered down. The SDU monitors the analog levels of the I0+/- input and monitors the output of the CRU digitally to indicate whether valid data is present.

The VSC7127/VSC7129 are similar to the VSC7124 which does not contain the FibreTimer™ cell or CMU.

VSC7127/VSC7129 Block Diagram



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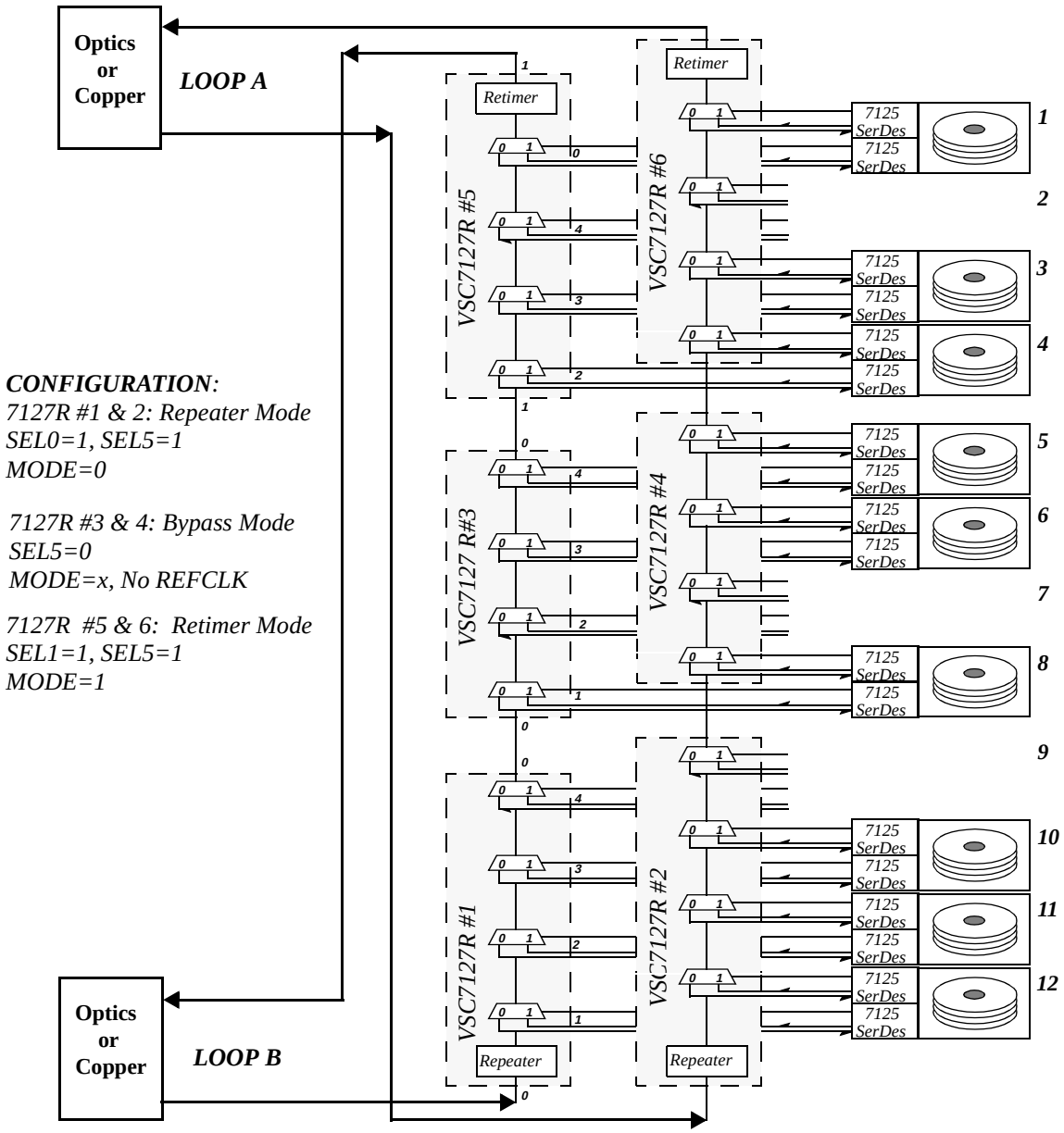
Application: Fibre Channel Disk Arrays

A 12-port JBOD is shown in Figure 1. This dual loop application uses 3 VSC7127Rs on each loop in order to configure the FC-AL disk array. Functional drives are included in the FC-AL loop while non-functional or missing drives (numbers 2,7,9) are excluded.

Figure 1: 12-Drive FC-AL JBOD Application



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Functionality

Device Configurations:

Four devices are specified in this datasheet: VSC7127R, VSC7127T, VSC7129R and VSC7129T. The VSC7127 is pin-compatible to the HDMP-0451. The VSC7129 is pin compatible with the HDMP-0452. The VSC712xR is configured as a Repeater when pin 12, MODE, is LOW, or a Retimer when HIGH. The VSC712xT is configured as a Retimer when pin 12, MODE, is LOW, or a Repeater when HIGH.

Port Bypass Circuits

The VSC712x contains six Port Bypass Circuits (PBCs) which are 2-to-1 multiplexers used to steer serial signals. Each PBC, PBCx, has a single select line, SELx, which when HIGH, selects the external input, Ix, to PBCx and when LOW, selects the output of the previous PBC. PCB5 does not have an external input but selects between the output of the CRU (when SEL5 is HIGH) and the output of PBC0 (when SEL5 is LOW). These controls allow FC-AL loops to include a functional device on the loop or exclude a non-functional device from the loop.

FibreTimer™ Clock Recovery Unit - Repeater Mode

The Clock Recovery Unit (CRU) is a digital PLL which extracts the clock from the incoming data and samples the data with the extracted clock. In repeater mode, the output of the CRU is synchronized to the recovered clock and has improved signal quality due to amplification of the signal and attenuation of jitter. Latency through the device is quite low, just a few bit times. Multiple repeaters can be cascaded without accumulation of jitter. MODE determines whether the CRU is a Repeater or a Retimer.

FibreTimer™ Clock Recovery Unit - Retimer Mode

MODE may configure the CRU as a retimer where the recovered data is placed into an elasticity buffer. Data is taken out of the elasticity buffer and retransmitted synchronously to the local REFCLK. For Fibre Channel data, Fill words will be added and dropped in the elasticity buffer in order to accomodate the differences in speed between the incoming data and the REFCLK. The retimer does not transfer jitter from the input to the output but has longer latency, up to 4 word times, through the device.

FibreTimer™ Clock Recovery Unit - Bypass Mode

When SEL5 is LOW, PBC5 selects the output of PBC0 and the CRU is unused. In this mode, the CRU is powered down to reduce power dissipation. If the part will be used only in this mode, REFCLK and MODE are ignored and can be left open. If the CRU is bypassed, the Signal Detect Unit is disabled and the output is LOW.

Signal Detection

A signal detect unit (SDU) monitors I0+/- and the output of the CRU to determine if there is a valid Fibre Channel signal present. The SIGDET is updated every 160 bits (an “interval”) with the previous interval’s status of three different Signal Detect Units: analog signal amplitude (ASDU), run length check (RLLSDU), Ordered Set density (OSSDU). If the input amplitude is less than 200mV (differential) then ASDU will be set LOW. If the input amplitude is greater than 400mV then ASDU will be asserted HIGH. If a run length viola-

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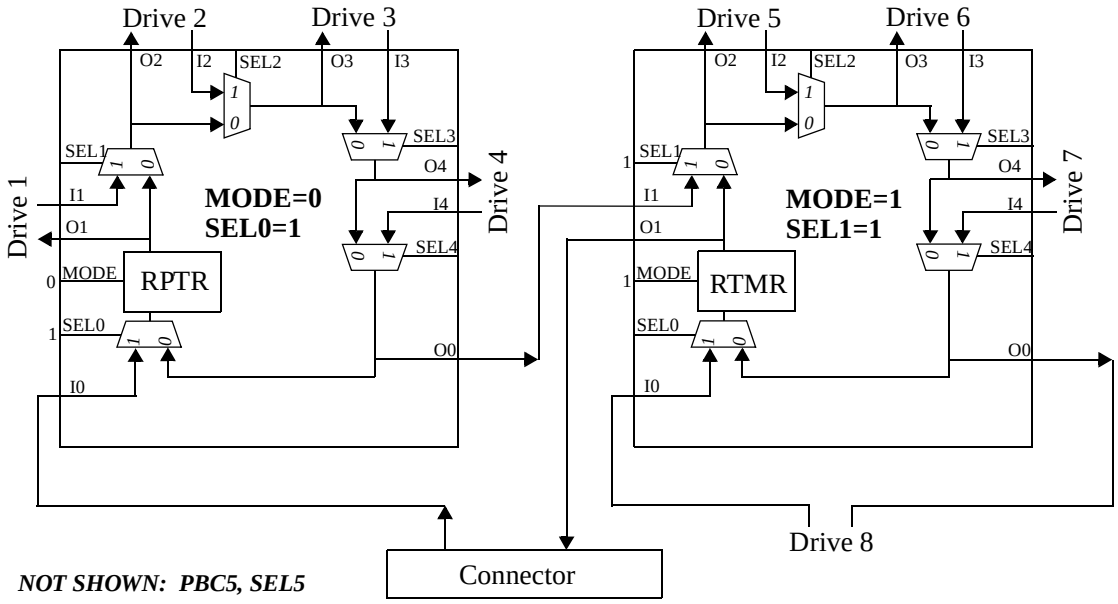
tion occurs (more than 5 consecutive ones or zeros) then the RLLSDU will be set LOW and stay LOW until the occurrence of a valid Fill Word or Primitive Sequence. Any Fill Word or Primitive Sequence will reset the OSSDU counter which will increment on any 40 bit sequence which is not a Fill Word or Primitive Sequence. If the counter reaches 256, a Fill Word or Primitive Sequence has not occured often enough so OSSDU is asserted until reset again. SIGDET is just an or'ing of these three state machines resynchronized to the 160 bit interval clock.

If SEL5 is LOW or REFCLK is absent, the signal detect unit is disabled and SIGDET is LOW.

Application Example

Figure 2 shows one loop of an 8 drive JBOD implemented with two VSC712xs per loop. The input from the connector goes through a repeater in order to clean up the signal prior to the array of disk drives. After all eight PBCs, the output the to connector is retimed to ensure jitter compliance at the connector.

Figure 2: 8-Drive JBOD



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AC Characteristics *(Over Recommended Operating Conditions)*

Figure 3: Timing Waveforms

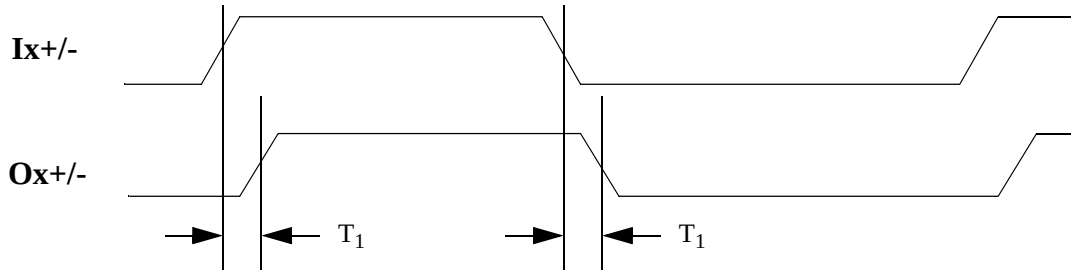

Table 1: AC Characteristics *(Over recommended operating conditions)*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	Propagation Delay (Repeater Mode)	—	7.0	ns	Delay with all circuits bypassed.
T_1	Propagation Delay (Retimer Mode)	—	180	ns	Delay with all circuits bypassed. Typical delay is 100 bit times.
T_R, T_F	Serial data rise and fall time	—	300	ps.	At ΔV_{IN} minimum levels
$T_{j(PBC)}$	Data Jitter Accummulation [PBC Only]	—	TBD	ps	Peak-to-Peak on Ox+/- in Port Bypass Circuit Mode.
$T_{J(RPTR)}$	Total data output jitter [Repeater Mode]	—	192	ps	Jitter Generation at Ox+/- when driven by the CRU in Repeater Mode. IEEE 802.3z Clause 38.68
$T_{DJ(RPTR)}$	Serial data output deterministic jitter (p-p) [Repeater Mode]	—	80	ps	Jitter Generation at Ox+/- when driven by the CRU in Repeater Mode. IEEE 802.3z Clause 38.68
$T_{J(RTMR)}$	Total data output jitter [Retimer Mode*]	—	192	ps	Jitter Generation at Ox+/- when driven by the CRU in Retimer Mode.
$T_{DJ(RTMR)}$	Serial data output deterministic jitter (p-p) [Retimer Mode*]	—	80	ps	Jitter Generation at Ox+/- when driven by the CRU in Retimer Mode.
T_{JTOL}	Jitter Tolerance	0.24	—	UI	Minimum Eye Opening for proper operation as defined in MJS 8.0.
* NOTE: Retimer Mode is available only for Fibre Channel applications.					

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Figure 4: REFCLK Timing Waveforms

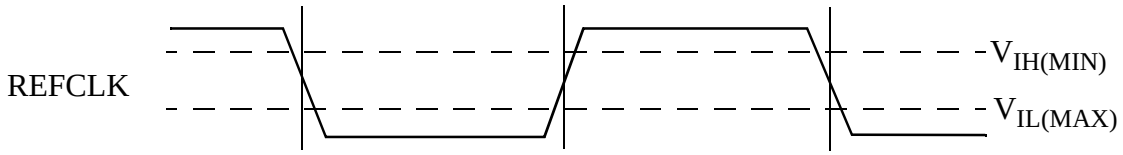

Table 2: Reference Clock Requirements

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	105	107	MHz	
FO	Frequency Offset	-200	200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link
DC	Duty Cycle	35	65	%	Measured at 1.5V
T_R,T_F	Rise and Fall Time	—	2.0	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$

DC Characteristics *(Over recommended operating conditions)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} =0.5V
ΔV_{OUT75}*	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}*	TX Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
ΔV_{IN}*	Receiver differential peak-to-peak Input Sensitivity RX	300	—	2600	mVp-p	Internally biased to Vdd/2
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	700	900	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Current (All Supplies)	—	215	260	mA	Outputs open, V_{DD} = V_{DD} max
I_{DDA}	Current (VDDA)	—	50	70	mA	V_{DDA} = V_{DD} max

** Refer to Application Note AN-37 for details regarding differential voltage measurements.*

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Absolute Maximum Ratings (1)

TTL Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\ TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 2000 V

Recommended Operating Conditions(2)

Power Supply Voltage, (V_{DD}) ..... +3.14V to 3.47V
Ambient Operating Temperature Range, (T) ..... 0°C Ambient to +95°C Case

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions: except where specifically noted in the AC and DC Parametric Tables*

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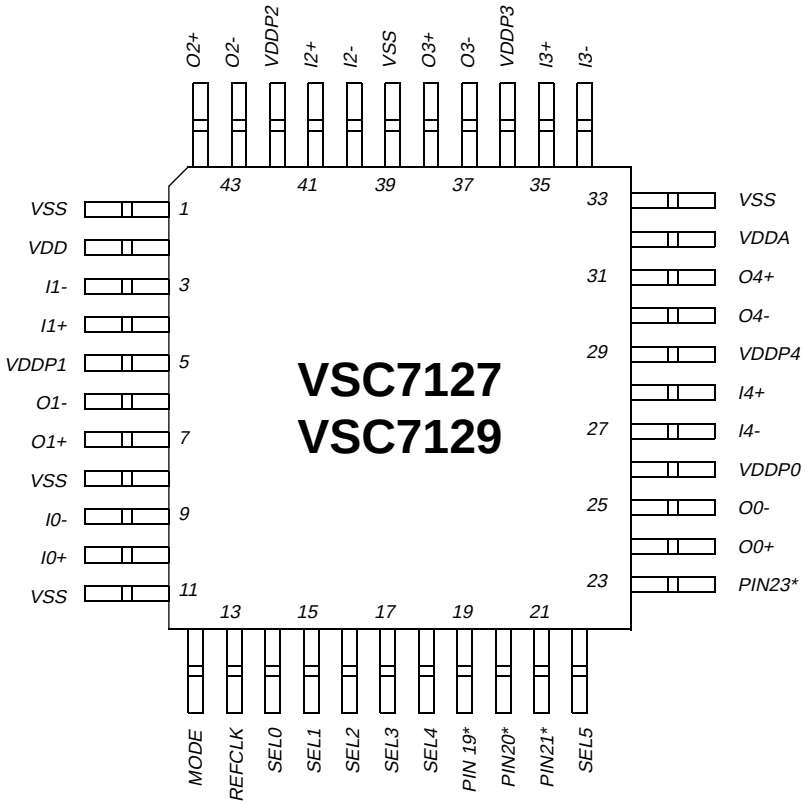
Package Pin Descriptions

Figure 5: Pin Diagram



* See Table 4 for Pin Assignments

Table 3: VSC7127/VSC7129 Pin Assignment Differences

	PIN 19	***PIN 20***	***PIN 21***	***PIN 23***	
VSC7127	VSS	SIGDET	VDD	TRST	Compatible with HDMP-0451
VSC7129	SIGDET	VDD	TRST	VSS	Compatible with HDMP-0452

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Table 4: Pin Identification

Pin #	*Name*	*Description*
4, 3 41, 40 35, 34 28, 27 10, 9	I1+, I1- I2+, I2- I3+, I3- I4+, I4- I0+, I 0-	INPUT - Differential, Internally Biased to VDD/2 I1+/I1- is the serial input to PBC1. I2+/I2- is the serial input to PBC2. I3+/I3- is the serial input to PBC3. I4+/I4- is the serial input to PBC4. I0+/I0- is the serial input to PBC0.
15, 16, 17, 18 14, 22	SEL1, SEL2 SEL3, SEL4 SEL0, SEL5	INPUT - TTL. Port Bypass Mux SELect lines. A HIGH selects Ix. A LOW selects the output of the previous internal device.
7, 6 44, 43 38, 37 31, 30 24, 25	O1+, O1- O2+, O2- O3+, O3- O4+, O4- O0+, O0-	OUTPUT - Differential O1+/O1- is the serial output from Mux1. O2+/O2- is the serial output from PBC port 1. O3+/O3- is the serial output from PBC port 2. O4+/O4- is the serial output from PBC port 3. O0+/O0- is the serial output from PBC port 4.
13	REFCLK	INPUT - TTL 106.25 MHz REFerence CLocK for the internal Clock Multiplier PLL.
12	MODE	INPUT - TTL [NOTE: Different for VSC7127T or VSC7127R] In the VSC7127T, MODE configures the part as a Retimer if LOW or a Repeater if HIGH. In the VSC7127R, MODE configures the parts as a Repeater if LOW or a Retimer if HIGH. If unused, tie HIGH or LOW.
20 (VSC7127) 19 (VSC7129	SIGDET	OUTPUT - TTL: SIGnal DETect output.
23 (VSC7127) 21 (VSC7129)	TRST	INPUT - TTL: (Internal Pull-up Resistor) Test mode input. Pull HIGH or leave open for normal operation.
2 21 (VSC7127) 20 (VSC7129)	VDD	Digital Logic Power Supply..
5 26 29 36 42	VDDP1 VDDP2 VDDP3 VDDP4 VDDP0	Power Supply (3.3V) for O1+/-. If unused, connect to VSS. Power Supply (3.3V) for O2+/-. If unused, connect to VSS. Power Supply (3.3V) for O3+/-. If unused, connect to VSS. Power Supply (3.3V) for O4+/-. If unused, connect to VSS. Power Supply (3.3V) for O0+/-. If unused, connect to VSS
32	VDDA	Analog Power Supply.
1, 8, 11, 33, 39 19 (VSC7127) 23 (VSC7129)	VSS	Ground.

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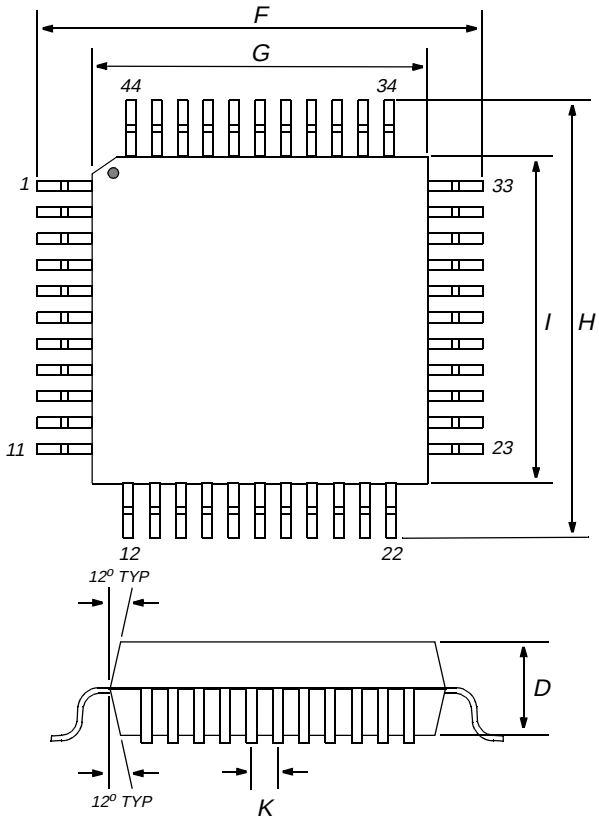
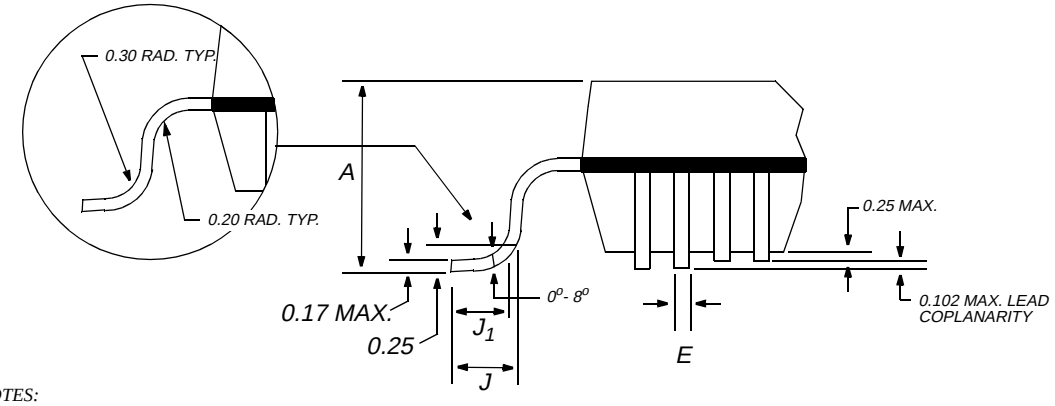
Package Information

44-Pin PQFP 10 x 10 mm



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10
E	0.35	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.80	BASIC



NOTES:
Drawing not to scale.
Cavity up
All units in mm unless otherwise noted.

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Package Thermal Characteristics

The VSC7127/VSC7129 is packaged in a standard plastic quad flatpack, PQFP, with an embedded, but unexposed thermal heatslug. This package adheres to industry standard EIAJ footprints for a 10 mm body, 44 lead PQFP. The package construction is as shown below. The 44 PQFP with embedded slug has the thermal properties shown below.

Figure 6: Package Cross Section - 10 mm package

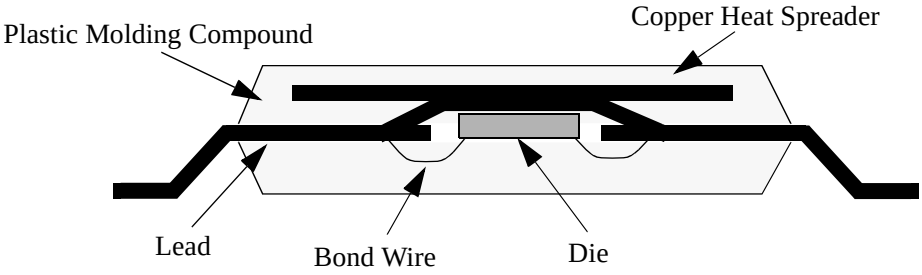

Table 5: 44 PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
$\theta_{ca\text{-}0}$	Thermal resistance from case to ambient, still air	50	^{o}C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient, 100 LFPM air	43	^{o}C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient, 200 LFPM air	39	^{o}C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient, 400 LFPM air	36	^{o}C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient, 600 LFPM air	34	^{o}C/W

The VSC7127/VSC7129 is designed to operate with a case temperature up to 95^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown above, the 10mm PQFP can operate in still air ambient temperatures of 50^{o}C [50^{o}C = 95^{o}C - 0.9W * 50]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Moisture Sensitivity Level

This device is rated at with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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Ordering Information

The order number for this product is formed by a combination of the device number and package type.

VSC712xx QM

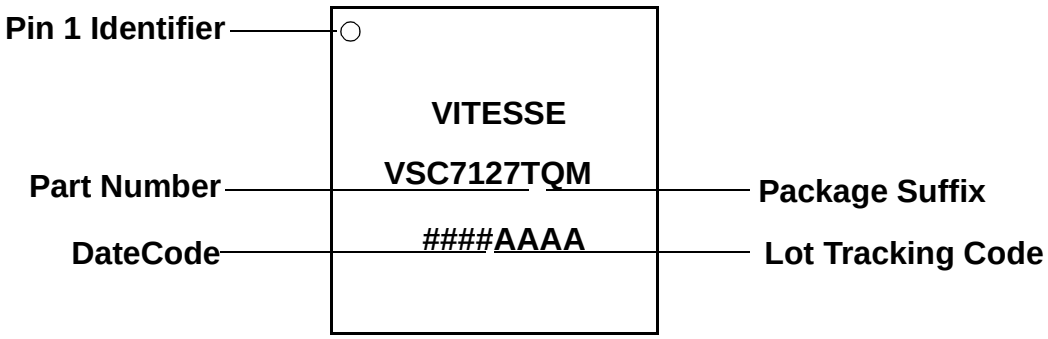
Device Type
VSC7127T - Configured as a Retimer when MODE is LOW. HDMP-0451 Compatible
VSC7127R - Configured as a Repeater when MODE is LOW. HDMP-0451 Compatible
VSC7129T- Configured as a Retimer when MODE is LOW. HDMP-0452 Compatible
VSC7129R- Configured as a Repeater when MODE is LOW. HDMP-0452 Compatible

Package Type
QM: 44 Pin PQFP, 10mm Body

Marking Information

The package is marked with three lines of text as shown below {VSC7127TQM shown)

Figure 7: Package Marking Information



Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in the document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

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