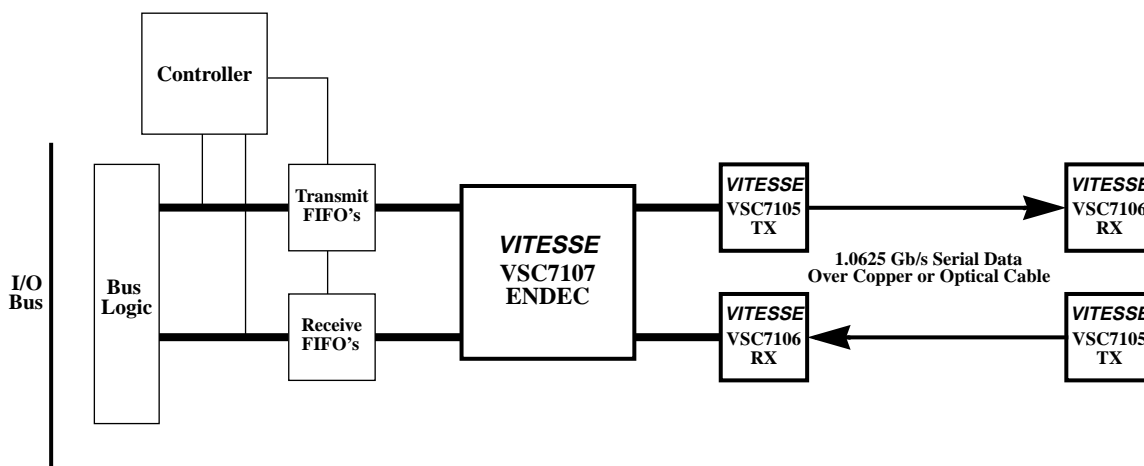


## 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

- ANSI X3T11 Fibre Channel Compatible at 1.0625 Gbit/s
- On-chip Fully Monolithic Clock Recovery and Clock Multiplication Circuits Require No External Components
- On Chip Clock Multiplication Relieves System of High Speed Clock Generation
- Single +3.3V Supply Operation
- Dual Receiver Serial Inputs and Transmitter Outputs for Loopback and Multiple Link Applications
- Selectable 10 or 20 bit TTL Compatible Parallel Interface
- High Sensitivity Differential Receiver Suitable for both Coaxial and Optical Link Applications

The VSC7105/VSC7106 chipset is compatible with the ANSI X3T11 Fibre Channel Standard. Fibre Channel is a high speed communication channel standardized by ANSI for mapping upper layer protocols (ULP) such as SCSI, IP, and HIPPI. Fibre Channel can then provide a channel over which concurrent communication of all ULP's may exist on a single interconnect between workstations, mainframes, and supercomputers, and for connection to mass storage devices and other peripherals. The Fibre Channel physical layer is also ideal for building cost effective, very high speed point-to-point communications links.

### System Block Diagram



**VSC7105 Transmitter Functional Description**

The VSC7105 is an ANSI X3T11 compatible Fibre Channel (FC) transmitter designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7105 performs the serialization of parallel data and simplifies system design by performing clock multiplication from the parallel data clock. The VSC7105 has two modes of operation: 10-bit and 20-bit. The functional block diagrams for the 20-bit and 10-bit modes are shown in Figure 1 and Figure 2 respectively.

The VSC7105 accepts 8B/10B encoded TTL input data as one or two parallel 10 bit characters which are clocked into the device at 1/10 or 1/20 of the baud rate. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification or any other equivalent coding scheme with a transition density of 40% or greater and a maximum run length of 6 consecutive 1's or 0's. The VSC7105 serializes the input data and transmits it at a baud rate of 10 times the frequency of the REFCLK input. The device includes a phase locked loop-based clock multiplier that generates the baud clock. This PLL is fully monolithic, and requires no external components.

The parallel input port timing is derived from the REFCLK input. REFCLK is internally divided by two, and driven off chip as complementary TTL outputs: TCLK and TCLKN. In 20-bit mode, the VSC7105 loads parallel data on the falling edge of TCLK. TCLK thus provides a convenient means to clock the data source. For 10 bit mode, the VSC7105 loads parallel data on the rising edge of REFCLK. The rising edge of REFCLK corresponds to the falling edges of both TCLK and TCLKN. The system designer may either use the rising edge of REFCLK or the falling edges of TCLK and TCLKN to clock the data source. Only data on T10:19 are used in 10-bit mode. The width of the input data bus is controlled by the DWS (Data Width Select) input. A logic LOW on this input places the VSC7105 in 20-bit mode and a logic HIGH places the VSC7105 in 10-bit mode.

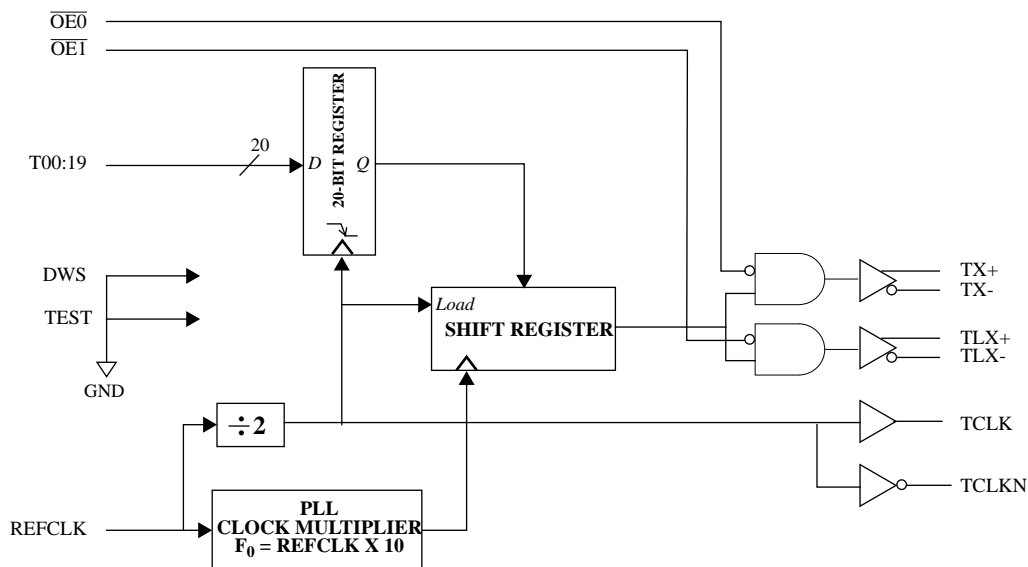
Output Enable controls are provided for each of the serial output ports.  $\overline{OE0}$  controls the primary outputs, TX, while  $\overline{OE1}$  controls the secondary outputs, TLX. When an  $\overline{OE}$  control is brought HIGH, the respective output is forced to a logical HIGH state. For example, a logical HIGH on the TX differential outputs will cause TX- to be LOW and TX+ to be HIGH. The secondary outputs can be used as a local loopback for system testing.

A three-level TEST signal is provided to facilitate functional testing and to select NRZ or NRZI data format. When TEST is left floating, REFCLK replaces the PLL-generated internal clock. For normal operation using the PLL-generated bit clock in Fibre Channel compliant mode which uses NRZ formatting, the TEST pin is tied to GND. For normal operation using NRZI formatting, the TEST pin is tied  $V_{DD}$ .

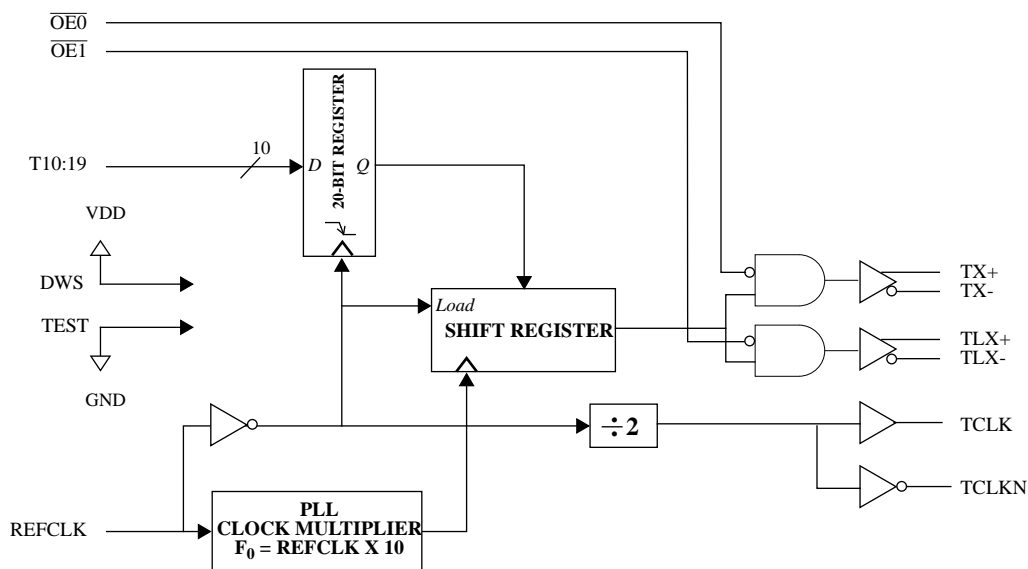
### Data Sheet

1.0625 Gbit/sec Transmitter/Receiver Chipset  
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**Figure 1: VSC7105 Transmitter Functional Block Diagram (20-Bit Mode)**



**Figure 2: VSC7105 Transmitter Functional Block Diagram (10-Bit Mode)**



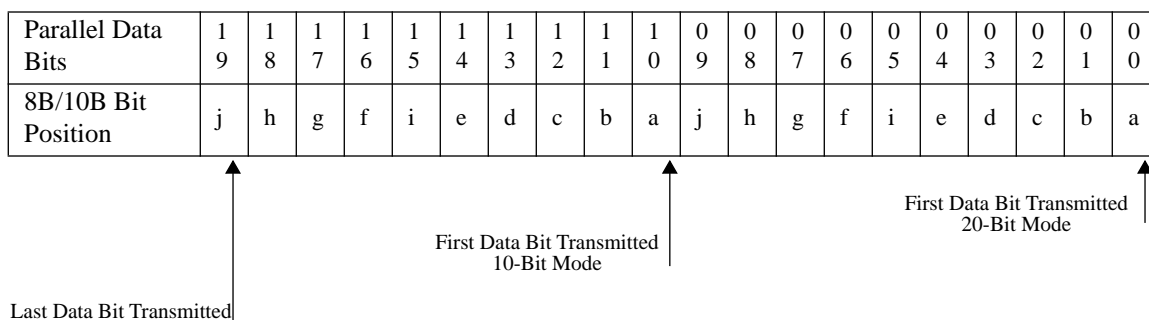
## 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

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### Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. A Fibre Channel word is 32 bits which is encoded into a transmission word of 40 bits. The 20 bit interface on the VSC7105 corresponds to a half transmission word. This document uses character and half-word to refer to transmission character and half transmission word respectively. Hence the VSC7105 has a selectable transmission character or half transmission word Fibre Channel interface. The bit ordering and its relationship to Fibre Channel bit position is shown in Figure 3 for the VSC7105. In 20-bit mode, T00 is transmitted first and in 10-bit mode, T10 is transmitted first.

**Figure 3: Transmission Order and Mapping to Fibre Channel Character**



### VSC7106 Receiver Functional Description

The VSC7106 is an ANSI compatible Fibre Channel (FC) receiver designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7106 accepts differential high speed serial inputs, extracts the clock and retimes the data from the serial bit stream. The serial bit stream should be 8B/10B encoded data produced by a FC compatible transmitter, or any other source with a transition density of 40% or greater and a maximum run length of 6 consecutive 1's or 0's. The retimed serial bit stream is converted into either a 10 or 20-bit parallel output word. The VSC7106 provides Fibre Channel SYNC character recognition and data word alignment. The VSC7106 has internal PLL-based clock recovery circuitry which requires no external components.

Serial data is received on the RX, RLX pins as determined by LPEN. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within 1.0% of the expected data rate. The expected data rate is 10 times the REFCLK frequency. For example if the REFCLK used is 106.25MHz, then the incoming serial baud rate must be 1.0625 Gigabaud  $\pm 1.0\%$ .

The VSC7106 provides complementary TTL recovered clock, RCLK and RCLKN, which is at one twentieth of the serial baud rate. This clock is generated by dividing down the high-speed clock which is phase locked to the serial data. If serial input data is not present, or does not meet the required transition density or baud rate, the RCLK frequency will be within  $\pm 1.5\%$  of half of the REFCLK. The serial data is retimed by the internal high-speed clock, and deserialized. Parallel data is loaded into the output register on the falling edge of RCLK in 20-bit mode or on the falling edges of RCLK and RCLKN in 10 bit mode. The width of the output field can be 10 or 20-bit, under the control of the DWS (Data Width Select) pin. A logic LOW on this input causes the parallel data to be presented 20-bit wide. A logic HIGH causes a single 10-bit character to be presented on

### Data Sheet

### 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

R10:19, R00:09 are held HIGH in this mode. The functional block diagrams for operation in 20-bit or 10-bit modes are shown in Figure 4 and Figure 5 respectively.

Word synchronization is enabled in the VSC7106 by tying the SYNCEN pin to  $V_{DD}$ . When synchronization is enabled, the VSC7106 constantly examines the serial data for the presence of the Fibre Channel “Sync” character. This pattern is “0011111010” and is referred to as a K28.5 character with negative beginning disparity. The K28.5 character is not a normal data character, but a special character defined specifically for synchronization by Fibre Channel. Improper alignment occurs when a K28.5 straddles a 10 bit boundary or when a K28.5 is in the wrong 10-bit position of a half-word. When an improperly aligned sync character is encountered in 20-bit mode, the internal divider which produces RCLK and RCLKN is stalled in such a manner that the sync character is aligned in the R00:09 output field. This results in proper character and half-word alignment. In 10-bit mode, proper alignment is established when the K28.5 does not straddle a 10-bit character boundary, and appears in a character that is clocked out on the falling edge of RCLKN. Half-word synchronization is still relevant in 10-bit mode.

When the parallel data alignment changes in response to a sync pattern, some data which would have been presented on the parallel output port will be lost. The detection of the sync character is pipelined. Depending on the required new output phase, the sync character itself may be destroyed by the synchronization operation. Nonetheless, data following the sync character will be correctly aligned. Thus if downstream logic requires detection of the sync character (for example, to accomplish ordered set alignment) then more than one sync character must be transmitted in order to guarantee that one will be forwarded out of the VSC7106 uncorrupted. Fibre Channel compliant systems requires the receipt of a minimum of three ordered sets for word synchronization. Ordered sets are special Fibre Channel transmission words that have the K28.5 sync character as the first character received. The first of these ordered sets will cause resynchronization in the VSC7106. The subsequent two ordered sets will be correctly aligned when they are received. In systems where synchronization is undesired, tying SYNCEN to GND will disable the sync function, and the data will be unframed.

On encountering a sync pattern, a pulse is generated on the SYNC output to inform the user that realignment of the parallel data field may have occurred. The SYNC pulse is presented one cycle in advance of the actual K28.5 character, and has a duration equal to the data. When operating the VSC7106 in 20-bit mode, the SYNC pulse spans one period of RCLK. In 10-bit mode, the pulse is HIGH for half of an RCLK period. Functional waveforms for synchronization in both modes are given in Figure 6 and Figure 7. Figure 6 shows the case when a sync character is detected and no phase adjustment is necessary. It illustrates the position of the SYNC pulse in relation to the sync character. Figure 7 shows the case where the K28.5 is detected, but out of alignment and a change in RCLK and the output data is required. Note that the VSC7106 always stretches the RCLK so it will never create a clock sliver on resynchronization.

Figure 4: VSC7106 Receiver Functional Block Diagram (20-Bit Mode)

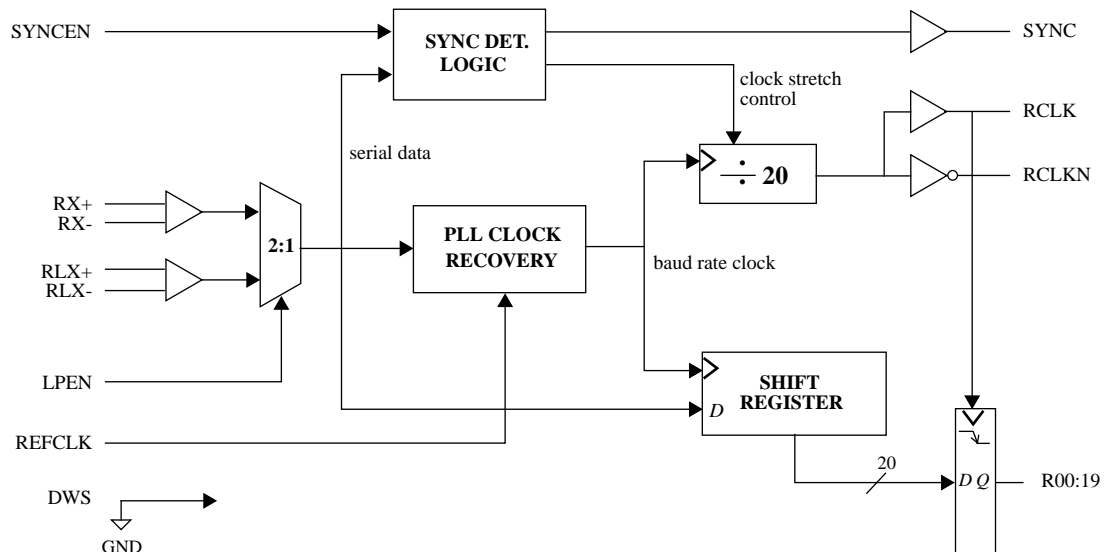
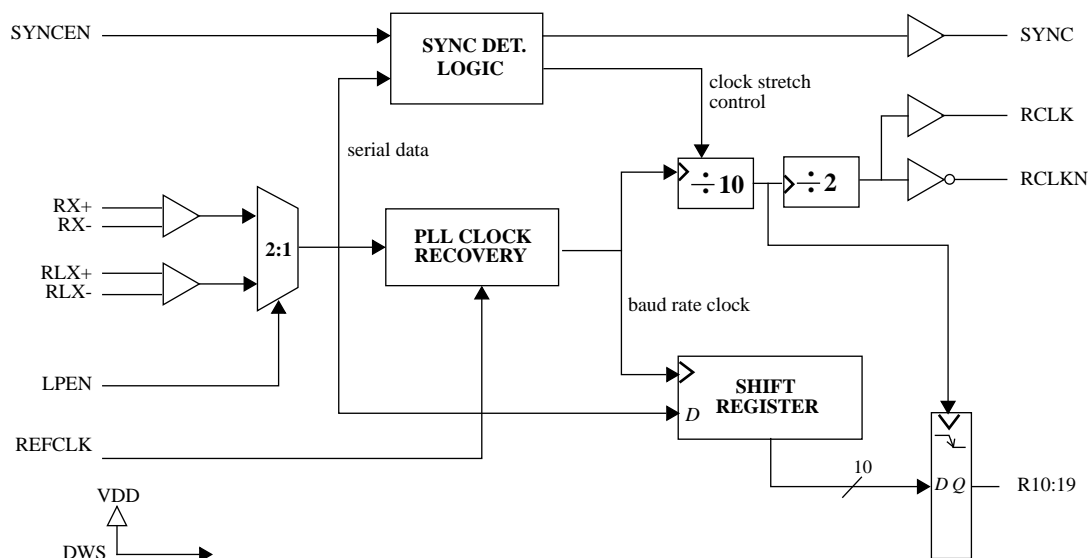


Figure 5: VSC7106 Receiver Functional Block Diagram (10-Bit Mode)

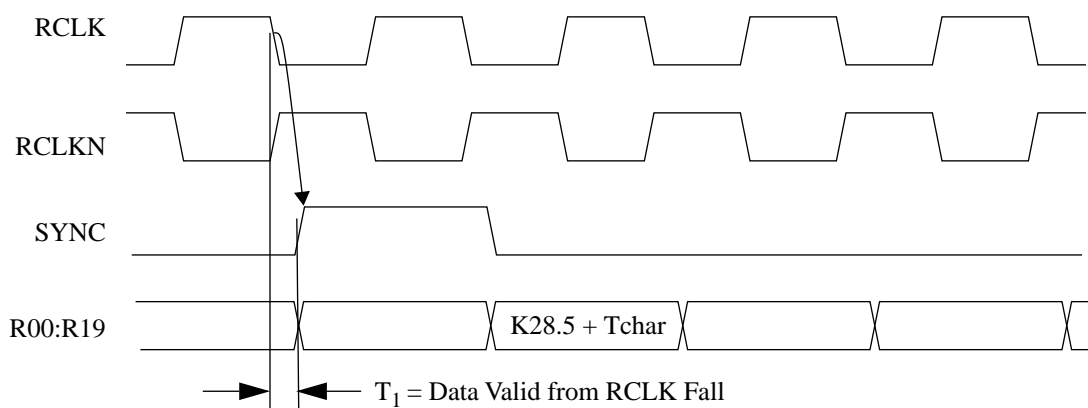


### Data Sheet

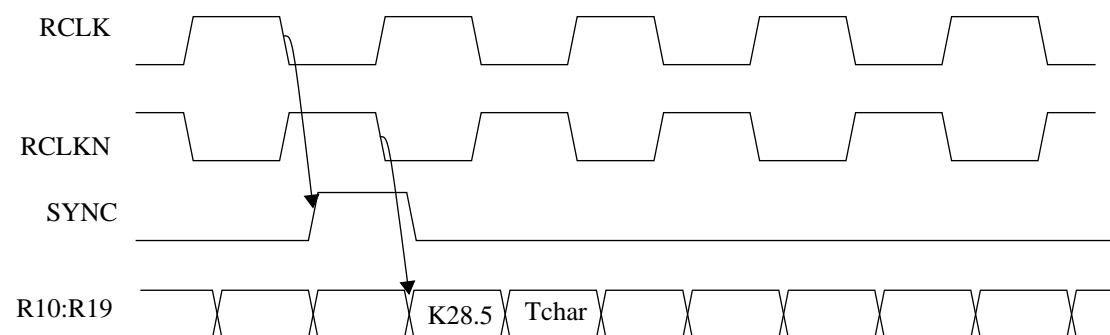
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Figure 6: Sync Timing While In Sync

#### 20 Bit Mode Timing

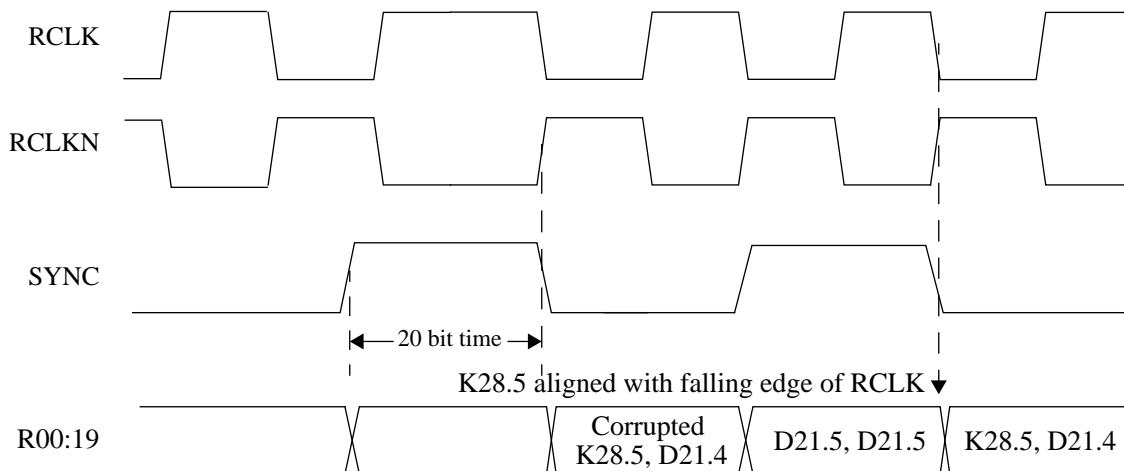
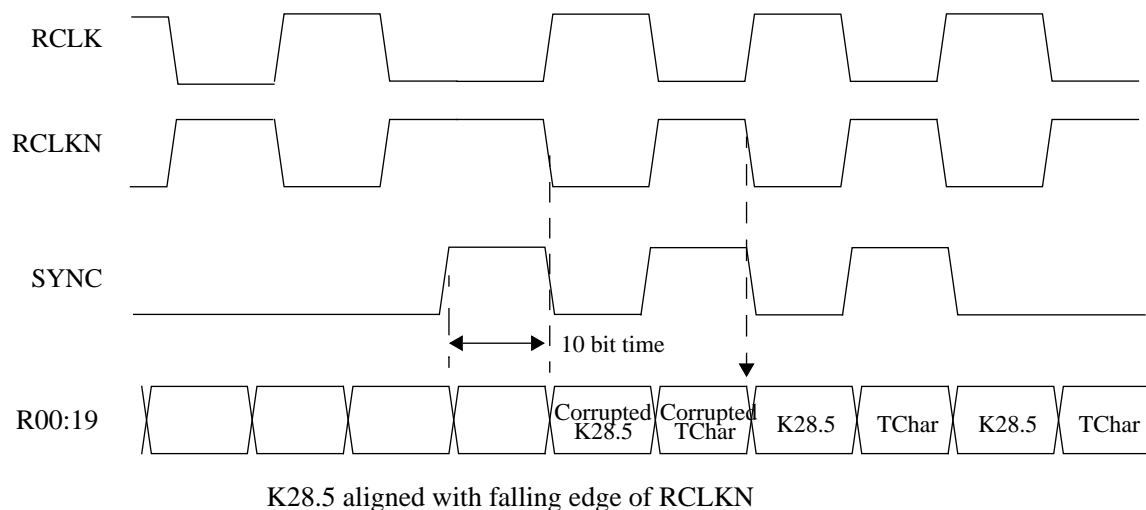


#### 10 Bit Mode Timing



*TChar: 10 bit Transmission Character*

Figure 7: Sync and RCLK Timing When Resynchronizing

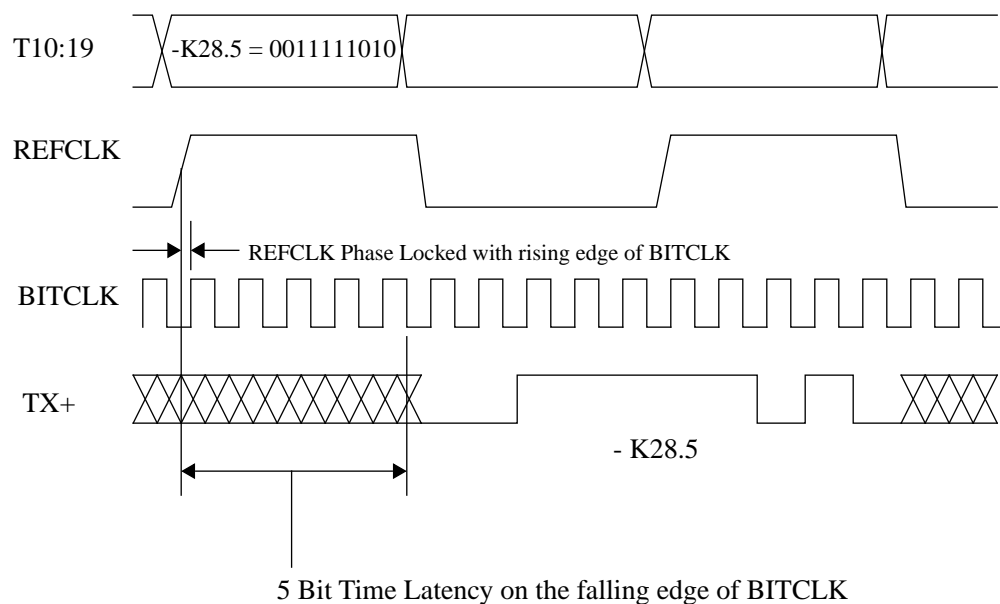
**20 Bit Timing, Receiving Two Consecutive IDLE Words (K28.5, D21.4, D21.5, D21.5)****10 Bit Timing, Receiving Three Consecutive K28.5+TChar Half-Words**



### Data Sheet

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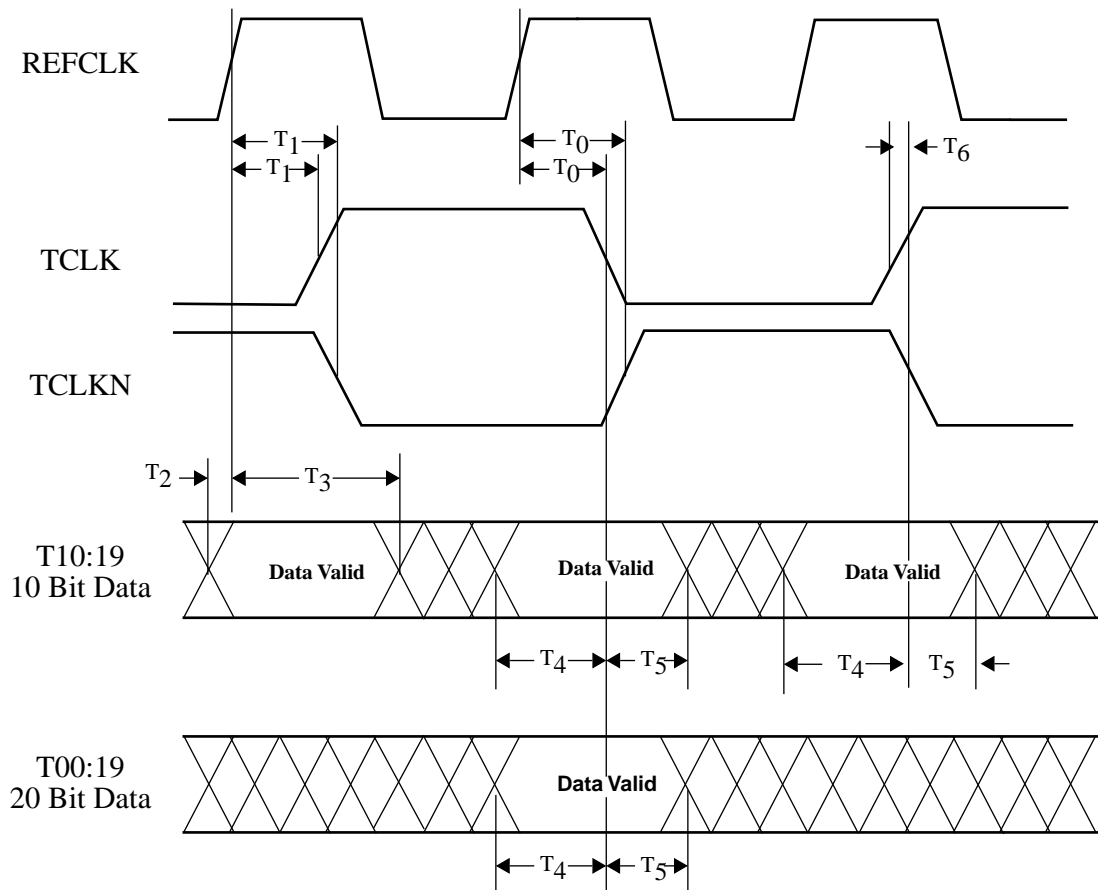
**Figure 8: Transmitter Latency Waveform**



**Table 1: Data Latency**

VSC7105 Parallel to Serial Latency (10-Bit Mode)	5 Bit Times
VSC7105 Parallel to Serial Latency (20-Bit Mode)	5 Bit Times
VSC7106 Serial to Parallel Latency (10-Bit Mode)	26 Bit Times
VSC7106 Serial to Parallel Latency (20-Bit Mode)	46 Bit Times

Figure 9: VSC7105 Timing Waveforms



### Data Sheet

### 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

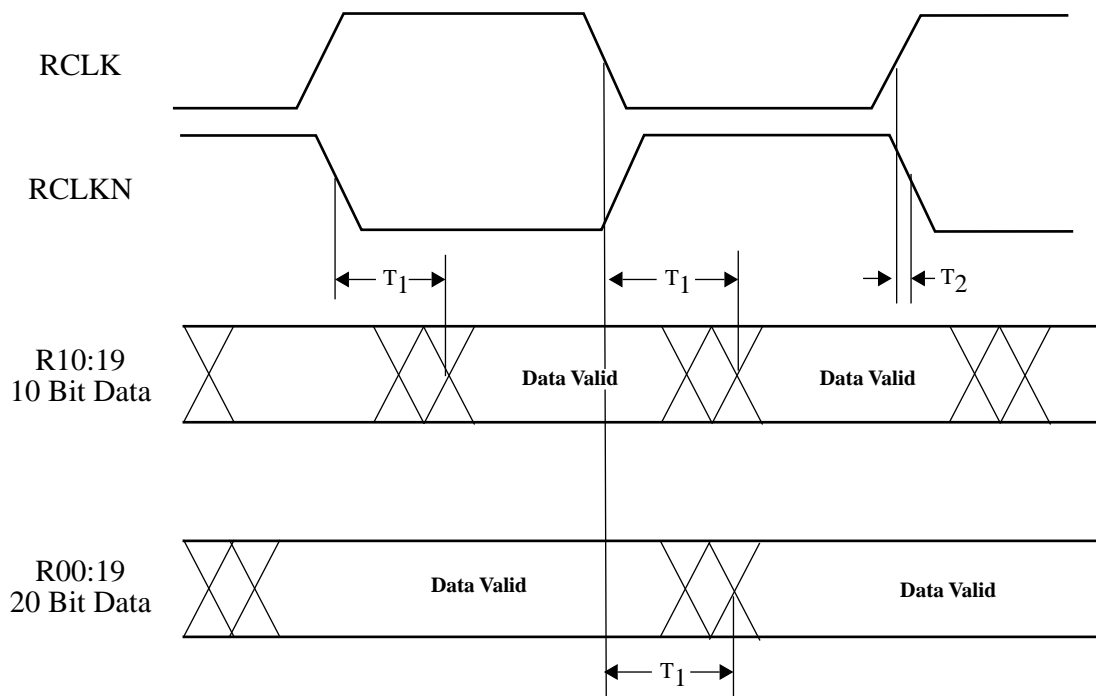
**Table 2: VSC7105 AC Characteristics**

<i>Parameters</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
$T_0$	REFCLK rise to TCLK fall and TCLKN rise	1.0	4.0	ns	—
$T_1$	REFCLK rise to TCLK rise and TCLKN fall	1.0	4.0	ns	—
$T_2$	Data setup w.r.t. REFCLK	1.0	—	ns	—
$T_3$	Data hold w.r.t. REFCLK	5.0	—	ns	—
$T_4$	Data setup w.r.t. TCLK/TCLKN	5.0	—	ns	Derived from Data setup to REFCLK and REFCLK to TCLK/TCLKN delay
$T_5$	Data hold w.r.t. TCLK/TCLKN	1.0	—	ns	Derived from Data hold from REFCLK and REFCLK to TCLK/TCLKN delay
$T_{CR}, T_{CF}$	TCLK rise and fall time	—	5.0	ns	0.8V to 2.0V, tested on a sample basis Refer to TTL Rise/Fall Time vs. Loading
$T_{SDR}, T_{SDF}$	Serial data rise and fall time	—	300	ps	20% to 80%, tested on a sample basis
$T_6$	TCLK to TCLKN skew	—	+/-1	ns	Tested on a sample basis
$T_{DC}$	TCLK, TCLKN duty cycle	45	55	%	—
Transmitter Output Jitter Allocation					
$T_J$ (RMS)	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis (refer to Figure 13)
$T_{DJ}$	Serial data output deterministic jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis (refer to Figure 13)

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**Data Sheet**

**Figure 10: VSC7106 AC Timing Waveforms**



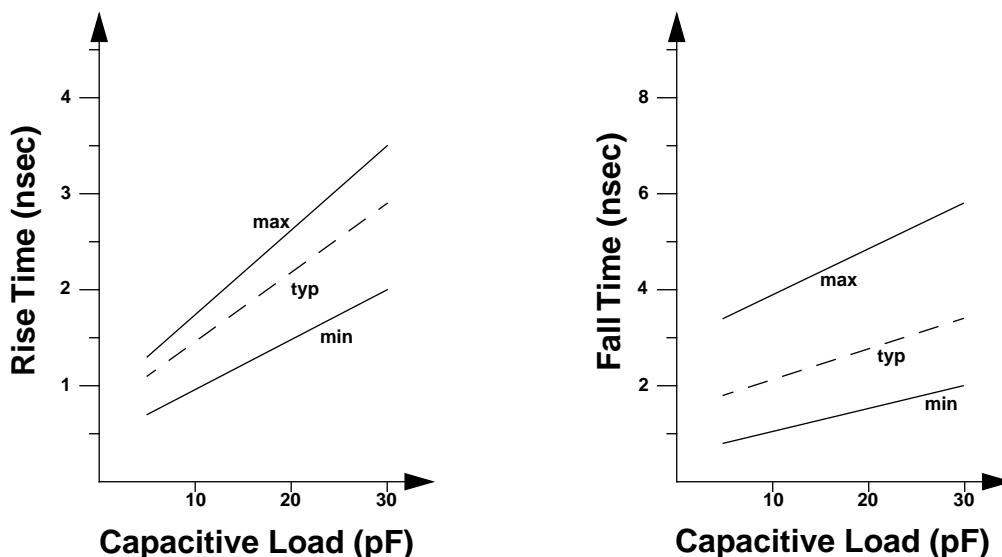
**Table 3: VSC7106 AC Characteristics**

<i>Parameters</i>	<i>Description</i>	<i>Min.</i>	<i>Max.</i>	<i>Units</i>	<i>Conditions</i>
$T_1$	RCLK or RCLKN fall to Data Valid	0.0	3.0	ns	—
$T_2$	RCLK to RCLKN skew	—	1.0	ns	Tested on sample basis
$T_{RCR}, T_{RCF}$	RCLK rise and fall time	—	5.0	ns	Between 0.8 & 2.0V, tested on a sample basis
$T_{DR}, T_{DF}$	Data output rise and fall time	—	5.0	ns	Between 0.8 & 2.0V, tested on a sample basis
$T_{LOCK}$	Data acquisition lock time @ 1.0625Gb/s	—	2.4	$\mu$ s	8B/10B IDLE pattern sample basis (refer to Figure 12).
Input Jitter Tolerance	Input data eye opening allocation at receiver input for $BER \leq 1E-12$	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask (refer to Figure 13).

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Figure 11: TTL Rise and Fall Time vs Output Loading



(VSC7105 TCLK/TCLKN: VSC7106 RCLK/RCLKN and R00:19)

Table 4: Reference Clock Requirements (VSC7105/VSC7106)

Parameters	Description	Min	Max	Units	Conditions
FR	REFCLK Frequency Range	98	113	MHz	Tested on a sample basis
FT	REFCLK Frequency Tolerance	-100	100	ppm	Note 1
TD <sub>1-2</sub>	Symmetry	40	60	%	Duty cycle at 50% pt.
SR <sub>R</sub> ,SR <sub>F</sub>	REFCLK rise and fall slew rate.	500	—	mV/ns	Note 2
—	Random jitter	—	75	ps	peak to peak

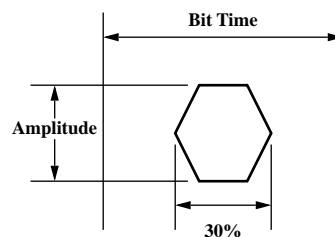
Note 1) This value is based on typical system requirements (i.e., Fibre Channel). The VSC7105 and VSC7106 can tolerate REFCLK mismatching of up to 0.5%.

2) This value assumes an AC-coupled REFCLK. Higher slew rates will minimize REFCLK's contribution to jitter due to edge-triggering ambiguity.

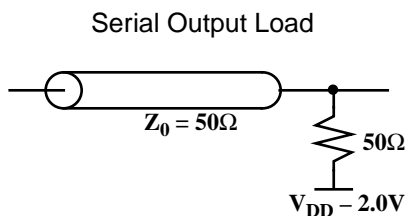
Figure 12: Parametric Measurement Information



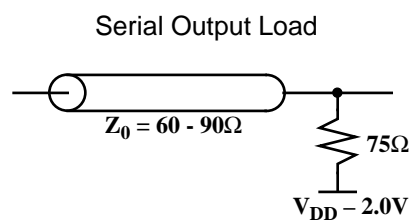
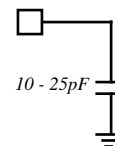
Receiver Input Eye Diagram Jitter Mask



Parametric Test Load Circuit



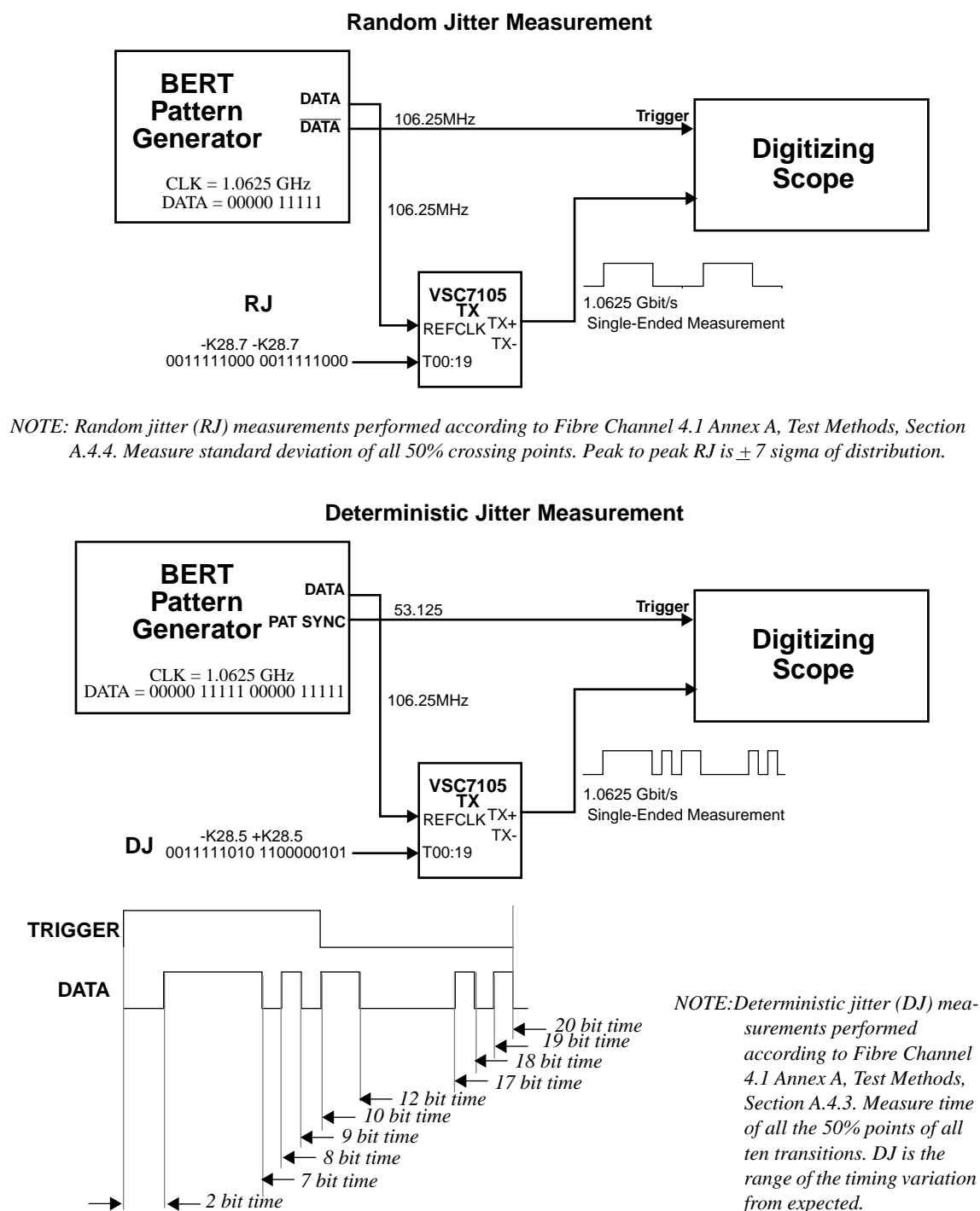
TTL A.C. Output Load



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### 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

**Figure 13: Transmitter Jitter Measurement Method**



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**Absolute Maximum Ratings** <sup>(1)</sup>

Power Supply Voltage, ( $V_{DD}$ ).....	0.5V to +4V
PECL DC Input Voltage, ( $V_{INP}$ ).....	-0.5V to $V_{DD} + 0.5V$
TTL DC Input Voltage, ( $V_{INT}$ ).....	-0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, ( $V_{IN\ TTL}$ ).....	-0.5V to $V_{DD} + 0.5V$
TTL Output Current ( $I_{OUT}$ ), (DC, Output High).....	50mA
PECL Output Current, ( $I_{OUT}$ ), (DC, Output High).....	-50mA
Case Temperature Under Bias, ( $T_C$ ).....	-55° to +125°C
Storage Temperature, ( $T_{STG}$ ).....	-65°C to +150°C

**Recommended Operating Conditions**

Power Supply Voltage, ( $V_{DD}$ ).....	+3.3V±5%
Operating Temperature Range, (T) <sup>(2)</sup> .....	0°C to +90°C

Notes:

- (1) CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
- (2) Lower limit is ambient temperature and upper limit is case temperature.



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### 1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

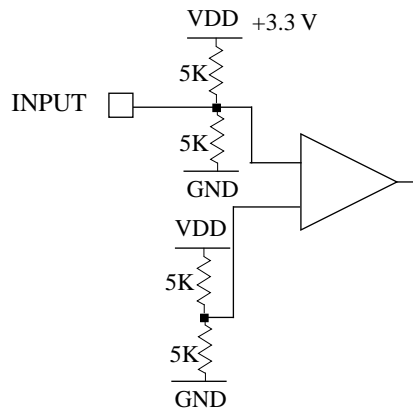
**Table 5: VSC7105 DC Characteristics** (Over recommended operating conditions).

Parameters	Description	Min	Typ	Max	Units	Conditions
V <sub>OH</sub>	Output HIGH voltage (TTL)	2.4	—	—	V	I <sub>OH</sub> = -1.2 mA
V <sub>OL</sub>	Output LOW voltage (TTL)	—	—	0.5	V	I <sub>OL</sub> = +1.2 mA
V <sub>IH</sub>	Input HIGH voltage (TTL)	2.0	—	5.5	V	I <sub>IH</sub> ≤ 6.6 mA @ V <sub>IH</sub> = 5.5 V
V <sub>IL</sub>	Input LOW voltage (TTL)	0	—	0.8	V	—
I <sub>IH</sub>	Input HIGH current (TTL)	—	—	50	μA	V <sub>IN</sub> = 2.4 V
I <sub>IL</sub>	Input LOW current (TTL)	-500	—	-50	μA	V <sub>IN</sub> = 0.5 V
V <sub>DD</sub>	Supply voltage	3.14	3.3	3.47	V	3.3V ±±-5%
I <sub>DD</sub>	Supply current	—	—	350	mA	Outputs open V <sub>DD</sub> max
P <sub>D</sub>	Power dissipation	—	1.0	1.2	W	Outputs open, @ V <sub>DD</sub> max Tcase = 20°C to 90°C.
ΔV <sub>INCLKDC</sub>	Single-ended Clock input swing (REFCLK)	600	—	1300	mVpp	Internally biased at V <sub>DD</sub> /2. See Figure 14 for input structures.
ΔV <sub>OUT</sub>	Serial Output differential peak to peak voltage swing (TX, TLX)	1200	—	2200	mVpp	50Ω to V <sub>DD</sub> - 2.0 V

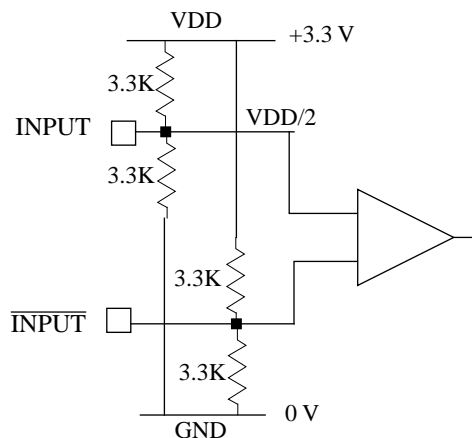
**Table 6: VSC7106 DC Characteristics** (Over recommended operating conditions).

Parameters	Description	Min	Typ	Max	Units	Conditions
V <sub>OH</sub>	Output HIGH voltage (TTL)	2.4	—	—	V	I <sub>OH</sub> = -1.2 mA
V <sub>OL</sub>	Output LOW voltage (TTL)	—	—	0.6	V	I <sub>OL</sub> = +1.2 mA
V <sub>IH</sub>	Input HIGH voltage (TTL)	2.0	—	5.5	V	I <sub>IH</sub> ≤ 6.6 mA @ V <sub>IH</sub> = 5.5 V
V <sub>IL</sub>	Input LOW voltage (TTL)	0	—	0.8	V	—
I <sub>IH</sub>	Input HIGH current (TTL)	—	—	50	μA	V <sub>IN</sub> = 2.4 V
I <sub>IL</sub>	Input LOW current (TTL)	-500	—	-50	μA	V <sub>IN</sub> = 0.5 V
V <sub>DD</sub>	Supply voltage	3.14	3.3	3.47	V	3.3V ±±-5%
I <sub>DD10</sub>	Supply current - 10-Bit Mode	—	—	520	mA	Outputs open, @ V <sub>DD</sub> max Tcase=20°C to 90°C.
I <sub>DD20</sub>	Supply current - 20-Bit Mode	—	—	560	mA	
P <sub>D10</sub>	Power Dissipation - 10-bit mode	—	—	1.8	W	Outputs Open, V <sub>DD</sub> =V <sub>DD</sub> max
P <sub>D20</sub>	Power Dissipation - 20-bit mode	—	—	1.9	W	Outputs Open, V <sub>DD</sub> =V <sub>DD</sub> max
ΔV <sub>INCLKDC</sub>	Single-ended REFCLK input swing	600	—	1300	mVpp	AC coupled
ΔV <sub>INSI</sub>	Receiver differential peak to peak input sensitivity on RX & RLX	300	—	2600	mVpp	AC coupled. See Figure 14 for input structures.

Figure 14: Input Structures



**REFCLK Input**  
(7105 : REFCLK)  
(7106 : REFCLK)

**A**

**High Speed Differential Input**  
(7106: RX/RLX)

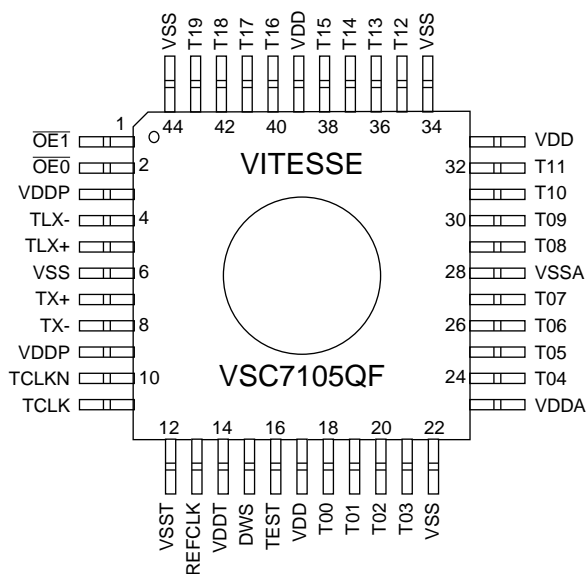
**B**

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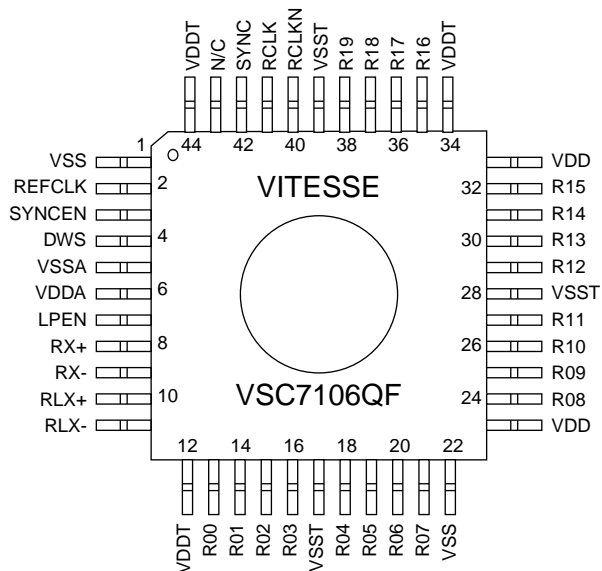
Figure 15: VSC7105/7106 Pin Diagrams

#### 44 PQFP



Heat Spreader Up  
Top View

#### 44 PQFP



Note: The heat spreader is connected to  $V_{SS}$ .

1.0625 Gbit/sec Transmitter/Receiver Chipset  
for Fibre Channel or Proprietary Serial Links

**Data Sheet**

**Table 7: VSC7105 Pin Description**

<i>Pin # 44 PQFP</i>	<i>Name</i>	<i>Description</i>																				
18-21,24-27 29-32,35-38 40-43	T00:19	INPUT - TTL Parallel data on this bus is clocked in on the falling edge of TCLK in 20 bit mode, or on the falling edge of both TCLK and TCLKN in 10 bit mode. T00 is transmitted first in 20 bit mode and T10 first in 10 bit mode.																				
16	TEST	INPUT - Multi-Level Static Input The level on this pin determines the serial encoding and the source of the bit clock to be used. The table below lists the effects caused by driving TEST to various levels. <table><tr><th><i>Level</i></th><th><i>Effect</i></th></tr><tr><td>GND</td><td>PLL 10X Multiplied Clock used as bit clock and NRZ encoding used. [Fibre Channel Compatible]</td></tr><tr><td>Tristate Open</td><td>Test Mode where REFCLK input is used as bit clock and NRZ encoding used</td></tr><tr><td>VDD</td><td>PLL 10X Multiplied Clock used as bit clock and NRZI Encoding used.</td></tr></table>	<i>Level</i>	<i>Effect</i>	GND	PLL 10X Multiplied Clock used as bit clock and NRZ encoding used. [Fibre Channel Compatible]	Tristate Open	Test Mode where REFCLK input is used as bit clock and NRZ encoding used	VDD	PLL 10X Multiplied Clock used as bit clock and NRZI Encoding used.												
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Tristate Open	Test Mode where REFCLK input is used as bit clock and NRZ encoding used																					
VDD	PLL 10X Multiplied Clock used as bit clock and NRZI Encoding used.																					
15	DWS	INPUT - Static: TTL This pin selects the parallel data bus width. When LOW, a 20 bit parallel bus width is selected and T00:19 are active. When HIGH, a 10 bit parallel data bus is selected, T10:19 are active and T00:09 are ignored.																				
2, 1	OE0 OE1	INPUT - TTL Outputs enable inputs. Select serial output state as shown in the Table below. <table><tr><th><i>OE0</i></th><th><i>OE1</i></th><th><i>TX+/TX-</i></th><th><i>TLX+/TLX-</i></th></tr><tr><td>LOW</td><td>LOW</td><td>active</td><td>active</td></tr><tr><td>LOW</td><td>HIGH</td><td>active</td><td>HIGH/LOW</td></tr><tr><td>HIGH</td><td>LOW</td><td>HIGH/LOW</td><td>active</td></tr><tr><td>HIGH</td><td>HIGH</td><td>HIGH/LOW</td><td>HIGH/LOW</td></tr></table>	<i>OE0</i>	<i>OE1</i>	<i>TX+/TX-</i>	<i>TLX+/TLX-</i>	LOW	LOW	active	active	LOW	HIGH	active	HIGH/LOW	HIGH	LOW	HIGH/LOW	active	HIGH	HIGH	HIGH/LOW	HIGH/LOW
<i>OE0</i>	<i>OE1</i>	<i>TX+/TX-</i>	<i>TLX+/TLX-</i>																			
LOW	LOW	active	active																			
LOW	HIGH	active	HIGH/LOW																			
HIGH	LOW	HIGH/LOW	active																			
HIGH	HIGH	HIGH/LOW	HIGH/LOW																			
13	REFCLK	CLOCK INPUT - Single-Ended (Biased at VDD/2, refer to Figure 14-A) A free running reference clock for the PLL clock multiplier. The frequency of REFCLK is 0.1x the desired baud rate.																				
11, 10	TCLK TCLKN	OUTPUTS - COMPLEMENTARY TTL Half word rate clock true and complement (frequency = REFCLK/2). In the 10 bit parallel data bus mode a new data word is clocked into the transmitter on the falling edge of both TCLK and TCLKN. In the 20 bit parallel data bus mode a new data word is clocked into the transmitter only on the falling edge of TCLK.																				
5,4	TLX+, TLX-	OUTPUTS - DIFFERENTIAL Serial Output (Centered at VDD - 1.32V) These outputs are functionally equivalent to TX+ and TX-.																				

### Data Sheet

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Pin # 44 PQFP	Name	Description
7,8	TX+ TX-	OUTPUTS - DIFFERENTIAL Serial Output (Centered at VDD - 1.32V) These outputs output the serial transmitted data and drive 75Ω or 50Ω termination to VDD-2V.
12	VSST	TTL Ground
14	VDDT	TTL Power Supply
3, 9	VDDP	Differential Output Power Supply
17, 33, 39	VDD	Digital Power Supply
6, 22, 34, 44	VSS	Digital and Differential Output Ground
23	VDDA	Analog Power Supply
28	VSSA	Analog Ground

**Table 8: VSC7106 Pin Description**

Pin # 44 PQFP	Name	Description
13-16,18-21, 24-27, 29-32,35-38	R00:19	OUTPUTS - TTL The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK in 20 bit mode and on the falling edges of both RCLK and RCLKN in 10 bit mode. R00 is the first bit received in 20 bit mode and R10 is the first bit received in 10 bit mode. In 10 bit mode, R00:09 are driven high.
7	LPEN	INPUT - TTL When HIGH, LPEN selects the loopback differential serial inputs pins. When LOW, LPEN selects RX+ and RX- (normal operation).
4	DWS	INPUT - Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20 bit parallel bus width is selected and R00:19 are active. When HIGH, a 10 bit parallel data bus is selected (R10:19 are active) and R00:10 will go HIGH.
41, 40	RCLK, RCLKN	OUTPUTS - COMPLEMENTARY TTL Recovered clock rate (frequency ~ REFCLK/2). The falling edge of RCLK outputs a new word on the 20 bit data bus in the 20 bit mode. The falling edge of RCLK and RCLKN outputs a new word on R10:19 in the 10 bit mode. After a sync word is detected the period of the current RCLK and RCLKN is stretched to align with the half-word boundary.
2	REFCLK	INPUT - Single-Ended Clock (Biased at VDD/2, refer to Figure 14-A) A free running reference clock for the PLL clock multiplier. The frequency of REFCLK is within ±1.00% of 0.1x the desired baud rate.
42	SYNC	OUTPUT - TTL Upon detection of a valid sync symbol this output goes high for a RCLK period in 20 bit mode. In 10 bit mode, the SYNC output goes high for half an RCLK period.
10, 11	RLX+, RLX-	INPUT - DIFFERENTIAL Serial Input (Biased at VDD/2, refer to Figure 14-B) The serial loopback data inputs. Functionally equivalent to RX+ and RX-.
8, 9	RX+, RX-	INPUT - DIFFERENTIAL Serial Input (Biased at VDD/2, refer to Figure 14-B) The received serial data inputs.

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<i>Pin # 44 PQFP</i>	<i>Name</i>	<i>Description</i>
3	SYNCEN	INPUT - STATIC: MULTI-LEVEL When tied to VDD, enables synch detection. Detection of the sync pattern (K28.5:0011111010, negative beginning running disparity) will establish the word boundary for the data to follow. When open (not connected) or tri-state, REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation sync detection is always enabled. When tied to GND, data is treated as unframed data.
12, 34, 44	VDDT	TTL Power Supply
17, 28, 39	VSST	TTL Ground
23, 33	VDD	Digital Power Supply
1, 22	VSS	Digital Ground
6	VDDA	Analog Power Supply
5	VSSA	Analog Ground

### Data Sheet

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#### Package Thermal Characteristics

The VSC7105 and VSC7106 are packaged into thermally enhanced plastic quad flatpacks. These packages use industry standard EIAJ footprints, but have been enhanced to improve thermal dissipation through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the leadframe through the heat spreader overlap of the leadframe. The construction of the package is as shown in Figure 16.

Figure 16: Package Cross Section

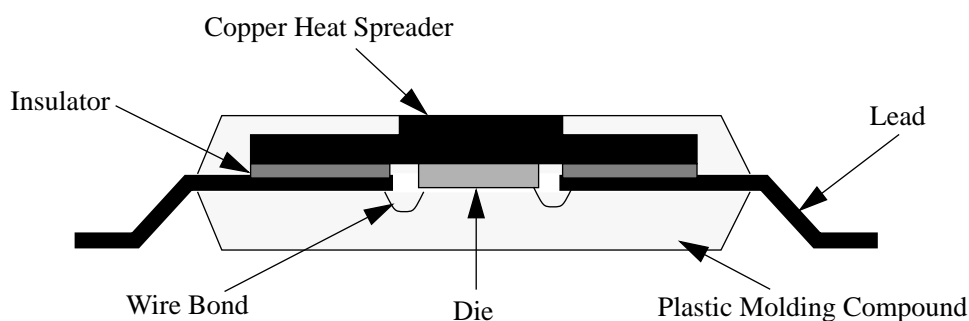


Table 9: 44 and 52 PQFP Thermal Resistance

Symbol	Description	44-pin Value	Units
$\theta_{jc}$	Thermal resistance from junction to case	2.1	°C/W
$\theta_{ca-0}$	Thermal resistance from case to ambient, still air*	30	°C/W
$\theta_{ca-100}$	Thermal resistance from case to ambient, 100 LFPM air*	24	°C/W
$\theta_{ca-200}$	Thermal resistance from case to ambient, 200 LFPM air*	21	°C/W
$\theta_{ca-300}$	Thermal resistance from case to ambient, 300 LFPM air*	19	°C/W
$\theta_{ca-500}$	Thermal resistance from case to ambient, 500 LFPM air*	15	°C/W

\*Note: Includes conduction through the leads of the package for a non-thermally saturated board.

The VSC7105 and VSC7106 are designed to operate with at a case temperature up to 90°C. The user must guarantee that the case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC7106 in still air if the ambient temperature does not exceed 36°C on a non-thermally saturated board.

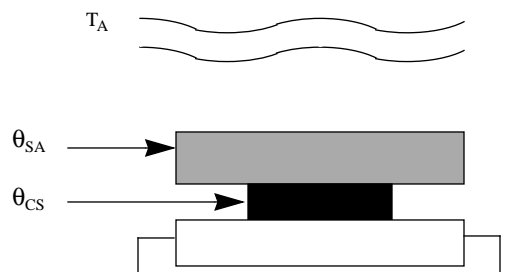
If the user's environment exceeds 36°C, then the user must either provide adequate airflow, attach a heat sink, or both. Below is an example to guide the user in determining these requirements with additional airflow and with adding a heatsink.

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**1 Thermal Resistance with Heat Sink**

The determination of appropriate heat sink to use is as shown below.

**Figure 17: Package Thermal Considerations**

where:

$q_{SA}$	Thermal resistance from heatsink to ambient [airflow dependent]
$q_{CS}$	Thermal resistance from case to heatsink [User supplied, typically < 0.6° C/W]
$T_{A(MAX)}$	Maximum Air temperature [User supplied, 70° C for this example]
$T_{C(MAX)}$	Maximum Case temperature (90° C)
$\Delta T$	$T_C - T_A$
$P_{(MAX)}$	Maximum Power Dissipation (1.9 W for VSC7106)

$$\therefore P = \frac{\Delta T}{\Sigma \theta} = \frac{T_C - T_A}{\theta_{SA} + \theta_{CS}}$$

$$\theta_{SA} = \frac{\Delta T}{P} - \theta_{CS}$$

If  $T_A = 70^\circ \text{C}$  and  $\theta_{CS}$  is  $0.6^\circ \text{C/W}$ ,

$$\theta_{SA} = \frac{(90 - 70)^\circ \text{C}}{1.9 \text{ W}} - 0.6^\circ \text{C/W}$$

$$\theta_{SA} = 10^\circ \text{C/W}$$

Therefore, to maintain the proper case and junction temperature, a heat sink with a  $\theta_{SA}$  of  $10^\circ \text{C/W}$  or less must be selected at the appropriate air flow.

**NOTE:** The heat spreader is tied to  $V_{SS}$  in both the VSC7105 and VSC7106.

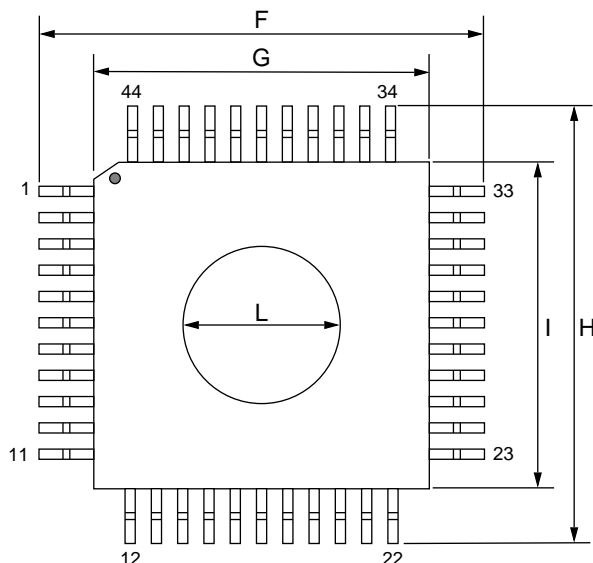


### Data Sheet

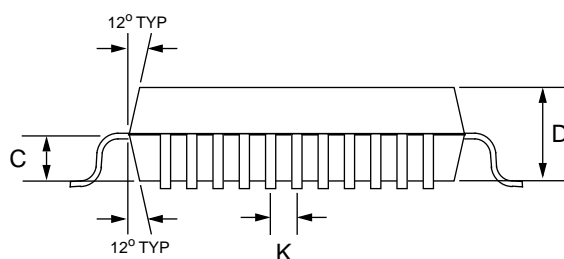
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### Package Information

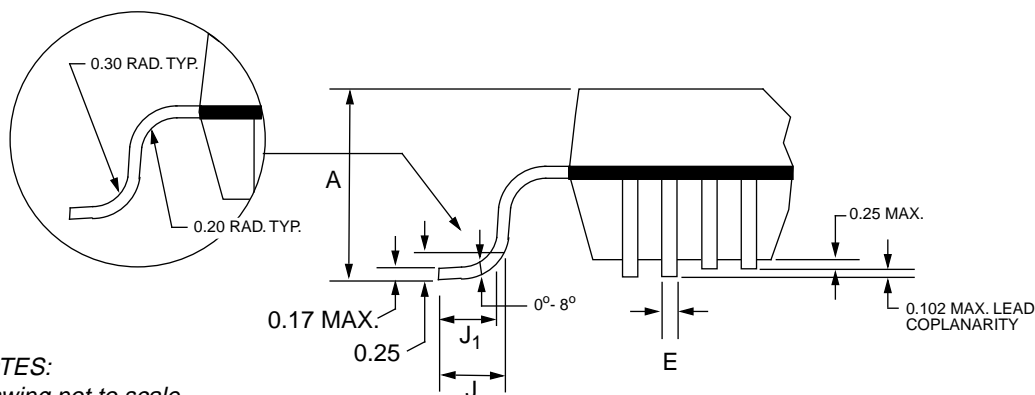
#### 44-Pin PQFP Package Drawings



Item	mm	Tol.
A	2.35	MAX
D	2.00	+0.10 / -0.05
E	0.35	±0.05
F	17.20	±0.25
G	14.00	±0.10
H	17.20	±0.25
I	14.00	±0.10
J	0.88	+0.15 / -0.10
J1	0.80	+0.15 / -0.10
K	1.00	BASIC
L	6.86	±0.50 DIA.



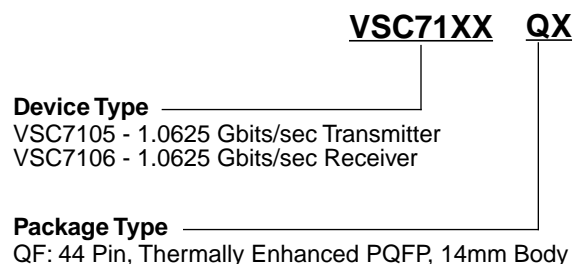
The heat spreader is tied to  $V_{SS}$



NOTES:  
Drawing not to scale.  
Heat spreader up.  
All units in mm unless otherwise noted.

**1.0625 Gbit/sec Transmitter/Receiver Chipset  
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The part number for this product is formed by a combination of the device number, package type, and the operating temperature range.

**Notice**

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